

CLAIMS

WHAT IS CLAIMED IS:

1. A power adjustment method of an upper electrode power supply of a semiconductor process apparatus, comprising:

obtaining a corresponding processing load of an upper electrode power supply of a reference process chamber ~~and a when performing a semiconductor process step and a~~ corresponding processing load of an upper electrode power supply of a current process chamber ~~corresponding to a semiconductor process step;~~

when ~~starting to perform~~ performing the semiconductor process step;

determining a ~~power~~ corresponding compensation coefficient ~~corresponding to for the~~ current process chamber when performing the semiconductor process step ~~for the current process chamber relative to the reference process chamber~~ according to the corresponding processing load of the current process chamber and the corresponding processing load of the reference process chamber; and

when the semiconductor process step is performed, controlling the upper electrode power supply of the current process chamber to output a compensation power, the compensation power being a product of a set rated power of the upper electrode power supply ~~of the current process chamber corresponding to set in~~ the semiconductor process step performed by the current process chamber and the corresponding ~~power~~ compensation coefficient.

2. The power adjustment method according to claim 1, wherein ~~determining the power~~ compensation coefficient ~~for the current process chamber relative to the reference process chamber according to the~~ is a ratio of the corresponding processing load of the current process

chamber ~~and then~~ when performing the semiconductor process step to the corresponding
processing load of the reference process chamber ~~includes;~~ when performing the semiconductor
process step.

~~calculating a ratio between the processing load of the current process chamber and the~~
~~processing load of the reference process chamber; and~~

~~using the ratio as the power compensation coefficient.~~

3. The power adjustment method according to claim 1 or 2, wherein upper electrode
circuits are arranged at the reference process chamber and the current process chamber, the upper
electrode power supply is configured to output power to the corresponding process chamber
through a corresponding upper electrode circuit, and obtaining the corresponding processing load
of the upper electrode power supply of the reference process chamber ~~and then~~ when performing
the semiconductor process step and the corresponding processing load of the upper electrode
power supply of the current process chamber ~~corresponding to~~ when performing the
semiconductor process step includes:

obtaining a plasma load ~~of the reference process chamber~~ corresponding to ~~the~~ each
semiconductor process step;

adding a circuit load ~~of~~ corresponding to the reference process chamber and the plasma
load of the performed semiconductor process step to obtain the processing load of the reference
process chamber when performing the corresponding semiconductor process step; and

adding a circuit load ~~of~~ corresponding to the current process chamber and the plasma load
of the ~~reference~~ performed semiconductor process ~~chamber~~ step to obtain the processing load of
the current process chamber when performing the corresponding semiconductor process step.

4. The power adjustment method according to claim 3, wherein obtaining the plasma load ~~of the reference process chamber~~ corresponding to ~~the each~~ semiconductor process step includes:

when performing ~~the each~~ semiconductor process step, controlling the upper electrode power supply of ~~the reference any~~ process chamber to output a processing power and detecting a process current between the upper electrode power supply and the ~~reference corresponding~~ process chamber;

obtaining the processing load of the ~~reference~~ process chamber ~~corresponding to each semiconductor process step~~ according to the processing power and the process current; and

subtracting the circuit load ~~of corresponding to the reference~~ process chamber from the processing load of the ~~reference~~ process chamber ~~corresponding to each semiconductor process step~~ to obtain the plasma load ~~of the reference corresponding to each semiconductor process chamber step~~.

5. The power adjustment method according to claim 4, wherein ~~obtaining~~ the processing load ~~of the reference process chamber according to the processing power and the process current~~ includes:

~~calculating~~ is a ratio of the processing power to square of the process current; ~~and~~ ~~using the ratio as the processing load~~.

6. The power adjustment method according to claim ~~34~~, wherein the circuit load ~~of any one of the reference process chamber and the current~~ ~~corresponding to each~~ process chamber is obtained by:

controlling the upper electrode power supply ~~of the~~corresponding to each process chamber to output detection power to detect a detection current between ~~the~~each upper electrode power supply ~~and~~the corresponding process chamber, the plasma being not ignited in the process chamber under the detection power; and

obtaining the circuit load ~~of the~~corresponding to each process chamber according to the detection power and detection current ~~of the~~corresponding to each process chamber.

7. The power adjustment method according to claim 6, wherein ~~obtaining~~ the circuit load ~~of the process chamber according to the detection power and detection current of the process chamber includes:~~

~~calculating~~is a ratio of the detection power to square of the detection current; ~~and,~~
~~using the ratio as the circuit load.~~

~~8. The power control method according to claim 3,~~
~~wherein a plurality of semiconductor process steps are provided;~~
~~after obtaining the processing load of the upper electrode power supply of the reference process chamber and the processing load of the upper electrode power supply of the current process chamber corresponding to the semiconductor process step, and before starting to perform all the semiconductor process steps, the method further comprising:~~

~~writing the obtained plasma load of the reference process chamber corresponding to each semiconductor process step of the plurality of semiconductor process steps into a parameter table;~~

~~accessing the circuit load of the reference process chamber and the circuit load of the current process chamber;~~

~~when starting to perform the semiconductor process step, determining the power compensation coefficient of the current process chamber relative to the reference process chamber corresponding to the semiconductor process step according to the processing load of the current process chamber and the processing load of the reference process chamber including:~~

~~when starting to perform the semiconductor process steps, accessing the plasma load of the reference process chamber corresponding to a current semiconductor process step in the parameter table; and~~

~~determining the power compensation coefficient of the current process chamber relative to the reference process chamber corresponding to the current semiconductor process step according to the processing load of the current process chamber and the processing load of the reference process chamber.~~

9

8. A semiconductor process apparatus comprising ~~a plurality of~~ at least one process ~~chambers~~chamber, wherein the semiconductor process apparatus is ~~configured to adjust~~capable of adjusting power of ~~an~~ upper electrode power ~~supply~~supply of the ~~plurality of~~ at least one process ~~chambers~~chamber through the power adjustment method of the upper electrode power supply ~~according to~~of any one of claims 1 to 8, ~~any one process chamber of the plurality of process chambers are used as the reference process chamber, a process chamber of the other~~

process chambers that performs the semiconductor process step is the current process chamber;

7.

the

9. The semiconductor process apparatus further comprising:

an acquisition unit configured to obtain the processing load of the upper electrode power supply of the reference process chamber and the processing load of the upper electrode power supply of the current process chamber corresponding to according to claim 8, wherein the semiconductor process step;

apparatus includes a calculation unit configured to determine the power compensation coefficient corresponding to the plurality of process chambers, and the semiconductor process step for the current process chamber relative to the reference apparatus is configured to use one of the plurality of process chambers as a reference process chamber to adjust power of upper electrode power supplies of remaining process chamber according to the processing load chambers of the current plurality of process chamber and the processing load of the reference process chamber; and chambers through the power adjustment method.

a control unit configured to, when performing the semiconductor process step, control the upper electrode power supply of the current process chamber to output the compensation power, the compensation power being the product of the set power of the upper electrode power supply of the current process chamber corresponding to the semiconductor process step and the corresponding power compensation coefficient.

10. The semiconductor process apparatus according to claim 9, wherein the acquisition unit semiconductor process apparatus further includes a plurality of current detection devices, a

~~number~~wherein the plurality of ~~the~~current detection devices ~~being the same as a number of the~~
~~process chambers, and the current detection devices being are~~ arranged between ~~the a plurality of~~
~~upper~~ electrode power supplies and ~~the~~corresponding process chambers in a one-to-one
correspondence, ~~and~~ the current detection devices ~~beingare~~ configured to obtain the process
current and/or the detection current between ~~each of~~ the ~~corresponding~~ upper electrode power
supplies and the corresponding process ~~chamberschamber~~, and the detection current
~~referringrefers~~ to a current outputted by the upper electrode power supply when the plasma is not
ignited in the process chamber.