## Claims

1. A system for clock signaling, the system comprising:

a transmitting device including:

a terminal configured to receive an initial clock signal;

a first phase lock loop configured to lock a phase of an initial periodic signal with a phase of the initial clock signal;

a down sampling module configured to down-sample the initial clock signal to a frequency of the initial periodic signal; and

a transmitting data block interface configured to construct a plurality of data blocks and provide the plurality of data blocks to a receiving device, each of the plurality of data blocks including at least one sample of the initial periodic signal; and

the receiving device including:

a receiving data block interface configured to receive the plurality of data blocks;

a second phase lock loop configured to recreate the initial periodic signal as a recreated periodic signal, and to lock a phase of the recreated periodic signal with a phase of the ~~samples~~ at least one sample of the initial periodic signal from the plurality of data blocks; and

a clock signal generator configured to recreate the initial clock signal as a recreated clock signal and to provide the recreated clock signal, the recreated clock signal being synchronized to the initial clock signal based on the phase of the recreated periodic signal.

2. The system of claim 1 wherein the transmitting data block interface is further configured to construct the plurality of data blocks to include data from the terminal.

3. The system of claim 2 wherein the receiving device further ~~comprises~~ includes a timing module configured to receive data from the plurality of data blocks received by the receiving data block interface, to receive the recreated clock signal from the clock signal generator, and to provide the data and the recreated clock signal.

~~4. The system of claim 1 wherein the transmitting device further comprises a down sampling module configured to down-sample the initial clock signal to the frequency of the initial periodic signal.~~

4~~5~~. The system of claim 1 further comprising a decimation module operating based on a first backplane clock signal, the decimation module being configured to provide a subset of samples of the initial periodic signal to the transmitting data block interface.

5~~6~~. The system of claim ~~5~~ 4 wherein the receiving data block interface operates based on ~~a~~ the first backplane clock signal.

6~~7~~. The system of claim ~~5~~ 4 wherein the receiving data block interface operates based on a second clock signal that is not the first backplane clock signal.

7~~8~~. The system of claim 1 wherein the second phase lock loop ~~further~~ comprises a second decimation module configured to generate a subset of samples of the recreated periodic signal to provide feedback and assist in locking the phase of the recreated periodic signal with the phase of the ~~samples~~ at least one sample of the initial periodic signal.

8~~9~~. The system of claim 1 wherein the transmitting data block interface and the receiving data block ~~interfaces~~ interface are time division multiplexing (TDM) interfaces.

9~~10~~. The system of claim ~~9~~ 8 wherein the plurality of data blocks are a plurality of TDM frames.

10~~11~~. The system of claim ~~9~~ 8 wherein the transmitting data block interface incorporates a plurality of bits based on the at least one sample of the initial periodic signal in each TDM frame.

11~~12~~. A method for clock signaling, the method comprising:

receiving, by a transmitting device, an initial clock signal;

locking, with a first phase lock loop, a phase of an initial periodic signal with a phase of the initial clock signal;

down-sampling the initial clock signal to a frequency of the initial periodic signal;

constructing a plurality of data blocks to be provided to a receiving device, each of the plurality of data blocks including at least one sample of the initial periodic signal;

providing the plurality of data blocks to the receiving device;

recreating the initial periodic signal to create a recreated periodic signal;

locking, with a second phase lock loop of the receiving device, a phase of the recreated periodic signal with a phase of the ~~samples~~ at least one sample of the initial periodic signal from the plurality of data blocks; and

recreating the initial clock signal as a recreated clock signal synchronized to the initial clock signal based on the locked phase of the recreated periodic signal.

12~~13~~. The method of claim ~~12~~ 11 wherein the plurality of data blocks further include data received by the transmitting device.

13~~14~~. The method of claim ~~13~~ 12 further comprising providing the data and the recreated clock signal by a timing module of the receiving device.

~~15. The method of claim 12 further comprising down-sampling the initial clock signal to the frequency of the initial periodic signal.~~

14~~16~~. The method of claim ~~12~~ 11 further comprising decimating a first backplane clock signal to provide the ~~samples~~ at least one sample of the initial periodic signal.

15~~17~~. The method of claim ~~16~~ 14 further comprising receiving, by the receiving device utilizing the first backplane clock signal, the plurality of data blocks.

16~~18~~. The method of claim ~~16~~ 14 further comprising receiving, by the receiving device utilizing a second clock signal, the plurality of data blocks, wherein the first backplane clock signal is not the second clock signal.

17~~19~~. The method of claim ~~12~~ 11 further comprising down-sampling the recreated periodic signal to provide feedback and assist in locking the phase of the recreated periodic signal with the phase of the ~~samples~~ at least one sample of the initial periodic signal.

18~~20~~. The method of claim ~~12~~ 11 wherein the plurality of data blocks are a plurality of time division multiplexing (TDM) frames.

1921. The method of claim 20 18 wherein constructing the plurality of data blocks to be provided to the receiving device comprises incorporating a plurality of bits based on the at least one sample of the initial periodic signal in each TDM frame.

2022. A system for clock signaling, the system comprising:

a transmitting device on a time division multiplexing (TDM) backplane bus, the transmitting device including:

a terminal configured to receive an initial clock signal and data;

a first phase lock loop configured to lock a phase of an initial periodic signal with a phase of the initial clock signal;

a down sampling module configured to down-sample the initial clock signal to a frequency of the initial periodic signal; and

a transmitting TDM interface configured to construct a plurality of frames, the transmitting TDM interface being further configured to store, within a control byte of each frame, at least one bit or more of a sample of the locked initial periodic signal, to store at least some of the data within one or more data bytes of each frame, and to provide the plurality of frames to a receiving device on the TDM backplane bus; and

the receiving device on the TDM backplane bus, the receiving device including:

a receiving TDM interface configured to receive the plurality of frames;

a second phase lock loop configured to recreate the initial periodic signal as a recreated periodic signal, and to lock a phase of the recreated periodic signal with a phase of the initial periodic signal based on the bits of the samples at least one bit or more of the sample of the locked initial periodic signal from the plurality of frames received by the receiving TDM interface; and

a clock signal generator configured to recreate the initial clock signal as a recreated clock signal, to provide the recreated clock signal, and to provide the data from the data bytes of the plurality of frames received by the receiving TDM interface, the recreated clock signal being synchronized to the initial clock signal based on the phase of the recreated periodic signal.