

SEMICONDUCTOR PACKAGE STRUCTURE HAVING HOLLOW CHAMBER AND BOTTOM SUBSTRATE AND PACKAGE PROCESS THEREOF

FIELD OF THE INVENTION

The present invention generally relates to a semiconductor package structure, particularly represents the semiconductor package structure having hollow chamber.

BACKGROUND OF THE INVENTION

Conventional micro-electromechanical system (MEMS) package technology is performed as following: forming a connection portion on a substrate; disposing electronic components (such as resistor, transistor, radio frequency apparatus, integrated circuit or capacitor) on the substrate; coating a solder paste on the connection portion of the substrate by way of screen printing; disposing a cover on the connection portion and packaging by thermal compression to form a hollow chamber between the substrate and the cover. The electronic components can operate steadily in the hollow chamber. The conventional substrate incapable of fine-pitch package due to screen printing process requires larger area for solder paste coating, therefore, fine-pitch substrate development for shrinking package size is essential in MEMS package technology.

SUMMARY

The primary object of the present invention is that a connection layer is formed on a bottom metal layer of a bottom substrate by reflowing solder balls, and a top substrate connects to the bottom substrate via the connection layer. The bottom metal layer with particular corner is able to prevent

overflow or undulating surface of the connection layer in formation process, furthermore prevent pollution because of overflow and enhance surface coplanarity of the connection layer.

A semiconductor package structure having hollow chamber of the present invention includes a bottom substrate, a connection layer and a top substrate. The bottom substrate comprises a bottom baseboard and a bottom metal layer, wherein the bottom baseboard comprises a surface having a disposing area, at least one first exposing area and a second exposing area. The disposing area is a closed loop and surrounds the second exposing area. The bottom metal layer is formed on the disposing area and comprises at least one corner having a first outer lateral surface, a second outer lateral surface and an outer connection surface located between the first outer lateral surface and the second outer lateral surface, wherein the outer connection surface connects the first outer lateral surface and the second outer lateral surface. The first outer lateral surface comprises a first bottom edge having a first extreme point, and a first extension line is formed extendedly from the first extreme point. The second outer lateral surface comprises a second bottom edge having a second extreme point, and a second extension line is formed extendedly from the second extreme point, wherein a cross point is formed by crossing the first extension line and the second extension line, and the first exposing area is defined by connecting the cross point, the first extreme point and the second extreme point. The connection layer is formed on the bottom metal layer. The top substrate comprises a connection surface, wherein the connection surface connects to the connection layer to form a hollow chamber between the top substrate and the bottom substrate.

In this invention, the top substrate connects to the bottom substrate via the connection layer formed by reflowing solder balls to form the sealed hollow chamber for accommodating an electronic component. Besides, use solder ball reflowing process to reduce the width of the bottom metal layer and further shrink the size of the semiconductor package structure having hollow chamber. And the corner of the bottom metal layer is able to prevent pollution problems result from overflow of the connection layer, or inadequate adaptation result from inadequate coplanarity of the connection layer, therefore, it is able to improve the yield rate of the semiconductor package structure having hollow chamber.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a flow chart illustrating a package process of semiconductor package structure having hollow chamber in accordance with a first embodiment of the present invention.

Fig. 2 is a perspective diagram illustrating a bottom baseboard in accordance with the first embodiment of the present invention.

Fig. 3 is a perspective diagram illustrating a bottom substrate in accordance with the first embodiment of the present invention.

Fig. 4 is a diagram illustrating the package process of semiconductor package structure having hollow chamber in accordance with the first embodiment of the present invention.

Fig. 5 is a diagram illustrating the package process of semiconductor package structure having hollow chamber in accordance with the first embodiment of the present invention.

Fig. 6 is a diagram illustrating the package process of semiconductor package structure having hollow chamber in accordance with the first

embodiment of the present invention.

Fig. 7 is a diagram illustrating the package process of semiconductor package structure having hollow chamber in accordance with the first embodiment of the present invention.

Fig. 8 is a perspective diagram illustrating a bottom substrate in accordance with a second embodiment of the present invention.

Fig. 9 is an SEM image of reference bottom substrate.

Fig. 10 is an SEM image of the bottom substrate in accordance with the second embodiment of the present invention.

Fig. 11 is a perspective diagram illustrating a bottom substrate in accordance with a third embodiment of the present invention.

Fig. 12 is a section diagram illustrating the semiconductor package structure having hollow chamber in accordance with a fourth embodiment of the present invention.

Fig. 13 is a section diagram illustrating the semiconductor package structure having hollow chamber in accordance with a fifth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A flow chart of a package process of semiconductor package structure having hollow chamber 10 in accordance with a first embodiment of the present invention is illustrated in Fig. 1, the package process of semiconductor package structure having hollow chamber 10 includes step 11 of providing a bottom baseboard, step 12 of forming an bottom metal layer on disposing area, step 13 of disposing a plurality of solder balls on bottom metal layer, step 14 of reflowing solder balls, and step 15 of connecting a top substrate to a bottom substrate.

With reference to Figs. 1 and 2, in the step 11 of providing a bottom baseboard 110, the bottom baseboard 110 is selected from one of silicone, ceramic, glass, metal, polymer or other semiconductor materials. Referring to Fig. 2, the bottom baseboard 110 comprises a surface 111 having a disposing area 111a, at least one first exposing area 111b and a second exposing area 111c, wherein the disposing area 111a is a closed loop and surrounds the second exposing area 111c. An electronic component E is disposed on the second exposing area 111c.

With reference to Figs. 1 and 3, in the step 12 of forming a bottom metal layer 120 on the disposing area 111a, a bottom substrate 100 is composed of the bottom baseboard 110 and the bottom metal layer 120. In this embodiment, the bottom metal layer 120 is formed on the disposing area 111a by conventional photolithography process and electroplating/chemical plating process, and the bottom metal layer 120 is a multilayer metal structure or alloy used for adhesion, moisture and barrier, wherein material of the bottom metal layer 120 includes Titanium (Ti), Titanium/Wolfram (Ti/W), Copper (Cu), Chromium (Cr) and Nickel/Vanadium (Ni/V).

With reference to Fig. 3, the bottom metal layer 120 comprises at least one corner 121, and the bottom metal layer 120 comprises four corners 121 in this embodiment. The corner 121 comprises a first outer lateral surface 121a, a second outer lateral surface 121b and an outer connection surface 121c located between the first outer lateral surface 121a and the second outer lateral surface 121b, wherein the outer connection surface 121c connects the first outer lateral surface 121a and the second outer lateral surface 121b. The outer connection surface 121c is planar or curved, and the outer connection surface 121c is planar in this embodiment. The first outer

lateral surface 121a comprises a first bottom edge S1 having a first extreme point P1, and a first extension line L1 is formed extendedly from the first extreme point P1. The second outer lateral surface 121b comprises a second bottom edge S2 having a second extreme point P2, and a second extension line L2 is formed extendedly from the second extreme point P2, wherein a cross point P is formed by crossing the first extension line L1 and the second extension line L2, and the first exposing area 111b is defined by connecting the cross point P, the first extreme point P1 and the second extreme point P2. In this embodiment, the surface 111 of the bottom baseboard 110 relative to the corner 121 of the bottom metal layer 120 comprises four first exposing areas 111b.

With reference to Fig. 3, in this embodiment, the corner 121 of the bottom metal layer 120 further comprises a first inner lateral surface 121d opposite to the first outer lateral surface 121a and a second inner lateral surface 121e opposite to the second outer lateral surface 121b, wherein the first inner lateral surface 121d and the second inner lateral surface 121e face toward the second exposing area 111c. Preferably, the first inner lateral surface 121d is substantially parallel to the first outer lateral surface 121a, and the second inner lateral surface 121e is substantially parallel to the second outer lateral surface 121b. A first width W1 is defined between the first outer lateral surface 121a and the first inner lateral surface 121d, wherein the first width W1 is the shortest distance between the first outer lateral surface 121a and the first inner lateral surface 121d. A second width W2 is defined between the second outer lateral surface 121b and the second inner lateral surface 121e, wherein the second width W2 is the shortest distance between the second outer lateral surface 121b and the second inner

lateral surface 121e. In this embodiment, the first width W1 is substantially equal to the second width W2, and both of the first width W1 and the second width W2 are between 150 μ m and 400 μ m. A connection width W is defined between edge of the second exposing area 111c and the outer connection surface 121c, wherein the connection width W is the shortest distance between edge of the second exposing area 111c and the outer connection surface 121c. In this embodiment, the ratio of the first width W1 to the connection width W is 1:0.8 to 1:1.4, and the ratio of the second width W2 to the connection width W is also 1:0.8 to 1:1.4.

With reference to Figs. 1, 4 and 5, in the step 13 of disposing a plurality of solder balls B on the bottom metal layer 120, each of the solder balls B has a diameter D and there is a spacing G between two adjacent solder balls B, wherein the spacing G is not smaller than half of the diameter D of the solder balls B to prevent position deviation of the solder balls B result from collision between two adjacent solder balls B. Besides, if the spacing G between two adjacent solder balls B is too large, a gap between two adjacent solder balls B may be formed after reflow because that two adjacent solder balls B might be unable to connect mutually. In this embodiment, the ratio of the diameter D of the solder balls B to the spacing G between two adjacent solder balls B is 1:0.5 to 1:3. Preferably, the solder balls B are selected from one of Tin (Sn), Bismuth (Bi), Indium (In), Gold/Tin (Au/Sn), Tin/Silver (Sn/Ag), Tin/Copper (Sn/Cu), Ti/Bismuth (Sn/Bi), Ti/Silver/Copper (Sn/Ag/Cu), Ti/Silver/Bismuth (Sn/Ag/Bi) or Tin/Silver/Copper/Antimony (Sn/Ag/Cu/Sb) lead-free solder material.

With reference to Figs. 1 and 6, in the step 14 of reflowing the solder balls B, the solder balls B are melted and connect mutually to form a

connection layer 200 on the bottom metal layer 120, wherein the connection layer 200 forms a spherical-shaped surface because of surface tension. In this embodiment, the connection layer 200 completely covers the surface of the bottom metal layer 120. Reflow temperature depends on the melting point of the solder balls B, preferably, reflow temperature is 0 to 80 degrees higher than the melting point of the solder balls B to ensure the solder balls B melted completely in the reflow process. Besides, the connection layer 200 formed after reflow process possible overflows from the bottom metal layer 120 to pollute the electronic component E or the package structure when the solder balls B are oversize. Conversely, the connection layer 200 formed after reflow process may be unable to cover the bottom metal layer 120 completely when the solder balls B are too small. With reference to Fig. 5, in this embodiment, the ratio of the diameter D of the solder balls B to the first width W1 is 1:0.5 to 1:3 for preventing overflow or incomplete covering.

With reference to Figs. 1 and 7, in the step 15 of connecting a top substrate 300 to the bottom substrate 100, preferably, the top substrate 300 connects to the bottom substrate 100 by reflow process or thermal compression. The top substrate 300 comprises a joint surface 310 connected with the connection layer 200 for forming a hollow chamber C between the top substrate 300 and the bottom substrate 100. The hollow chamber C is used to accommodate the electronic component E for external insulation and stability enhancement. In this embodiment, the top substrate 300 comprises a top metal layer 320 formed on the joint surface 310, therefore, the joint surface 310 of the top substrate 300 connects with the connection layer 200 via the top metal layer 320 when the top substrate 300 connects to the

bottom substrate 100. Material of the top metal layer 320 includes Titanium (Ti), Titanium/Tungsten (Ti/W), Copper (Cu), Chrome (Cr) and Nickel/Vanadium (Ni/V), wherein the top metal layer 320 is used for adhesion, moisture and barrier.

Because the connection layer 200 formed by reflowing the solder balls B has fine fluidity on the bottom metal layer 120, so the connection layer 200 is able to flow toward any direction to cover the bottom metal layer 120 completely. When the connection layer 200 flows toward the corner 121 of the bottom metal layer 120, the connection layer 200 maintains fine fluidity at the corner 121 by the outer connection surface 121c of the corner 121, to prevent the connection layer 200 from accumulating on the corner 121, enhance surface coplanarity of the connection layer 200, and further enhance the adaptation between the bottom substrate 100 and the top substrate 300.

A second embodiment of the present invention is illustrated in Fig. 8, the primary difference between the first and second embodiments is that the corner 121 of the bottom metal layer 120 further comprises an inner connection surface 121f opposite to the outer connection surface 121c in the second embodiment, wherein the inner connection surface 121f connects and locates between the first inner lateral surface 121d and the second inner lateral surface 121e. The inner connection surface 121f is planar or curved, and the inner connection surface 121f is planar in this embodiment, and the inner connection surface 121f is substantially parallel to the outer connection surface 121c. The shortest distance between the inner connection surface 121f and the outer connection surface 121c is substantially equal to the connection width W (the shortest distance between edge of the second exposing area 111c and the outer connection surface 121c). An included

angle θ is defined between the inner connection surface 121f and the first inner lateral surface 121d, wherein the included angle θ is smaller than 180 degrees. The connection width W is substantially equal to the first width W1 and the second width W2 because of the inner connection surface 121f, so the inner connection surface 121f is able to further enhance surface coplanarity of the connection layer 200.

An SEM image of reference bottom substrate is illustrated in Fig. 9 used for showing height distribution of the connection layer 200 at diagonal position of the reference bottom substrate. The corner of reference bottom substrate does not possess the outer connection surface 121c and the inner connection surface 121f, therefore the corner of reference bottom substrate is right angle. With reference to Fig. 9, the connection layer 200 formed after reflow process accumulates at inside corner of reference bottom substrate, therefore a asymmetric structure of the connection layer 200 is formed at the corner of reference bottom substrate. The asymmetric connection layer will affect surface coplanarity of the connection layer 200 and adaptation of the substrate package.

An SEM image of the bottom substrate 100 of this embodiment is illustrated in Fig. 10 used for showing height distribution of the connection layer 200 at diagonal position of the bottom substrate 100. With reference to Fig. 10, the connection layer 200 formed after reflow process displays symmetric at the corner 121 of the bottom metal layer 120, to prove that the outer connection surface 121c and the inner connection surface 121f of the corner 121 is able to prevent accumulation of the connection layer 200, so the corner 121 is able to enhance coplanarity of the connection layer 200, and further enhance adaptation between the bottom substrate 100 and the top

substrate 300. Coplanarity of the connection layer 200 of this embodiment is 1.7 μm , and coplanarity of the connection layer 200 of reference bottom substrate is 10.2 μm , it is clear to know that the outer connection surface 121c and the inner connection surface 121f of the present invention enables to enhance coplanarity of the connection layer 200 availably.

A third embodiment of the present invention is illustrated in Fig. 11, the difference between the first and the third embodiments is that the surface 111 of the bottom baseboard 110 further comprises a third exposing area 111d surrounding the disposing area 111a and the first exposing area 111b in the third embodiment, wherein the first exposing area 111b locates between the third exposing area 111d and the disposing area 111a. The third exposing area 111d is used to provide allowance to improve the yield rate in package process.

A fourth embodiment of the present invention is illustrated in Fig. 12, the difference between the first and fourth embodiments is that the bottom baseboard 110 of the bottom substrate 100 further comprises a bottom protrusion portion 112 in the fourth embodiment, wherein the disposing area 111a and the first exposing area 111b are located on the surface of the bottom protrusion portion 112. A fifth embodiment of the present invention is illustrated in Fig. 13, the difference between the first and the fifth embodiments is that the top substrate 300 further comprises an top baseboard 330 having an top protrusion portion 331, wherein the joint surface 310 is the surface of the top protrusion portion 331. The height of the hollow chamber C increased by the bottom protrusion portion 112 of the fourth embodiment or the top protrusion portion 331 of the fifth embodiment is able to accommodate higher electronic component or vertical operation

electronic component.

In the present invention, a semiconductor package structure A is formed by steps 11-15 of the package process, wherein the top substrate 300 connects to the bottom substrate 100 via the connection layer 200 formed by reflowing the solder balls B. Owing to the diameter D of the solder balls B is micrometer level, so the width of the bottom metal layer 120 and the size of the semiconductor package structure A having hollow chamber are able to be reduced effectively. And coplanarity of the connection layer 200 and adaptation between the top substrate 300 and the bottom substrate 100 are enhanced effectively by the outer connection surface 121c of the corner 121.

While this invention has been particularly illustrated and described in detail with respect to the preferred embodiments thereof, it will be clearly understood by those skilled in the art that is not limited to the specific features shown and described and various modified and changed in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is:

1. A semiconductor package structure having hollow chamber (A) includes:
 - a bottom substrate (100) having a bottom baseboard (110) and a bottom metal layer (120), wherein the bottom baseboard (110) comprises a surface (111) having a disposing area (111a), at least one first exposing area (111b) and a second exposing area (111c), the disposing area (111a) is a closed loop and surrounds the second exposing area (111c), the bottom metal layer (120) is formed on the disposing area (111a) and comprises at least one corner (121) having a first outer lateral surface (121a), a second outer lateral surface (121b) and an outer connection surface (121c) located between the first outer lateral surface (121a) and the second outer lateral surface (121b), and the outer connection surface (121c) connects the first outer lateral surface (121a) and the second outer lateral surface (121b), wherein the first outer lateral surface (121a) comprises a first bottom edge (S1) having a first extreme point (P1), a first extension line (L1) is formed extendedly from the first extreme point (P1), and the second outer lateral surface (121b) comprises a second bottom edge (S2) having a second extreme point (P2), a second extension line (L2) is formed extendedly from the second extreme point (P2), wherein a cross point (P) is formed by crossing the first extension line (L1) and the second extension line (L2), and the first exposing area (111b) is defined by connecting the cross point (P), the first extreme point (P1) and the second extreme point (P2);
 - a connection layer (200) formed on the bottom metal layer (120); and
 - a top substrate (300) having a joint surface (310), wherein the joint surface (310) connects to the connection layer (200) to form a hollow

chamber (C) between the top substrate (300) and the bottom substrate (100).

2. The semiconductor package structure having hollow chamber (A) in accordance with claim 1, wherein the corner (121) of the bottom metal layer (120) further comprises a first inner lateral surface (121d) opposite to the first outer lateral surface (121a) and a second inner lateral surface (121e) opposite to the second outer lateral surface (121b), the first inner lateral surface (121d) and the second inner lateral surface (121e) face toward the second exposing area (111c), wherein a first width (W1) defined between the first outer lateral surface (121a) and the first inner lateral surface (121d) is the shortest distance between the first outer lateral surface (121a) and the first inner lateral surface (121d), and a connection width (W) defined between edge of the second exposing area (111c) and the outer connection surface (121c) is the shortest distance between edge of the second exposing area (111c) and the outer connection surface (121c), wherein the ratio of the first width (W1) to the connection width (W) is 1:0.8 to 1:1.4.
3. The semiconductor package structure having hollow chamber (A) in accordance with claim 2, wherein the corner (121) of the bottom metal layer (120) further comprises an inner connection surface (121f) opposite to the outer connection surface (121c), the inner connection surface (121f) connects and locates between the first inner lateral surface (121d) and the second inner lateral surface (121e), wherein an included angle (θ) is defined between the inner connection surface (121f) and the first inner lateral surface (121d), and the included angle (θ) is smaller than 180 degrees.

4. The semiconductor package structure having hollow chamber (A) in accordance with claim 1, wherein the connection layer (200) is formed by reflowing a plurality of solder balls(B).
5. The semiconductor package structure having hollow chamber (A) in accordance with claim 1, wherein the bottom baseboard (110) further comprises a bottom protrusion portion (112), the disposing area (111a) and the first exposing area (111b) are located on the bottom protrusion portion (112) surface.
6. The semiconductor package structure having hollow chamber (A) in accordance with claim 1, wherein the top substrate (300) comprises a top metal layer (320) formed on the joint surface (310) of the top substrate (300), the joint surface (310) connects to the connection layer (200) via the top metal layer (320).
7. The semiconductor package structure having hollow chamber (A) in accordance with claim 6, wherein the top substrate (300) further comprises a top baseboard (330) having a top protrusion portion (331), the joint surface (310) is the top protrusion portion (331) surface.
8. The semiconductor package structure having hollow chamber (A) in accordance with claim 1, wherein the surface (111) of the bottom baseboard (110) further comprises a third exposing area (111d) surrounding the disposing area (111a) and the first exposing area (111b), the first exposing area (111b) is located between the third exposing area (111d) and the disposing area (111a).
9. A bottom substrate (100) of a semiconductor package structure having hollow chamber (A) includes:
a bottom baseboard (110) having a surface (111), wherein the surface

(111) comprises a disposing area (111a), at least one first exposing area (111b) and a second exposing area (111c), the disposing area (111a) is a closed loop and surrounds the second exposing area (111c); and
a bottom metal layer (120) formed on the disposing area (111a), wherein the bottom metal layer (120) comprises at least one corner (121) having a first outer lateral surface (121a), a second outer lateral surface (121b) and an outer connection surface (121c) located between the first outer lateral surface (121a) and the second outer lateral surface (121b), and the outer connection surface (121c) connects the first outer lateral surface (121a) and the second outer lateral surface (121b), wherein the first outer lateral surface (121a) comprises a first bottom edge (S1) having a first extreme point (P1), a first extension line (L1) is formed extendedly from the first extreme point (P1), and the second outer lateral surface (121b) comprises a second bottom edge (S2) having a second extreme point (P2), a second extension line (L2) is formed extendedly from the second extreme point (P2), wherein a cross point (P) is formed by crossing the first extension line (L1) and the second extension line (L2), and the first exposing area (111b) is defined by connecting the cross point (P), the first extreme point (P1) and the second extreme point (P2).

10. The bottom substrate (100) of a semiconductor package structure having hollow chamber (A) in accordance with claim 9, wherein the corner (121) of the bottom metal layer (120) further comprises a first inner lateral surface (121d) opposite to the first outer lateral surface (121a) and a second inner lateral surface (121e) opposite to the second outer lateral surface (121b), the first inner lateral surface (121d) and the second inner lateral surface face (121e) toward the second exposing area (111c),

wherein a first width (W1) defined between the first outer lateral surface (121a) and the first inner lateral surface (121d) is the shortest distance between the first outer lateral surface (121a) and the first inner lateral surface (121d), and a connection width (W) defined between edge of the second exposing area (111c) and the outer connection surface (121c) is the shortest distance between edge of the second exposing area (111c) and the outer connection surface (121c), wherein the ratio of the first width (W1) to the connection width (W) is 1:0.8 to 1:1.4.

11. The bottom substrate (100) of a semiconductor package structure having hollow chamber (A) in accordance with claim 10, wherein the corner (121) of the bottom metal layer (120) further comprises an inner connection surface (121f) opposite to the outer connection surface (121c), the inner connection surface (121f) connects and locates between the first inner lateral surface (121d) and the second inner lateral surface (121e), wherein an included angle (θ) is defined between the inner connection surface (121f) and the first inner lateral surface (121d), and the included angle (θ) is smaller than 180 degrees.
12. The bottom substrate (100) of a semiconductor package structure having hollow chamber (A) in accordance with claim 9, wherein the bottom baseboard (110) further comprises a bottom protrusion portion (112), the disposing area (111a) and the first exposing area (111b) are located on the bottom protrusion portion (112) surface.
13. The bottom substrate (100) of a semiconductor package structure having hollow chamber (A) in accordance with claim 9, wherein the surface (111) of the bottom baseboard (110) further comprises a third exposing area (111d) surrounding the disposing area (111a) and the first exposing area

(111b), the first exposing area (111b) is located between the third exposing area (111d) and the disposing area (111a).

14. A package process of a semiconductor package structure having hollow chamber (A) includes:

providing a bottom baseboard (110) having a surface (111), wherein the surface (111) comprises a disposing area (111a), at least one first exposing area (111b) and a second exposing area (111c), the disposing area (111a) is a closed loop and surrounds the second exposing area (111c);

forming an bottom metal layer (120) on the disposing area (111a), wherein the bottom metal layer (120) comprises a corner (121) having a first outer lateral surface (121a), a second outer lateral surface (121b) and an outer connection surface (121c) located between the first outer lateral surface (121a) and the second outer lateral surface (121b), and the outer connection surface (121c) connects the first outer lateral surface (121a) and the second outer lateral surface (121b), wherein the first outer lateral surface (121a) comprises a first bottom edge (S1) having a first extreme point (P1), a first extension line (L1) is formed extendedly from the first extreme point (P1), and the second outer lateral surface (121b) comprises a second bottom edge (S2) having a second extreme point (P2), a second extension line (L2) is formed extendedly from the second extreme point (P2), wherein a cross point (P) is formed by crossing the first extension line (L1) and the second extension line (L2), and the first exposing area (111b) is defined by connecting the cross point (P), the first extreme point (P1) and the second extreme point (P2), wherein a bottom substrate (100) is composed of the bottom baseboard (110) and the bottom metal layer

(120);

disposing a plurality of solder balls (B) on the bottom metal layer (120);
reflowing the solder balls (B) for making the solder balls (B) melt and
connect mutually to form a connection layer (200) on the bottom metal
layer (120); and

connecting a top substrate (300) with a joint surface (310) to the bottom
substrate (100), wherein the joint surface (310) connects to the
connection layer (200) to form a hollow chamber (C) between the top
substrate (300) and the bottom substrate (100).

15. The package process of a semiconductor package structure having hollow
chamber (A) in accordance with claim 14, wherein the corner (121) of the
bottom metal layer (120) further comprises a first inner lateral surface
(121d) opposite to the first outer lateral surface (121a) and a second inner
lateral surface (121e) opposite to the second outer lateral surface (121b),
the first inner lateral surface (121d) and the second inner lateral surface
(121e) face toward the second exposing area (111c), wherein a first width
(W1) defined between the first outer lateral surface (121a) and the first
inner lateral surface (121d) is the shortest distance between the first outer
lateral surface (121a) and the first inner lateral surface (121d), and a
connection width (W) defined between edge of the second exposing area
(111c) and the outer connection surface (121c) is the shortest distance
between edge of the second exposing area (111c) and the outer
connection surface (121c), wherein the ratio of the first width (W1) to the
connection width (W) is 1:0.8 to 1:1.4.

16. The package process of a semiconductor package structure having hollow
chamber (A) in accordance with claim 15, wherein the corner (121) of the

- bottom metal layer (120) further comprises an inner connection surface (121f) opposite to the outer connection surface (121c), the inner connection surface (121f) connects and locates between the first inner lateral surface (121d) and the second inner lateral surface (121e), wherein an included angle (θ) is defined between the inner connection surface (121f) and the first inner lateral surface (121d), and the included angle (θ) is smaller than 180 degrees.
17. The package process of a semiconductor package structure having hollow chamber (A) in accordance with claim 15, wherein each of the solder balls (B) comprises a diameter (D), the ratio of the diameter (D) to the first width (W1) is 1:0.5 to 1:3.
18. The package process of a semiconductor package structure having hollow chamber (A) in accordance with claim 14, wherein each of the solder balls (B) comprises a diameter (D), and there is a spacing (G) between two adjacent solder balls (B), the spacing (G) is not smaller than half of the diameter (D) of the solder balls (B).
19. The package process of a semiconductor package structure having hollow chamber (A) in accordance with claim 18, wherein the ratio of the diameter (D) of the solder balls (B) to the spacing (G) between two adjacent solder balls (B) is 1:0.5 to 1:3.
20. The package process of a semiconductor package structure having hollow chamber (A) in accordance with claim 14, wherein the bottom baseboard (110) further comprises a bottom protrusion portion (112), the disposing area (111a) and the first exposing area (111b) are located on the bottom protrusion portion (112) surface.
21. The package process of a semiconductor package structure having hollow

chamber (A) in accordance with claim 14, wherein the top substrate (300) further comprises a top metal layer (320) formed on the joint surface (310) of the top substrate (300), and the joint surface (310) connects to the connection layer (200) via the top metal layer (320).

22. The package process of a semiconductor package structure having hollow chamber (A) in accordance with claim 21, wherein the top substrate (300) further comprises a top baseboard (330) having a top protrusion portion (331), the joint surface (310) is the top protrusion portion (331) surface.

23. The package process of a semiconductor package structure having hollow chamber (A) in accordance with claim 14, wherein the surface (111) of the bottom baseboard (110) further comprises a third exposing area (111d) surrounding the disposing area (111a) and the first exposing area (111b), the first exposing area (111b) is located between the third exposing area (111d) and the disposing area (111a).