

PATENT SPECIFICATION

(11) 1 534 336

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- (21) Application No. 4625/76 (22) Filed 5 Feb. 1976
 (31) Convention Application No. 50/016280
 (32) Filed 10 Feb. 1975 in
 (33) Japan (JP)
 (44) Complete Specification published 6 Dec. 1978
 (51) INT CL² G11C 17/00
 (52) Index at acceptance
 G4C 17B4 2JX RM



(54) IMPROVEMENTS IN SEMICONDUCTOR READ ONLY MEMORIES

(71) We, HITACHI, LTD of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a semiconductor read only memory (hereinafter referred to as a "ROM"), comprising a memory matrix and a row selection matrix.

In general, a circuit in which both a memory matrix and an address decoder are constructed of ROMs employs ROMs of the lateral type (ROMs in which a plurality of driving MISFETs are connected in parallel between an output terminal and a reference voltage terminal) which have been described in 'Electronics Digest' December, 1973, pp. 49—50, "7. READ only MEMORY" etc.

Figure 1 of the accompanying drawings shows an address decoder, more especially a word address decoder, ROM 1, and a memory matrix ROM 2, which are of the above type. In the Figure, the word address decoder ROM 1 decodes an encoded address signal applied from address input lines A_1 , A_1 , A_2 and A_2 and selects one of the word address select lines W_1 — W_4 . The memory matrix ROM 2 is a ROM which stores 12 bits of information (4 words $\times$ 3 bits). The stored contents (3 bits of a information) of the selected column (word) in the ROM are read out from bit output lines B_1 — B_3 .

In the memory matrix ROM 2, the selected word address select line is at the supply voltage V_{DD} , whereas the non-selected word address select lines are at earth potential.

This means that, in the word address decoder ROM 1, currents flow through all but one of load MISFETs Q_{L1} — Q_{L4} which are connected to the word address line

W_1 — W_4 . As a result, the power which is dissipated in the word address decoder ROM 1 is high. If the memory capacity of the memory matrix ROM 2 is increased, the number of non-selected word address select lines goes up accordingly, and the problem becomes more serious.

Figure 2A of the accompanying drawings shows a pattern diagram of a part of the memory matrix ROM 2 illustrated in Figure 1, assembled as a P-channel MISLSI chip. Figure 2B is a front section taken along A—A' of Figure 2A.

The chip includes a portion 3 formed of Si, which forms gate electrodes for the MISFETs located in each column, and which is also the word address select line. There is a source region 5 for each MISFET, and an interconnection layer 4 earths the source regions 5 of the MISFETs. Each MISFET has a drain region 6. The earthed interconnection layer 4, the source region 5 and the drain region 6 are all formed of P⁺-type diffused layers in an insulating layer 9 on each drain region 6, and is shown as a blank region inside the shaded drain region 6. An aluminium interconnection layer 8 (corresponding to the bit output line B_1 — B_3 , serves to connect together the drain regions 6 of the MISFETs of each column. The connection between the drain region 6 and the aluminium interconnection layer 8 is performed through the contact window 7. The pattern or writing of the ROM in the Figures is determined by the mask patterns used for the diffused source and drain layers 5, 6 and the contact windows 7.

As is shown by Figure 2A, the lateral type ROM has the disadvantage that the density of integration in the MIS large-scale integrated circuit (LSI) is low for two reasons. Firstly, the interconnection layers 4 for earthing the source regions of the MISFETs are required for each of the columns. Secondly, since contact windows 7 are formed on the drain regions 6 of each of the MISFETs, the drain regions 6 and

the aluminium interconnection layers 8 need to be of large area because of the possibility of mask misregistration.

By use of the present invention, it is possible to reduce the power dissipation in a ROM decoder in which the number of non-selected output lines is larger than the number of selected output lines, and to provide a ROM memory matrix which can be connected to the ROM decoder without an increase in number of components compared to the prior art.

It is also possible to provide a ROM which has reduced power dissipation without having corresponding lowering of the density of integration, and a construction and a driving method for the address decoder and the memory matrix, which are capable of raising the read-out speed for the memory matrix without causing a lowering of the memory matrix integration density.

According to the present invention there is provided a semiconductor read only memory comprising a memory matrix and a row selection matrix; said memory matrix comprising a plurality of series connection circuits being arrayed along a plurality of rows and each including a plurality of memory cells which are connected in series and are selectively arrayed along a plurality of columns and said rows, each of said memory cells having one transistor, said series connection circuits having a common output terminal and being connected in parallel between said common output terminal and another common terminal; said row selection matrix comprising in each row at least one transistor, connected in series with said transistors of said memory matrix, between said common output terminal and said other common terminal, said transistors of said row selection matrix being selectively arrayed along said rows and columns for selecting only one of said series circuits in order to form a conduction path between said common output terminal and said another common terminal by way of said at least one transistor.

The present invention will now be described in greater detail with reference to the remaining Figures of the accompanying drawings, in which:—

Figure 3 is a circuit diagram of a first form of memory matrix ROM and associated word address decoder;

Figure 4 is a circuit diagram of a second form of memory matrix and associated word address decoder;

Figure 5A is a circuit diagram of a third form of memory matrix and associated word address decoder;

Figure 5B is a series of waveforms

illustrating the discharge characteristics of the circuit shown in Figure 5A;

Figure 6A is a pattern diagram showing the circuit of the memory matrix ROM shown in Figure 3, constructed as an MISLSI chip;

Figure 7 is a circuit diagram of a first preferred form of semiconductor memory comprising a memory matrix and a row selection matrix; and

Figure 8 is a circuit diagram of a second embodiment of a semiconductor memory.

Referring first to Figure 3, the circuit includes a word address decoder ROM 11 and a memory matrix ROM 22. The word address decoder ROM 11 is constructed according to the "longitudinal system" as opposed to the "lateral system". In the word address decoder ROM 11, MISFETs of the enhancement type Q_1 to Q_8 are arrayed in any desired pattern in rows and columns. The MISFETs in each column are connected in series between one of several load depletion-type MISFETs Q_{L1} — Q_{L8} and earth. The MISFET gates of each row are connected to one of the address input lines A_1 , A_1 , A_2 and A_2 , each of which correspond to a particular row. A "ratio type" logic circuit consisting of each load MISFET and the plurality of MISFETs is formed, and one of the word address select lines W_1 — W_4 is connected to its output. The expression "ratio type" indicates a circuit whose output level is determined by the resistance ratio between the load MISFET and the driving MISFET. In such a longitudinal type ROM, all the MISFETs connected to unselected input lines turn "on" and the MISFETs connected to selected input lines turn "off", so that information as to whether or not MISFETs are connected to the selected input lines appears on the output lines.

The operation of the word address decoder ROM will now be illustrated by taking as an example the case when the word address select line W_1 is selected.

When an address signal of logic value "0" (supply voltage V_{DD}) is applied to the address input lines A_1 and A_2 , both the MISFETs Q_1 and Q_2 turn "on", so that a D.C. path is established for the load MISFET Q_{L1} . In the case of the other load MISFETs Q_{L2} to Q_{L8} , at least one of the MISFETs connected to the particular column turns "off", and no D.C. path is therefore established. As a result, only the word address select line W_1 is at earth, and thus this line is selected. For the longitudinal type address decoder ROM 11, even if the memory capacity of the ROM memory matrix increases, it is always the case that only one word address select line is chosen, and the number of unselected word address select lines only increases.

If the information contained in one column, or one word in the memory matrix ROM 2 of the prior art lateral system shown in Figure 1, is to be selected by the use of the longitudinal system word address decoder ROM 11 inverters must be incorporated into the word address select lines W_1 to W_4 , the reason being that in the case of the address decoder ROM 11, the selected word address select line is at earth potential, and the unselected word address select lines are at the supply voltage, whereas in the case of the memory matrix ROM 2 the selected word address select line is at the supply voltage and the unselected word address is at earth potential. Thus, if the memory matrix ROM 2 is decoded by the address decoder ROM 11, extra components are needed.

The memory matrix ROM 22 is constructed according to the longitudinal system, and obviates the above effect. In the memory matrix ROM 22, MISFETs of the enhancement type are formed at desired points in rows and columns. The MISFETs in each row are connected in series between one of several load depletion type MISFETs Q_{L9} to Q_{L11} and earth. Each row of MISFET gates is connected to one of the word address select lines W_1 to W_4 . To one end of each of the load MISFETs Q_{L9} to Q_{L11} is connected one of the bit output lines B_1 to B_3 . Any portion of each row at which no MISFET exists is made into a short circuit by extending the P⁺-region.

In the memory matrix ROM 22, all the MISFETs connected to non-selected word address select lines turn "on", so that information as to whether or not MISFETs are connected to the selected word address select line appears on the bit output lines B_1 to B_3 . As an example, consider the case in which the fixed stored contents of the column selected by the word address line W_1 are read out.

When the earth potential on the selected word address select line W_1 and the supply voltage on the non-selected word address select lines W_2 to W_4 are applied, the MISFET Q_{13} turns "off" and the MISFETs Q_9 to Q_{12} and Q_{14} turn "on". Thus, for the load MISFET Q_{L9} , a D.C. path is established because no MISFET exists in the selected column, and the MISFET Q_9 and Q_{10} are "on". For the load MISFET Q_{L10} , a D.C. path is established because no MISFET exists in the selected column, and the MISFETs Q_{11} and Q_{12} are "on". For the load MISFET Q_{L11} , a D.C. path is not established because the MISFET Q_{13} , which exists in the selected column, is "off". In consequence, both the bit output line B_1 and the bit output line B_2 are earthed, and the supply voltage appears on

the bit output line B_3 , so that fixed stored contents is transferred to the output lines.

As set forth above, in the case of the memory matrix ROM 22, the selected word address select line is at earth potential and the unselected word address select lines are at the supply voltage. Thus, it may be connected to the word address decoder ROM 11 without the necessity of interposing inverters.

Referring now to Figure 4, there is shown a circuit arrangement in which a ratioless type memory matrix ROM 23 is provided in order to improve on the memory matrix ROM 22 of Figure 3, with regard to density of integration and power dissipation. The expression "ratioless type" indicates a circuit whose output potential is not determined by the resistance ratio between the load MISFET and the driving MISFET. As shown, precharging MISFETs Q_{P1} — Q_{P3} are driven by clock pulses ϕ_1 illustrated in Figure 5B. Capacitors C_1 to C_3 are, in fact, P-N junctions. Sampling MISFETs Q_{S1} — Q_{S3} are driven by clock pulses ϕ_2 illustrated in Figure 5B, and transfer gate MISFETs Q_{T1} to Q_{T3} are driven by the clock pulses ϕ_2 . The output is taken from the points O_1 to O_3 .

During a clock pulse ϕ_1 , charges are supplied from a power source through the precharging MISFETs to the capacitors C_1 to C_3 . Subsequently, during a clock pulse ϕ_2 , and address signal is applied to the word address decoder ROM 11 through the transfer MISFETs Q_{T1} to Q_{T3} . The chosen word address select line is then selected immediately because the word address decoder ROM 11 is built of the ratio type. The MISFET of the column selected by the word address decoder ROM 11 turns "off", whereas the MISFETs of the columns not selected turn "on". During the clock pulse ϕ_2 , the sampling MISFETs Q_{S1} to Q_{S3} also turn "on". Thus, in the case of a row in which there is no MISFET in the selected column, the charge on the capacitor connected to that particular row is discharged through the sampling MISFET, whereas for a row in which there is a MISFET in the selected column, the charge on the capacitor connected to that particular row are not discharged. The voltages on the capacitors C_1 to C_3 are read out through the transfer gate MISFETs Q_{T3} to Q_{T1} respectively at the output terminals O_1 to O_3 , and show the fixed stored content of the selected column.

The embodiment shown in Figure 4 possesses two main advantages. Firstly, since the output on any given output line is determined by whether the corresponding capacitor is discharged or not, it is practically unnecessary to consider the g_m (mutual conductance) ratio between the

precharging MISFETs and the MISFETs connected thereto. Thus, the g_m between the sampling MISFETs and the MISFETs connected thereto can be made small, and accordingly, the area occupied by the MISFETs can be made small, with the result that the integration density of the memory matrix ROM 23 is increased. Secondly, because the clock pulses ϕ_1 and ϕ_2 are completely different in phase, the precharging MISFETs and the sampling MISFETs can never turn "on" at the same time, so that no D.C. path is established between the power source (V_{DD}) and earth. Consequently, power dissipation in the memory matrix 23 is greatly reduced.

On the other hand, the read-out speed of the memory matrix ROM 23 shown in Figure 4 can be improved upon, because charges accumulated on the capacitors C_1 to C_3 by a clock pulse ϕ_1 are not discharged until a clock pulse ϕ_2 is applied, and because since the time constant determined by the total "on" resistance of the plurality of MISFETs arrayed in each row and by the capacity of the capacitor is large, the discharging time is long. In other words, the width of the clock pulse ϕ_2 needs to be large.

Referring now to Figure 5A, the circuit shown includes a ratio type longitudinal word address decoder ROM 11 and a ratioless type longitudinal memory matrix ROM 24 with the sampling MISFETs removed, on which an address signal is applied by the clock pulse ϕ_1 in order to shorten the discharging time, etc. of the memory matrix ROM 23 in Figure 4, and to thus raise the read-out speed. The operation of the memory matrix ROM 24 will now be described in the case when the word address select line W_1 is selected (zero volts) and the lines W_2 to W_4 are unselected ($-V_{DD}$).

First, the clock pulse ϕ_1 becomes negative and the precharging MISFETs Q_{P1} — Q_{P3} turn "on". Then, the MISFET Q_{11} is "off". On the other hand, the capacitors C_1 and C_2 are charged only to the values obtained by multiplying the supply voltage V_{DD} by the ratios between the mutual conductances of the precharging MISFETs Q_{P1} and Q_{P2} , and those of the data input MISFETs Q_9 , Q_{10} and Q_{11} , Q_{12} , because all the MISFETs connected in series with the respective output lines are "on". Subsequently, when the clock pulse ϕ_1 goes to earth potential, the charge stored on the capacitors C_1 and C_2 begins to discharge at once. The potentials of the respective output lines then go to earth potential. In contrast, the charges stored on the capacitor C_3 are not discharged, since the MISFET Q_{11} is still "off", and the potential of the output line is maintained substantially at the potential

V_{DD} . Subsequently, when the clock pulse ϕ_2 becomes negative, the transfer gate MISFETs Q_{T1} — Q_{T3} turn "on", and the potentials of the output lines are 0 (zero volts), 0 (zero volts) and V_{DD} at the output terminals O_1 , O_2 and O_3 , respectively.

Figure 5B shows the operational waveforms for the memory matrix ROM 24 in Figure 5A. In Figure 5B, ϕ_1 and ϕ_2 denote the clock pulses, which differ in phase from each other. The voltages on the word address select lines W_1 to W_4 are indicated by V_{W1} to V_{W4} , and the voltages on capacitors C_1 to C_3 by V_{N1} to V_{N3} . V_{O1} to V_{O3} show the state of the output terminals O_1 to O_3 .

The periods t_1 , t_2 , t_3 , and t_4 of the operational waveforms for V_{W1} to V_{W4} , V_{N1} to V_{N3} to V_{O1} to V_{O3} correspond to the reading of the fixed store contents of the columns selected by the word address select lines W_1 , W_2 , W_3 and W_4 respectively.

As is apparent from the above description, the memory matrix ROM 24 of Figure 5A has an improved discharge operation and a correspondingly faster read-out speed compared with the embodiment in Figure 4, because, since the sampling MISFETs are removed, the number of the MISFETs connected to each output line decreases by one. Consequently, the discharge time constants for the capacitors C_1 to C_3 diminish, and the discharging periods shorten. Also, the capacitors which are to be discharged to earth are charged, when the clock pulse ϕ_1 becomes negative, to a voltage of smaller magnitude than the supply voltage V_{DD} . Therefore, the discharging period of time becomes shorter. When the clock pulse ϕ_1 reaches earth potential, the point of time at which the charges stored in the capacitors C_1 to C_3 begin to be discharged is advanced.

Figure 6A shows a pattern diagram for the memory matrix portion 22 shown in Figure 3 assembled as a single semiconductor chip. Figure 6B is a sectional view taken along A—A' of Figure 6A. In Figure 6A, the information stored in the longitudinal type ROM is formed as the presence or absence of a buried region underneath each silicon gate layer. If a buried region exists underneath a silicon gate layer, then there is simply an interconnection, and practically no MISFET exists, whereas if a buried region does not exist underneath the silicon gate layer, then a MISFET is formed with isolated source and drain regions.

In Figure 6A, silicon gate layer 9 (corresponding to the word address select lines) form the gate portions of the MISFETs and connect the gates of each column. The buried regions 10 are formed by P⁺-

diffusion at the points at which mere interconnection is desired without a MISFET. Since the buried regions 10 lie directly under the silicon gates, they are formed before forming the silicon gate layer 9. A P⁺-interconnection layer forms the drain regions and source regions of the MISFETs, and which is used to connect in series the MISFETs in each row. Where no buried regions 10 are formed directly under the silicon gate layers 9, gate portions of corresponding MISFETs are produced.

The assembly of a longitudinal type ROM in MISLSI form, possesses a number of advantages. In order to write the ROM pattern in each row, the MISFETs may be connected in series by the P⁺-interconnection portion. It is not necessary to form contact windows for the connection of the word address select lines to the respective drain regions, as is required in the case of a lateral ROM. It is consequently unnecessary to provide contact regions in the drain regions, so that the area occupied can be made small. Also, an earth interconnection layer need not be provided for each column, as is required in the case of the lateral ROM, only one being necessary. (refer to Figure 5). A further advantage of the longitudinal type ROM is that the MISFETs are formed by interconnection of the silicon gate layer and the P⁺-interconnection layer, and so an aluminium interconnection layer can be formed on the longitudinal type ROM-forming area as a third layer. In the case where, as in the lateral type ROM, the MISFETs are formed from the three layers consisting of the silicon gate layer, the P⁺-interconnection layer, and the aluminium interconnection layer serving as the output line, it is difficult to form a further interconnection portion on the ROM-forming area, and it has been necessary to provide a special area for the interconnection portion outside the ROM-forming area.

The above circuits shown in the drawings are constructed of enhancement mode FETs, but the invention may be applied using other types of gated transistor.

In the first embodiment of a semiconductor memory comprising a memory matrix and a row selection matrix as shown in Figure 7, in order that any desired row of the memory matrix ROM may also be selectable, a memory matrix ROM portion 25 and the word address decoder ROM 11 are additionally provided with a bit address decoder ROM 26 and a bit selection ROM portion 27.

The bit selection ROM portion 27 is a gate circuit for selecting one of the bit output lines B₁ to B₃, and it is formed by a longitudinal ROM integral with the

memory matrix ROM portion 25. The bit address decoder ROM 26 controls the bit selection ROM portion 27.

The operation of the bit selection ROM portion 27 will now be illustrated by taking the selection of the bit output line B₁ as an example.

When a bit address select line Y₁ is selected by the bit select ROM portion 27 turn "OFF". MISFETs Q₂₁ and Q₂₂ are respectively connected with bit address select lines Y₂ and Y₃, and turn "on" because the supply voltage is applied to them. The bit output line B₁ is connected to one terminal of the capacitor C₄ since the MISFETs Q₂₁ and Q₂₂ turn "on", whereas the bit output line B₂ and B₃ are not connected to the one end of the capacitor C₄ since the MISFETs Q₂₃ and Q₂₅ are "off". In this manner, the predetermined address of the memory matrix ROM portion 25 can be selected by the word address decoder ROM and the bit address decoder ROM.

In the second embodiment, as illustrated in Figure 8, the bit address decoder ROM is a lateral type ROM in which a single MISFET is arrayed in each row of the bit selection ROM portion. The bit select ROM portion 27' has a MISFET Q₃₁ arranged at the intersection of the bit address select line Y₁ and the bit output line B₁, a MISFET Q₃₄ arranged at the intersection of the bit address select line Y₂ and the bit output line B₂, and a MISFET Q₃₃ arranged at the intersection of the bit address select line Y₃ and a bit output line B₃. As a result of this form of construction, only the bit select line which has a MISFET at its point of intersection with the bit address select line selected by the bit address decoder ROM 26' is connected to the capacitor C₄.

In the embodiment of Figure 8, a single MISFET is arrayed in each row of the bit select ROM, and hence, where the memory matrix portion and the bit select portion are formed by an integral longitudinal ROM, the discharge characteristics is good.

WHAT WE CLAIM IS:—

1. A semiconductor read only memory comprising a memory matrix and a row selection matrix; said memory matrix comprising a plurality of series connection circuits being arrayed along a plurality of rows and each including a plurality of memory cells which are connected in series and are selectively arrayed along a plurality of columns and said rows, each of said memory cells having one transistor, said series connection circuits having a common output terminal and being connected in parallel between said common output terminal and another common terminal; said row selection



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diffusion at the points at which mere interconnection is desired without a MISFET. Since the buried regions 10 lie directly under the silicon gates, they are formed before forming the silicon gate layer 9. A P⁺-interconnection layer forms the drain regions and source regions of the MISFETs, and which is used to connect in series the MISFETs in each row. Where no buried regions 10 are formed directly under the silicon gate layers 9, gate portions of corresponding MISFETs are produced.

The assembly of a longitudinal type ROM in MISLSI form, possesses a number of advantages. In order to write the ROM pattern in each row, the MISFETs may be connected in series by the P⁺-interconnection portion. It is not necessary to form contact windows for the connection of the word address select lines to the respective drain regions, as is required in the case of a lateral ROM. It is consequently unnecessary to provide contact regions in the drain regions, so that the area occupied can be made small. Also, an earth interconnection layer need not be provided for each column, as is required in the case of the lateral ROM, only one being necessary. (refer to Figure 5). A further advantage of the longitudinal type ROM is that the MISFETs are formed by interconnection of the silicon gate layer and the P⁺-interconnection layer, and so an aluminium interconnection layer can be formed on the longitudinal type ROM-forming area as a third layer. In the case where, as in the lateral type ROM, the MISFETs are formed from the three layers consisting of the silicon gate layer, the P⁺-interconnection layer, and the aluminium interconnection layer serving as the output line, it is difficult to form a further interconnection portion on the ROM-forming area, and it has been necessary to provide a special area for the interconnection portion outside the ROM-forming area.

The above circuits shown in the drawings are constructed of enhancement mode FETs, but the invention may be applied using other types of gated transistor.

In the first embodiment of a semiconductor memory comprising a memory matrix and a row selection matrix as shown in Figure 7, in order that any desired row of the memory matrix ROM may also be selectable, a memory matrix ROM portion 25 and the word address decoder ROM 11 are additionally provided with a bit address decoder ROM 26 and a bit selection ROM portion 27.

The bit selection ROM portion 27 is a gate circuit for selecting one of the bit output lines B₁ to B_n, and it is formed by a longitudinal ROM integral with the

memory matrix ROM portion 25. The bit address decoder ROM 26 controls the bit selection ROM portion 27.

The operation of the bit selection ROM portion 27 will now be illustrated by taking the selection of the bit output line B₁ as an example.

When a bit address select line Y₁ is selected by the bit select ROM portion 27 turn "OFF". MISFETs Q₂₁ and Q₂₂ are respectively connected with bit address select lines Y₂ and Y₃, and turn "on" because the supply voltage is applied to them. The bit output line B₁ is connected to one terminal of the capacitor C₄ since the MISFETs Q₂₁ and Q₂₂ turn "on", whereas the bit output line B₂ and B₃ are not connected to the one end of the capacitor C₄ since the MISFETs Q₂₃ and Q₂₃ are "off". In this manner, the predetermined address of the memory matrix ROM portion 25 can be selected by the word address decoder ROM and the bit address decoder ROM.

In the second embodiment, as illustrated in Figure 8, the bit address decoder ROM is a lateral type ROM in which a single MISFET is arrayed in each row of the bit selection ROM portion. The bit select ROM portion 27' has a MISFET Q₃₃ arranged at the intersection of the bit address select line Y₁ and the bit output line B₁, a MISFET Q₃₄ arranged at the intersection of the bit address select line Y₂ and the bit output line B₂, and a MISFET Q₃₅ arranged at the intersection of the bit address select line Y₃ and a bit output line B₃. As a result of this form of construction, only the bit select line which has a MISFET at its point of intersection with the bit address select line selected by the bit address decoder ROM 26' is connected to the capacitor C₄.

In the embodiment of Figure 8, a single MISFET is arrayed in each row of the bit select ROM, and hence, where the memory matrix portion and the bit select portion are formed by an integral longitudinal ROM, the discharge characteristics is good.

WHAT WE CLAIM IS:—

1. A semiconductor read only memory comprising a memory matrix and a row selection matrix; said memory matrix comprising a plurality of series connection circuits being arrayed along a plurality of rows and each including a plurality of memory cells which are connected in series and are selectively arrayed along a plurality of columns and said rows, each of said memory cells having one transistor, said series connection circuits having a common output terminal and being connected in parallel between said common output terminal and another common terminal; said row selection

(12)

5 matrix comprising in each row at least one transistor, connected in series with said transistors of said memory matrix, between said common output terminal and said other common terminal, said transistors of said row selection matrix being selectively arrayed along said rows and columns for selecting only one of said series circuits in order to form a conduction path between said common output terminal and said another common terminal by way of said at least one transistor.

15 2. A semiconductor memory according to claim 1, including an address decoder having a plurality of sets of true and complementary address inputs and including a first decoder matrix and a second decoder matrix each comprising a plurality of outputs and a plurality of transistors selectively arrayed along said plurality of rows and columns, one of said decoder matrices being responsive to different sets of said address inputs from the other, each output in each column of said second decoder matrix being supplied to the transistors in the same column of said selection matrix and each of said outputs in each column of said first decoder matrix being supplied to the transistors in the same column of said memory matrix.

25 3. A semiconductor memory according to claim 2, wherein in each of said decoder matrices the transistors in each column are connected in series.

30 4. A semiconductor memory according

to claim 2 or 3, wherein said transistors are all MISFETs, said decoder matrices each being operative in a ratio mode that output level thereof depends on a ratio between a load transistor and driving transistors, and said memory matrix and said row selection matrix being operative in a ratioless mode that the output level thereof does not depend on a ratio between a load transistor and driving transistors. 40

5. A semiconductor memory according to claim 4, wherein said load transistors are depletion mode MISFETs in which the gate and source electrodes are directly interconnected for each MISFET. 45

6. A semiconductor memory according to any one of the preceding claims 2 to 5, wherein in said first decoder matrix, said transistors in each column are connected in series, and in said second decoder matrix, said transistors in each column are connected in parallel. 50

7. A semiconductor read only memory comprising a memory matrix and a row selection matrix constructed substantially as herein described with reference to and as illustrated in Figure 7 or Figure 8 of the accompanying drawings. 55

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Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.



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