Claims:

1. A microelectronic package comprising:

a package substrate;

an active die; and

a memory die communicatively coupled with the package substrate and the active die, wherein the memory die includes:

a first memory cell at a first n-type metal-oxide-semiconductor (NMOS) layer of the memory die;

a second memory cell at a second NMOS layer of the memory die;

a complementary metal-oxide semiconductor (CMOS) layer comprising control logic for the memory die; and

a via in the memory die that communicatively couples the active die with the package substrate.

2. The microelectronic package of claim 1, wherein the memory die is between the package substrate and the active die.

3. The microelectronic package of claim 1, wherein an active side of the memory die is coupled with an active side of the active die by an interconnect.

4. The microelectronic package of claim 1, wherein the memory die has a z-height between 100 micrometers (“microns”) and 150 microns as measured perpendicularly to a face of the package substrate.

5. The microelectronic package of claim 1, wherein the memory die has a memory capacity between 4 gigabytes (GB) and 16 GB.

6. The microelectronic package of claim 1, wherein the active die and the memory die are communicatively coupled with the package substrate by an interconnect that is different than a wirebond.

7. The microelectronic package of claim 1, wherein the memory die further includes a third memory cell at a first layer of the memory die.

8. The microelectronic package of claim 1, wherein the first memory cell is a dynamic random-access memory (DRAM) cell that includes an n-type metal-oxide-semiconductor field-effect transistor (MOSFET).

9. The microelectronic package of claim 8, wherein the n-type MOSFET is coupled with a wordline of the memory die, a bitline of the memory die, and a bias voltage of the memory die.

10. An electronic device comprising:

an antenna to facilitate wireless communication between the electronic device and another electronic device; and

a microelectronic package communicatively coupled with the antenna, wherein the microelectronic package includes:

a memory die communicatively coupled with a package substrate of the electronic device, wherein the memory die includes:

a first memory cell at a first n-type metal-oxide-semiconductor (NMOS) layer of the memory die;

a second memory cell at a second NMOS layer of the memory die; and

a complementary metal-oxide semiconductor (CMOS) layer comprising control logic for the memory die; and

a system-on-chip (SOC) communicatively coupled with the package substrate of the electronic device by a conductive element in the memory die.

11. The electronic device of claim 10, wherein the memory die has a z-height of less than 150 micrometers (“microns”) as measured perpendicularly to a face of the package substrate.

12. The electronic device of claim 10, wherein the memory die has a memory capacity between 4 gigabytes (GB) and 16 GB.

13. The electronic device of claim 10, wherein the first memory cell is a dynamic random-access memory (DRAM) cell that includes an n-type metal-oxide-semiconductor field-effect transistor (MOSFET).

14. The electronic device of claim 10, wherein the memory die is between the SOC and the package substrate.

15. The electronic device of claim 10, wherein the SOC is communicatively coupled with the package substrate by an interconnect that is different than a wirebond.

16. A microelectronic package comprising:

a memory die communicatively coupled with a package substrate of the electronic device, wherein the memory die includes:

a first memory cell at a n-type metal-oxide-semiconductor (NMOS) first layer of the memory die, wherein the first memory cell includes a first a dynamic random-access memory (DRAM) cell with an n-type metal-oxide-semiconductor field-effect transistor (MOSFET);

a second memory cell at a second NMOS layer of the memory die, wherein the second memory cell includes a second DRAM cell with an n-type MOSFET; and

complementary metal-oxide semiconductor (CMOS) layer comprising control logic for the memory die; and

a conductive element; and

a system-on-chip (SOC) communicatively coupled with the package substrate of the microelectronic package by the conductive element in the memory die.

17. The microelectronic package of claim 16, wherein the memory die has a z-height of less than 100 micrometers (“microns”) as measured perpendicularly to a face of the package substrate.

18. The microelectronic package of claim 16, wherein the memory die has a memory capacity between 4 gigabytes (GB) and 16 GB.

19. The microelectronic package of claim 16, wherein the n-type MOSFET of the first memory cell is coupled with a wordline of the memory die, a bitline of the memory die, and a bias voltage of the memory die.