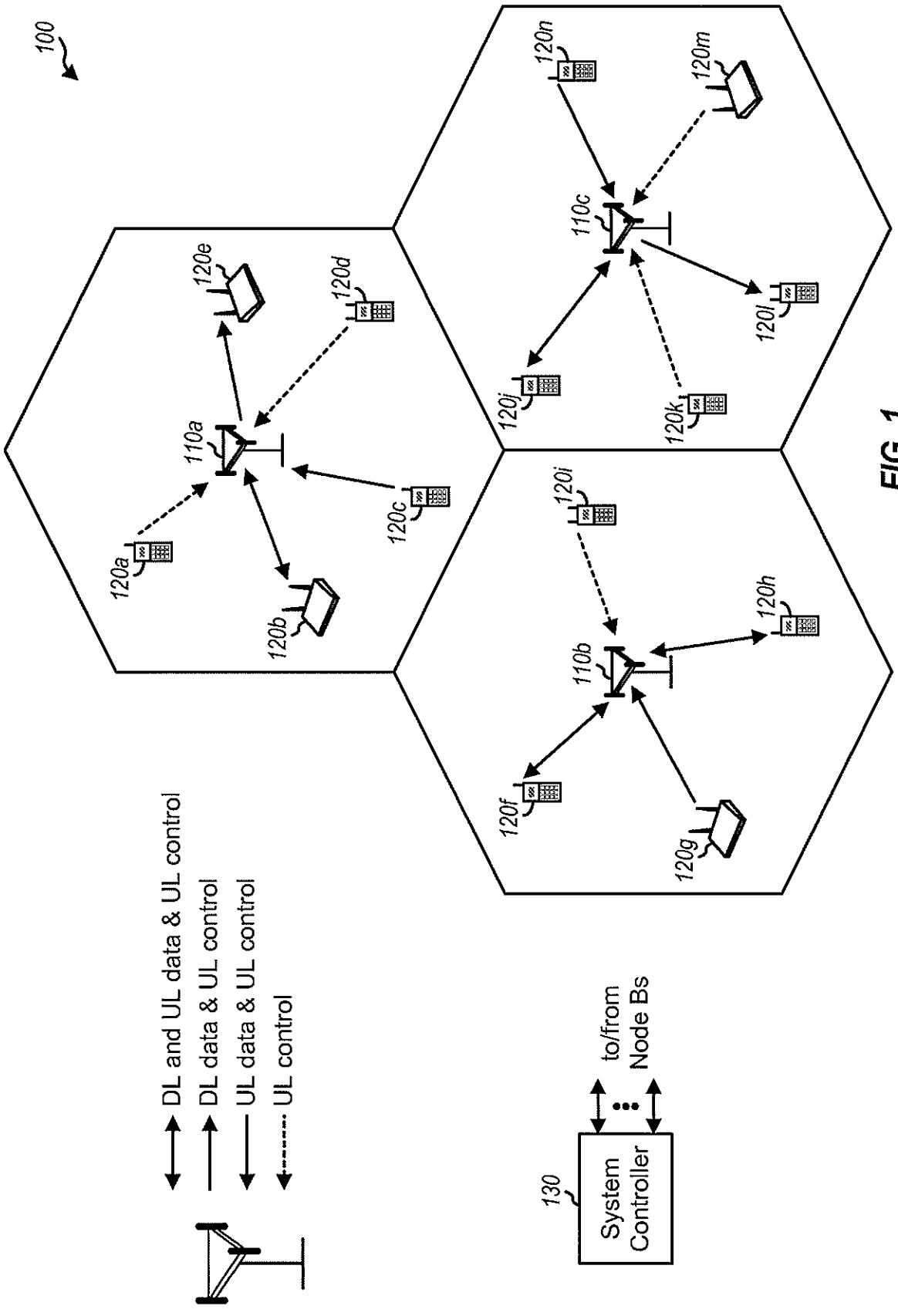

100
110a
110b
110c
120a
120b
120c
120d
120e
120f
120g
120h
120i
120j
120k
120l
120m
120n
DL and UL data & UL control
DL data & UL control
UL data & UL control
UL control
130
System Controller
to/from Node Bs

FIG. 1

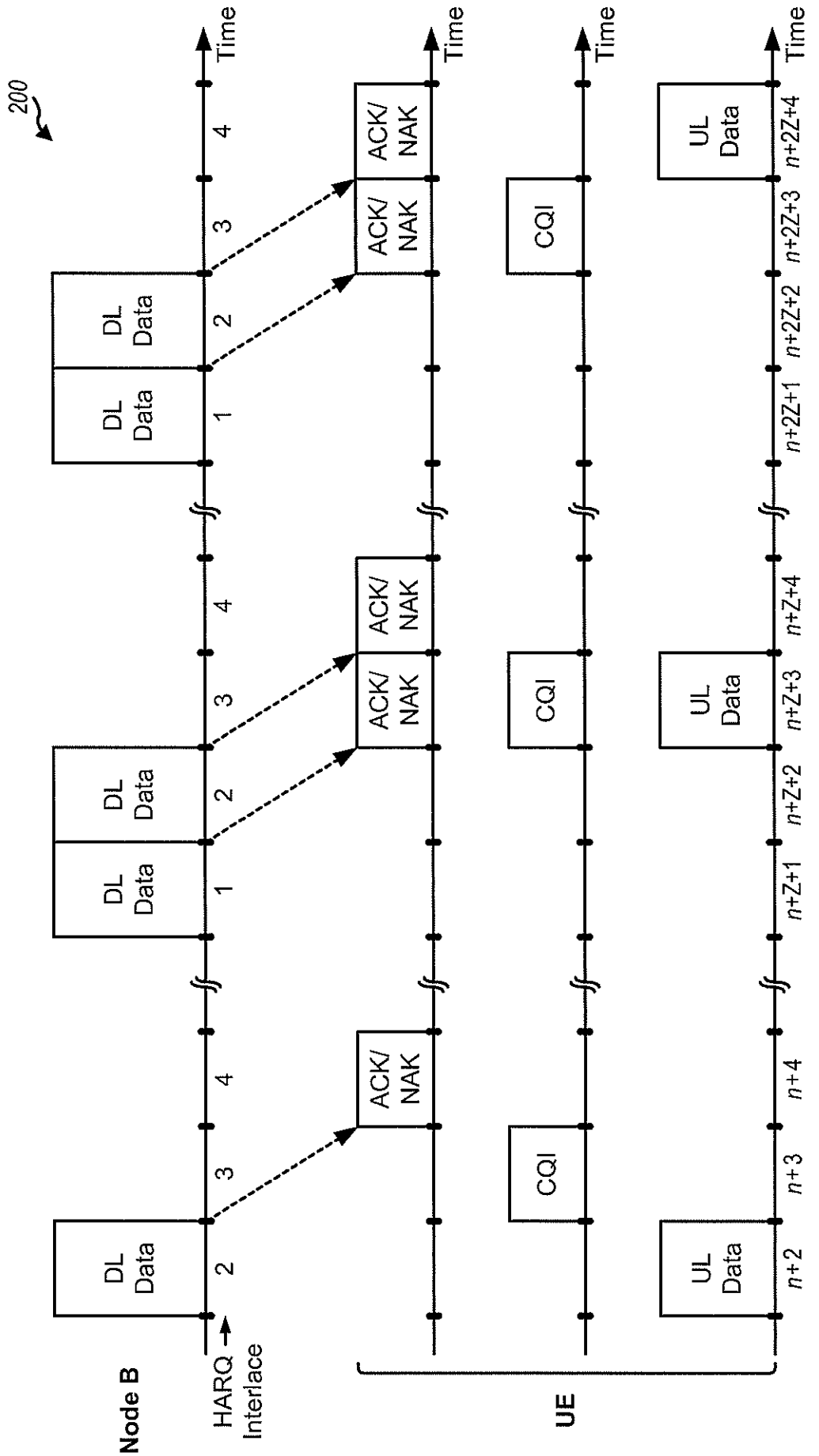

200
Node B
HARQ Interlace
UE
Time
DL Data
ACK/ NAK
CQI
UL Data
1
2
3
4
n+2
n+3
n+4
n+Z+1
n+Z+2
n+Z+3
n+Z+4
n+2Z+1
n+2Z+2
n+2Z+3
n+2Z+4

FIG. 2

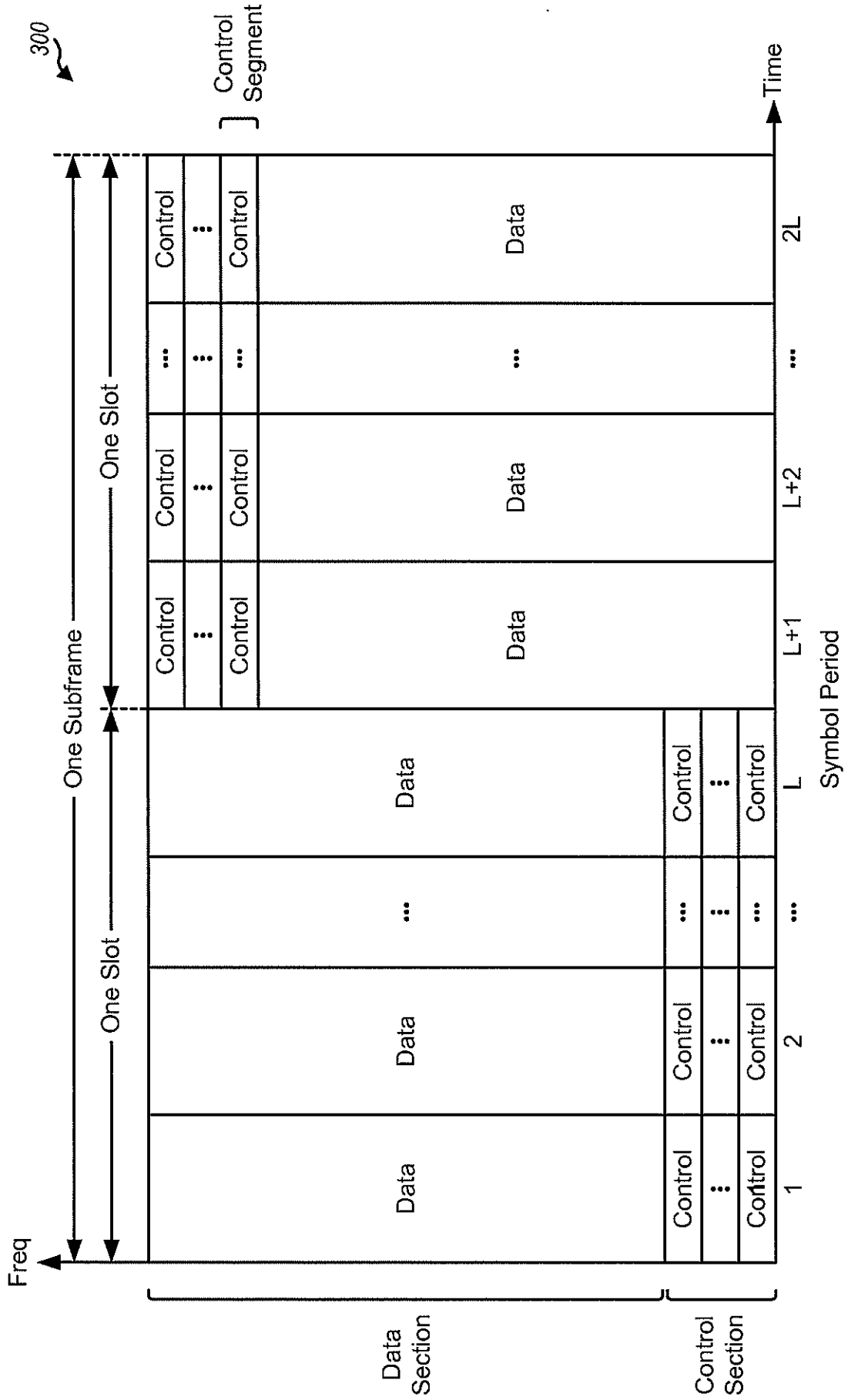

300
Control Segment
Time
One Subframe
One Slot
One Slot
Freq
Control
Data
1
2
...
L
L+1
L+2
...
2L
Symbol Period
Data Section
Control Section

FIG. 3

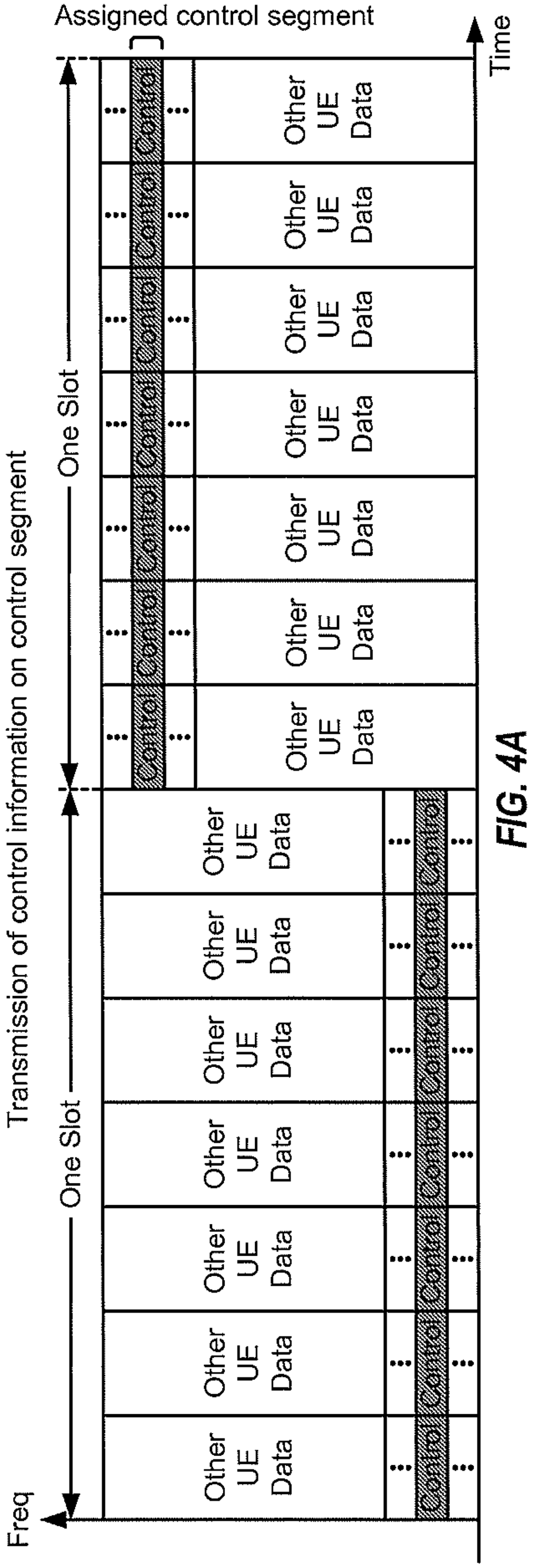

Transmission of control information on control segment
Assigned control segment
One Slot
One Slot
Freq
Time
Other UE Data
Control
...

FIG. 4A

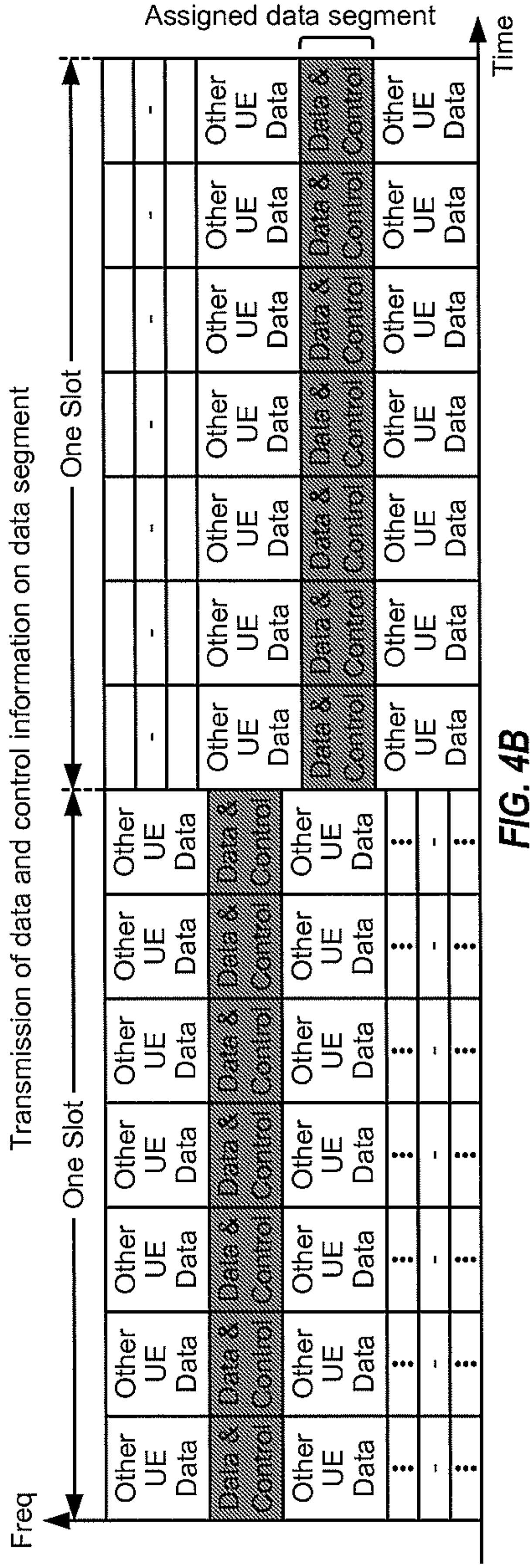

Transmission of data and control information on data segment
Assigned data segment
One Slot
One Slot
Freq
Time
Other UE Data
Data & Control
...

FIG. 4B

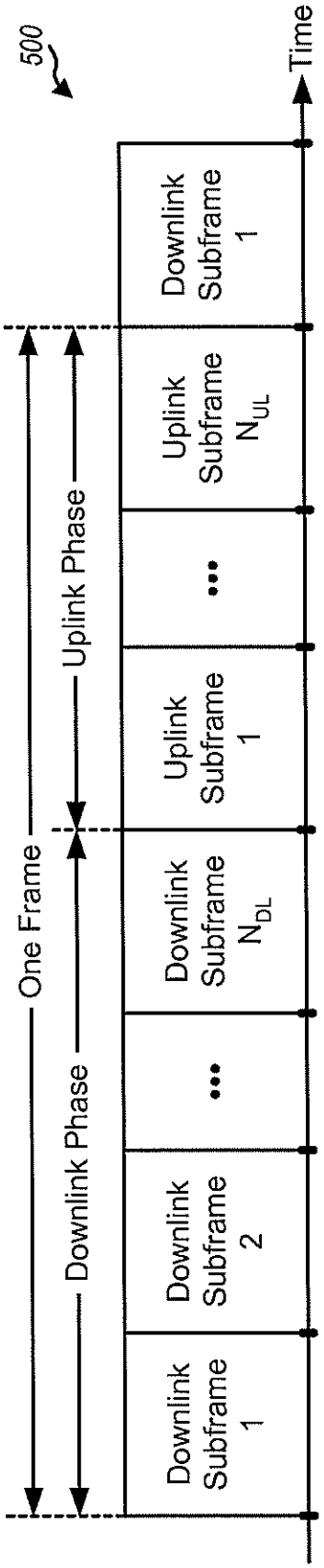

500
Time
One Frame
Downlink Phase
Uplink Phase
Downlink Subframe 1
Downlink Subframe 2
Downlink Subframe N_{DL}
Uplink Subframe 1
Uplink Subframe N_{UL}

FIG. 5

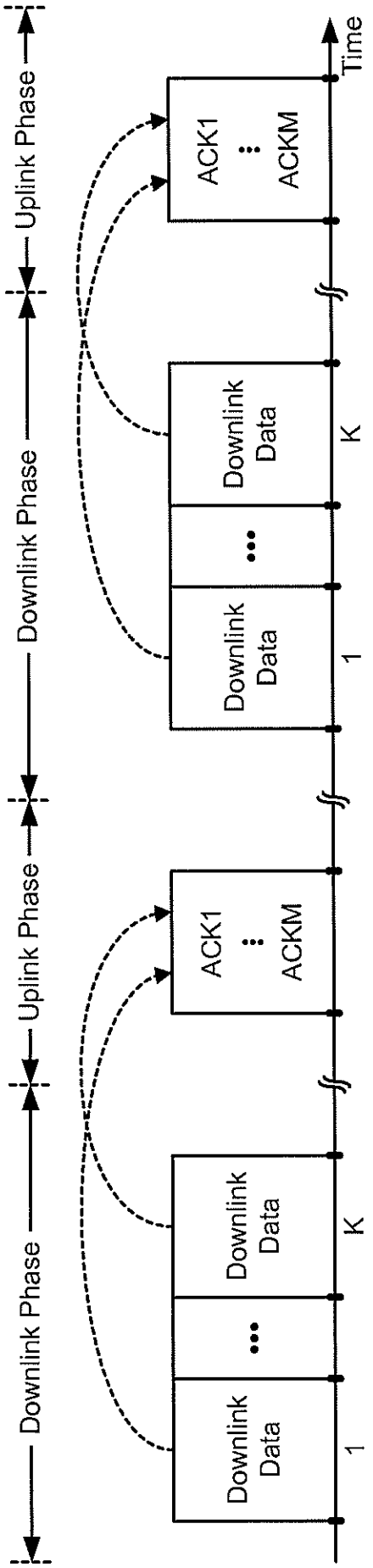

Time
Downlink Phase
Uplink Phase
Downlink Phase
Uplink Phase
Downlink Phase
Downlink Data
Downlink Data
Downlink Data
Downlink Data
ACK1
ACKM
ACK1
ACKM
1
K
1
K

FIG. 6

Sending only ACK Information on Control Segment

ACK Information for One HARQ Process

712

	Slot T1	Slot T2
VFR S1	ACK1	ACK1
VFR S2	ACK1	ACK1

ACK Information for Two HARQ Processes

714

	Slot T1	Slot T2
VFR S1	ACK1	ACK1
VFR S2	ACK2	ACK2

ACK Information for Three HARQ Processes

716

	Slot T1	Slot T2
VFR S1	ACK1	ACK3
VFR S2	ACK2	ACK 1/2/3

FIG. 7A

Sending CQI & ACK Information on Control Segment

CQI Information Only

720

	Slot T1	Slot T2
VFR S1	CQI	CQI
VFR S2	CQI	CQI

CQI & ACK Information for One HARQ Process

722

	Slot T1	Slot T2
VFR S1	CQI	CQI
VFR S2	ACK1	ACK1

CQI & ACK Information for Two HARQ Processes

724

	Slot T1	Slot T2
VFR S1	CQI	CQI
VFR S2	ACK1	ACK2

CQI & ACK Information for Three HARQ Processes

726

	Slot T1	Slot T2
VFR S1	CQI	ACK2
VFR S2	ACK1	ACK3

FIG. 7B

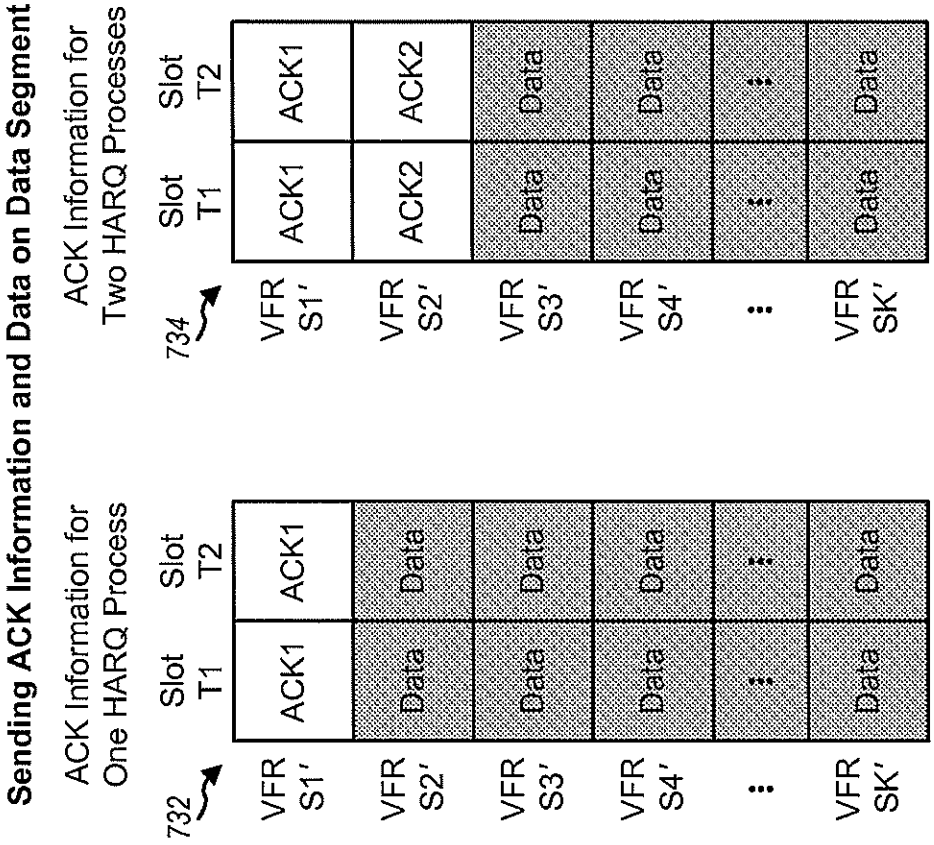

Sending ACK Information and Data on Data Segment
ACK Information for One HARQ Process
ACK Information for Two HARQ Processes
ACK Information for Three HARQ Processes
732
734
736
Slot T1
Slot T2
VFR S1'
VFR S2'
VFR S3'
VFR S4'
VFR SK'
ACK1
ACK2
ACK3
Data

FIG. 7C

Sending CQI & ACK Information & Data on Data Segment

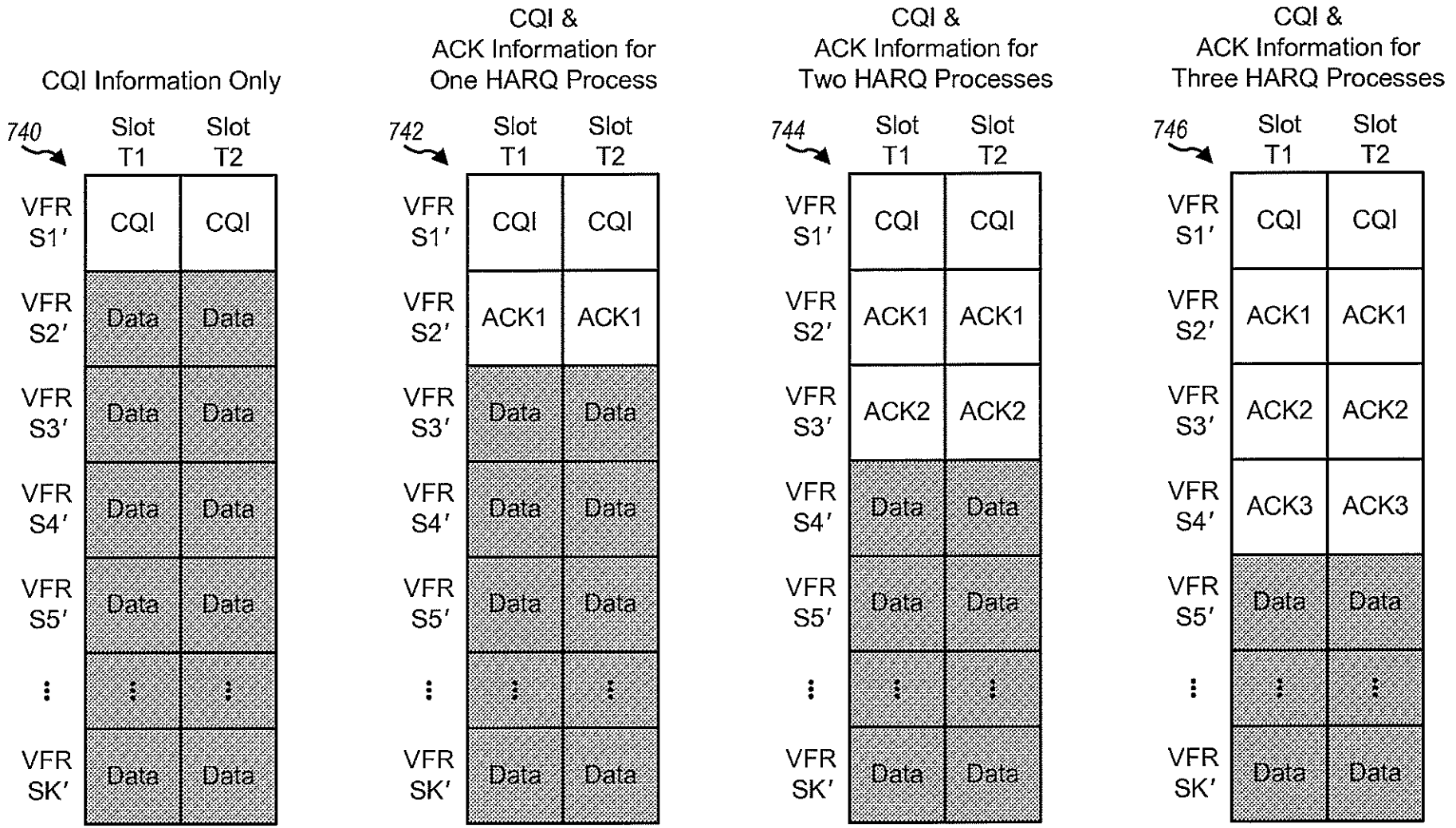


FIG. 7D

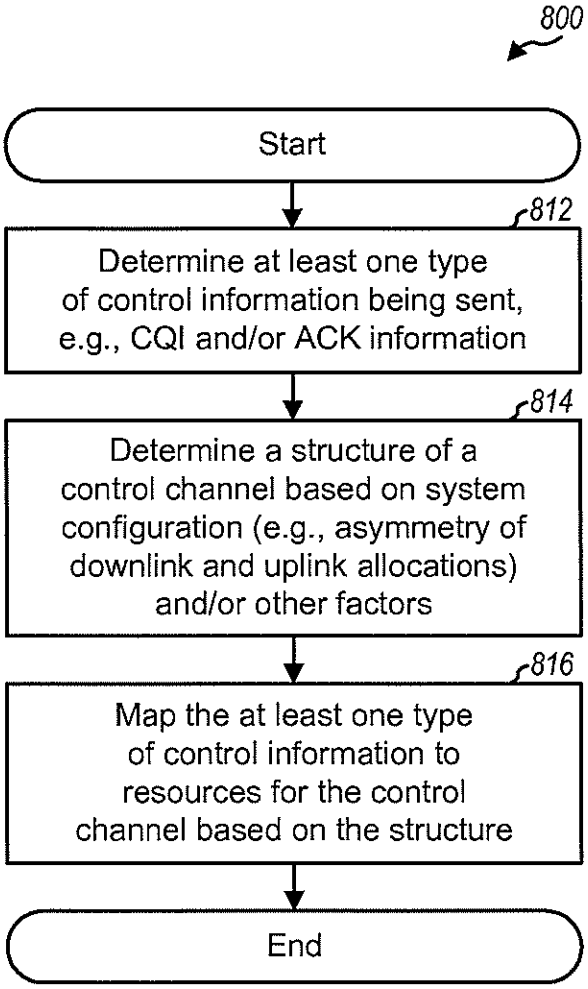

800
Start
812
Determine at least one type of control information being sent, e.g., CQI and/or ACK information
814
Determine a structure of a control channel based on system configuration (e.g., asymmetry of downlink and uplink allocations) and/or other factors
816
Map the at least one type of control information to resources for the control channel based on the structure
End

FIG. 8

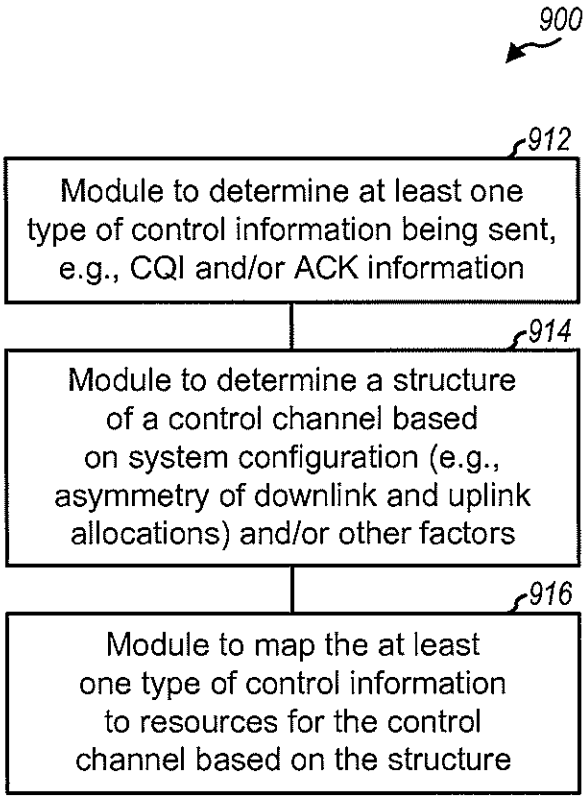

900
912
Module to determine at least one type of control information being sent, e.g., CQI and/or ACK information
914
Module to determine a structure of a control channel based on system configuration (e.g., asymmetry of downlink and uplink allocations) and/or other factors
916
Module to map the at least one type of control information to resources for the control channel based on the structure

FIG. 9

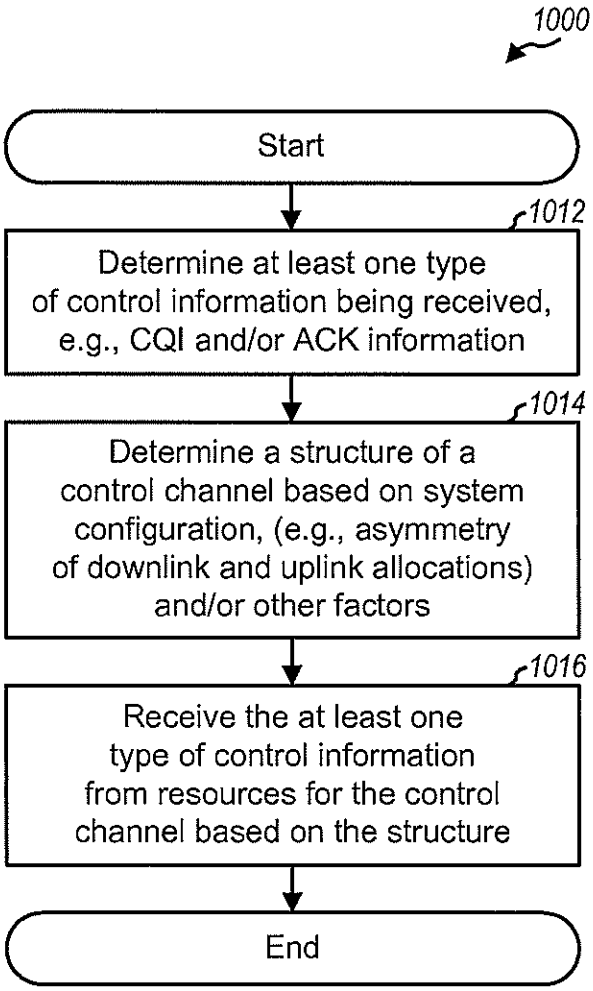

1000
Start
1012
Determine at least one type of control information being received, e.g., CQI and/or ACK information
1014
Determine a structure of a control channel based on system configuration, (e.g., asymmetry of downlink and uplink allocations) and/or other factors
1016
Receive the at least one type of control information from resources for the control channel based on the structure
End

FIG. 10

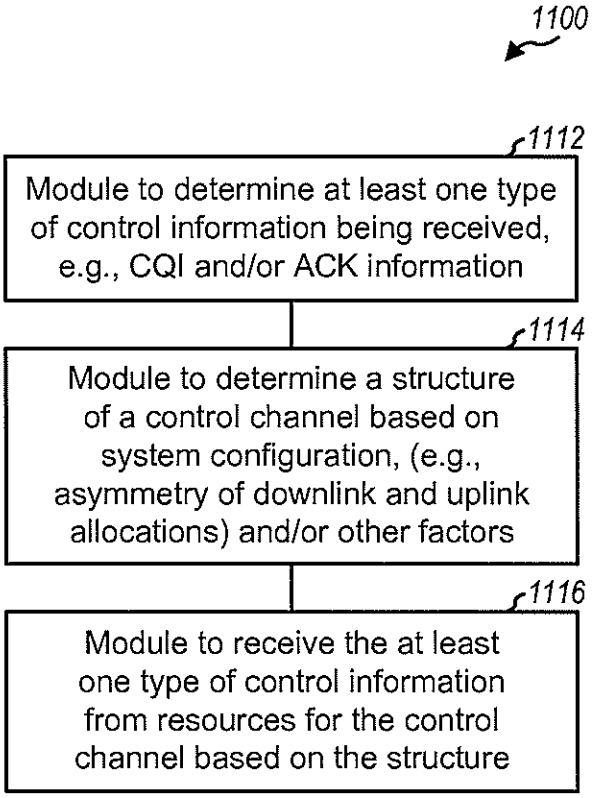

1100
1112
Module to determine at least one type of control information being received, e.g., CQI and/or ACK information
1114
Module to determine a structure of a control channel based on system configuration, (e.g., asymmetry of downlink and uplink allocations) and/or other factors
1116
Module to receive the at least one type of control information from resources for the control channel based on the structure

FIG. 11

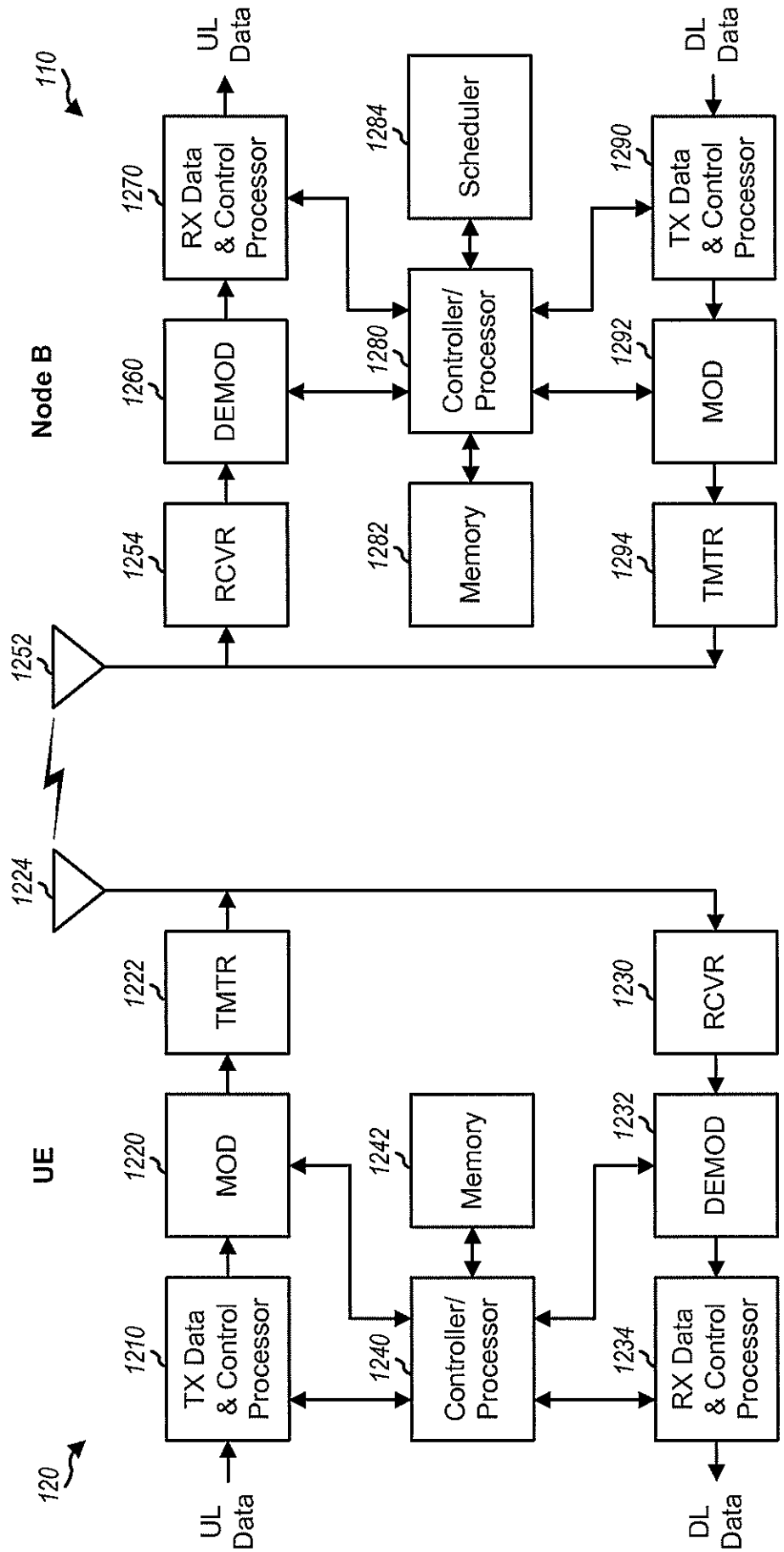

110
Node B
UL Data
1270
RX Data & Control Processor
1284
Scheduler
DL Data
1290
TX Data & Control Processor
1260
DEMOD
1280
Controller/ Processor
1292
MOD
1254
RCVR
1282
Memory
1294
TMTR
1252
1224
1222
TMTR
1230
RCVR
UE
1220
MOD
1242
Memory
1232
DEMOD
1210
TX Data & Control Processor
1240
Controller/ Processor
1234
RX Data & Control Processor
120
UL Data
DL Data

FIG. 12

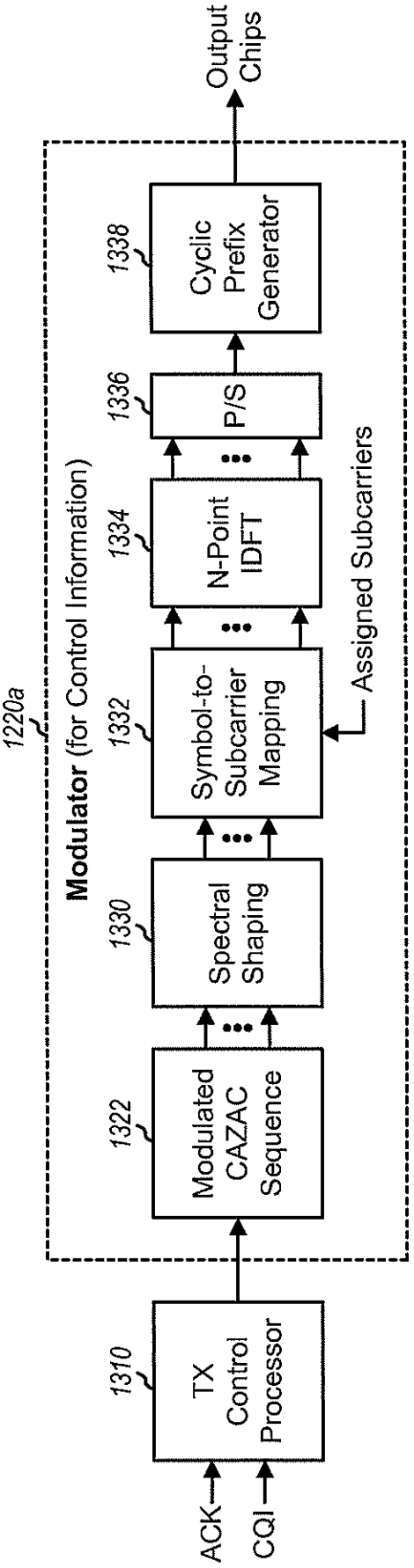

ACK
CQI
1310
TX Control Processor
1220a
Modulator (for Control Information)
1322
Modulated CAZAC Sequence
1330
Spectral Shaping
1332
Symbol-to-Subcarrier Mapping
Assigned Subcarriers
1334
N-Point IDFT
1336
P/S
1338
Cyclic Prefix Generator
Output Chips

FIG. 13

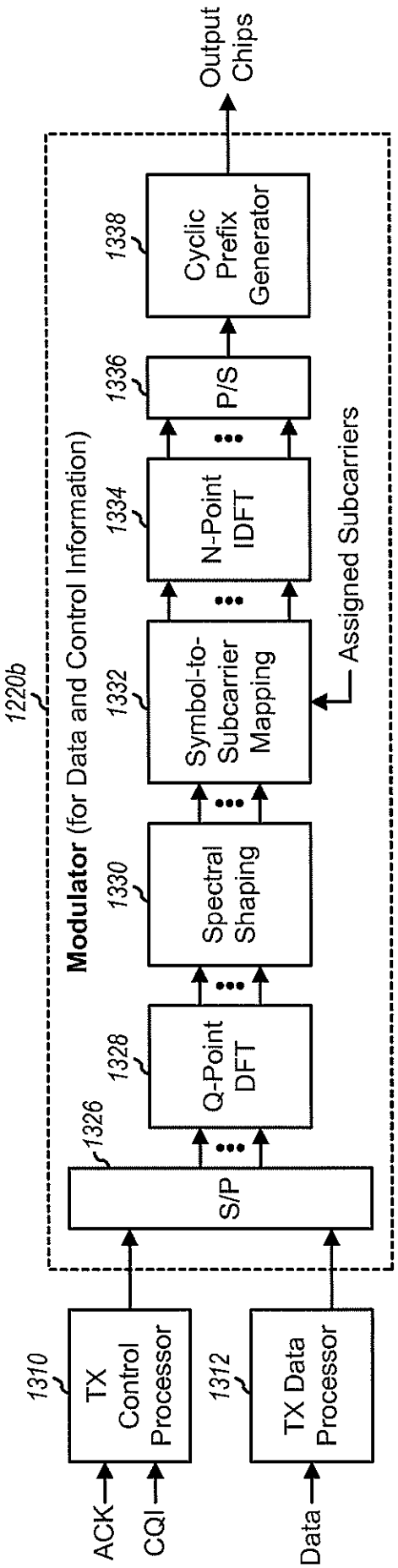

ACK
CQI
Data
1310
TX Control Processor
1312
TX Data Processor
1220b
Modulator (for Data and Control Information)
1326
S/P
1328
Q-Point DFT
1330
Spectral Shaping
1332
Symbol-to-Subcarrier Mapping
Assigned Subcarriers
1334
N-Point IDFT
1336
P/S
1338
Cyclic Prefix Generator
Output Chips

FIG. 14

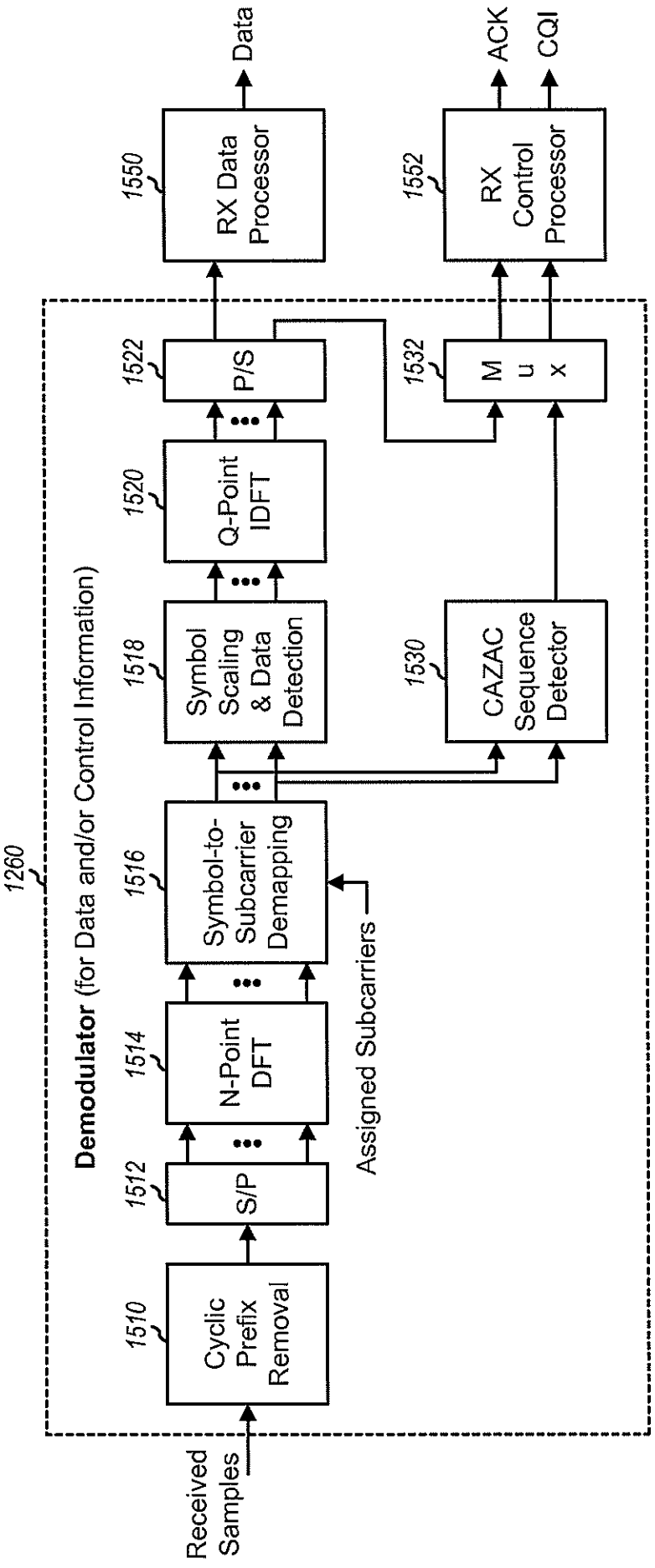

Data
ACK
CQI
1550
RX Data Processor
1552
RX Control Processor
1522
P/S
1532
M u x
1520
Q-Point IDFT
1518
Symbol Scaling & Data Detection
1530
CAZAC Sequence Detector
1516
Symbol-to-Subcarrier Demapping
1514
N-Point DFT
1512
S/P
1510
Cyclic Prefix Removal
1260
Demodulator (for Data and/or Control Information)
Assigned Subcarriers
Received Samples

FIG. 15