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Process and device for polishing semiconductor wafers

5 The invention relates to a process for polishing semiconductor wafers, in which at least one side of at least one semiconductor wafer is pressed against a polishing plate, over which a polishing cloth is stretched, and is polished, the semiconductor wafer and the polishing plate executing a relative movement. The invention also relates to a device which is suitable for carrying out the process.

10 Making a semiconductor wafer planar by means of a chemo-mechanical polishing process represents an important processing step in the process sequence for producing a planar, flawless and smooth semiconductor wafer. In many manufacturing sequences, this polishing
15 step represents the last shaping step, and therefore the step which decisively determines the surface properties, before the semiconductor wafer is used further as starting material for the production of electrical, electronic and microelectronic components. The aims of
20 the polishing process are in particular to achieve a high planarity and parallelism of the two sides of the wafer, to remove surface layers which have been damaged by pretreatments ("damage removal") and to reduce the microroughness of the semiconductor wafer.

25 Single side polishing processes and double side polishing processes are generally used. In the case of single side polishing of a batch of a plurality of semiconductor wafers ("single side batch polishing"), one side of the semiconductor wafers is mounted on the front
30 side of a carrier plate by producing a form-fitting and force-fitting connection between the side and the carrier plate, for example by adhesion, bonding, cementing or the application of vacuum. As a rule, the semiconductor wafers are mounted on the carrier plate in such a way
35 that they form a pattern of concentric rings. After having been mounted, the free sides of the wafers are pressed against a polishing plate, over which a polishing cloth is stretched, with a defined polishing force and



with a polishing abrasive being supplied and these sides are polished. In the process, the carrier plate and the polishing plate are usually rotated at different speeds. The polishing force required is transmitted to the rear side of the carrier plate by a pressure piston, which is referred to below as the polishing head. A large number of the polishing machines used are designed in such a way that they have a plurality of polishing heads and, accordingly, are able to accommodate a plurality of carrier plates.

In double side polishing (DSP), the front side and rear side are polished simultaneously, in that a plurality of semiconductor wafers are guided between two, upper and lower, polishing plates over which polishing cloths are stretched. In this case, the semiconductor wafers lie in thin wafer carriers, which are referred to as rotor disks and are also used in a similar form during lapping of semiconductor wafers. Double side polishing processes and devices are always designed for treating groups of semiconductor wafers ("batch polishing").

A plurality of factors make it difficult to achieve the desired planarity and parallelism of the semiconductor wafers, referred to below as the desired geometry. Polished semiconductor wafers often have sides which do not lie parallel to one another, but rather assume the form of a wedge in cross-section.

The shape of the wedge can be described using the term linear thickness variation. The linear thickness variation is the largest measured difference in thickness between two measurement points which lie on the same diameter, symmetrically with respect to the center of the semiconductor wafer. Usually, the measurement points lie symmetrically on a circle which is at a distance of, for example, 6 mm from the edge of the semiconductor wafer. If the edge of the semiconductor wafer which faces toward the edge of the carrier plate is thicker (thinner) than the wafer edge which faces toward the center of the carrier plate, this is known as a positive (negative) linear wedge shape.



Another measurement of the wedge shape of semiconductor wafers is the so-called TTV value (TTV = total thickness variation). This value gives the difference between the thickest and thinnest points on the semiconductor wafer.

A semiconductor wafer wedge shape caused by the polishing is ultimately the result of uneven removal of material. This may arise if the carrier plate is deformed radially during polishing as a result of its own weight or has a certain radial wedge shape caused by its production. Sometimes, incipient wear to the polishing cloth is also a cause of the wafer geometry deteriorating over the course of a number of polishing runs. A certain fundamental wedge shape results even when using carrier plates which are of ideal planarity, owing to the kinematic ratios during single wafer polishing, which require inhomogeneous removal of material.

It is proposed in EP-4033 A1 to insert interlayers of soft, elastic bodies between the polishing head and the rear side of the carrier plate, with the result that the carrier plate is deliberately curved slightly in a radially symmetrical manner. In this way, it is possible, to a certain extent, to prevent the semiconductor wafers from being polished into a wedge. However, this process cannot be automated and is susceptible to faults, since its success depends for the most part on the experience of and the care taken by the operating personnel, who have to select and insert the interlayers on the basis of their width. However, even if no mistakes are made in doing this, the wedge shape of the polished semiconductor wafers remains above a defined limit value.

The present invention achieves the object of improving the uniformity of polishing abrasion when polishing semiconductor wafers, so that in particular the wedge shape of the polished semiconductor wafers is low.

The invention relates to a process for polishing semiconductor wafers, in which at least one side of at least one semiconductor wafer is pressed against a





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polishing plate, over which a polishing cloth is stretched, and is polished, the semiconductor wafer and the polishing plate executing a relative movement, wherein the semiconductor wafer passes over at least two
5 regions on the polishing plate during the polishing, which regions have defined radial widths and are at different temperatures, and temperature-control means are provided in the polishing plate, with the aid of which the number, the radial widths and the temperatures of the
10 regions are fixed before the semiconductor wafers are polished.

The invention furthermore relates to a device for carrying out the process, which has a chamber system, which is accommodated in the polishing plate, comprising
15 concentrically arranged annular chambers through which a temperature-control medium flows, which is at a defined, adjustable temperature in each annular chamber.

Investigations carried out by the inventors have shown that during polishing a radially convex temperature
20 profile is established on the polishing plate, which is partly responsible for the wedge shape of polished semiconductor wafers. The temperature profile causes an inhomogeneous removal of material which cannot be compensated for (for example when using ceramic carrier plates,
25 which practically cannot be curved) or cannot be compensated for sufficiently (when using carrier plates made from less rigid material) by using the abovementioned elastic interlayers. The present invention allows such compensation, because the creation of temperature-
30 controlled regions specifies a radial temperature profile of the polishing plate which is to some extent decisive in determining the amount of material removed. The invention allows the wedge shape of semiconductor wafers to be set within comparatively wide limits by polishing.
35 By means of the invention, it is possible to produce semiconductor wafers which have a controlled positive or negative wedge shape. However, the invention is primarily used to compensate for kinematic effects and effects of the carrier plate or of the polishing cloth which would



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lead to wedge shapes and, for example, to extend the service life of the polishing cloth.

The invention can be used both for single side polishing (single-wafer and batch polishing) and for double side polishing. The invention is explained in more detail below with reference to the example of single side batch polishing.

According to the invention, it is ensured that the semiconductor wafers pass over at least two regions on the polishing plate during polishing, which regions are kept at certain temperatures by temperature-control means in the polishing plate. The regions are preferably positioned in concentric rings, with the temperatures of at least two of the regions differing. The number, the radial widths and the temperatures of the regions are fixed before a polishing run. The possibility of changing the temperatures at which the regions are held during a polishing run is not ruled out.

Owing to effects of polishing kinematics, the use of carrier plates which are not completely planar and inhomogeneous wear to the polishing cloth, on a conventional polishing plate the temperature is not homogeneous during polishing of semiconductor wafers. The temperature often increases from the edge to $r/2$ of the polishing plate (r is the radius of the polishing plate) and falls toward the center of the polishing plate, so that a radially convex temperature profile results. By establishing regions on the polishing plate which can be held at certain temperatures by temperature-control means accommodated in the polishing plate, it is possible to homogenize the temperature profile. In order to avoid the formation of a radially convex temperature profile, at least two temperature-controlled regions should be established on the polishing plate. A suitable form is, for example, three regions in the form of concentric rings, the outer and inner regions being held at a higher temperature than the middle region. As a result, heat which is generated in the central region of the polishing plate during polishing of semiconductor wafers is



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dissipated via the temperature-control means. The outer and inner ring, and hence those parts of the polishing plate which are close to the edge, by contrast, receive additional thermal energy, so that a flatter radial temperature profile is the overall result. In principle, the invention can be used to level out any desired radial temperature profile which occurs during polishing.

The number of regions, their radial width and the temperatures at which they are held are fixed before the semiconductor wafers are polished. Data from analyzing the geometry of previously polished semiconductor wafers, for example the linear thickness variation determined for these semiconductor wafers, can be used as a basis for fixing the above factors. Measured data relating to the radial temperature profile of the polishing plate which were determined during a preceding polishing run may also be used as a basis.

The functional connection between the semiconductor wafer geometry which is to be expected after a polishing and the number, width and temperatures of the regions on the polishing plate which are to be fixed is advantageously determined by routine experiments. In such experiments, the number, radial width and temperatures of the regions are systematically changed and the effects on the geometry of the polished semiconductor wafers are investigated.

After concluding such experiments, the polishing process can be automated in a simple manner. A master computer receives, as input data, the radial temperature profile which was determined during a preceding polishing run or data relating to the geometry (for example to the wedge shape) of semiconductor wafers which were polished during a preceding polishing run and, on the basis of the empirically discovered relationship, fixes the parameters required to achieve a desired wafer geometry (number, radial width and temperature of the regions).

The invention is described in more detail below with reference to figures. Figure 1 diagrammatically shows a preferred embodiment of the claimed device. The



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figure shows a side view of a vertical section through the device. Figure 2 shows a plan view of a horizontal section through the polishing plate of the device. Figures 3a, 3b and 4a, 4b diagrammatically show how the geometry of semiconductor wafers can be influenced by employing the invention. In the following text, reference is made only to features which are required to explain the invention. In the figures, similar features are denoted by the same reference symbols.

Reference is made initially to Figure 1. The embodiment shown relates to a single side polishing machine with a plurality of polishing heads, one of which can be seen. The polishing head 1 presses a carrier plate 2 with a polishing force X against a polishing plate 4 over which a polishing cloth 3 is stretched. The carrier plate is held on the polishing head by means of vacuum suction, for example. The semiconductor wafers 5 are fixed on the front side, facing toward the polishing cloth 3, of the carrier plate 2. During polishing, both the carrier plate and the polishing plate rotate at a certain speed and with a certain direction of rotation. The essential features of the device are annular chambers in the polishing plate which run in concentrically arranged paths and through which a temperature-control medium flows. In the polishing plate illustrated, five annular chambers Z1 to Z5 are provided. Each annular chamber, independently of any other, has a temperature-control medium, for example water, flowing through it, the temperature-control medium being at a specific temperature in each annular chamber and it being possible for the temperatures to differ. The temperature-control medium is pumped into the respective annular chambers through flow lines VZ1 to VZ5 and leaves these chambers again through return lines RZ1 to RZ5. The flow and return lines run through a rotary leadthrough 6 which is attached to the underside of the polishing plate 4. For reasons of clarity, the flow and return lines are illustrated in an interrupted manner. The temperature-control medium is held at a desired temperature by a thermostat



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device 7. The thermostat device is controlled by a master computer 8 which prescribes the desired temperatures SZ1 to SZ5 for the temperature-control medium in the annular chambers Z1 to Z5. The master computer for its part
5 accesses a memory 9 in which measured data from preceding polishing runs are stored and, from these, automatically calculates the desired temperatures.

The temperature-control medium maintains a defined temperature in each annular chamber, so that
10 radially symmetrical regions of characteristic temperature are formed on the polishing plate, the semiconductor wafers passing over these regions during polishing. The number of available regions depends on the number of annular chambers provided. The radial widths of the
15 regions are dependent on the selected radial widths of the annular chambers and on the temperature of the temperature-control medium which flows through the annular chambers.

Figure 2 illustrates a horizontal section through
20 the polishing plate of the device in accordance with Fig. 1, in plan view. If the temperature of the temperature-control medium differs in each annular chamber Z1 to Z5 from the temperatures of the temperature-control medium in the other annular chambers, the annular chambers form
25 a number of annular regions on the polishing plate which corresponds to the number of annular chambers. These regions are kept at a temperature which essentially corresponds to the temperature of the temperature-control medium in the associated annular chamber. The number of
30 regions is correspondingly lower if the temperature of the temperature-control medium in two or more adjacent annular chambers is identical. If the temperature of the temperature-control medium is identical in two adjacent annular chambers, this results in a region on the polish-
35 ing plate with a radial width which approximately corresponds to the sum of the radial widths of these annular chambers. Preferably, 2 to 5 annular chambers are provided. The radial widths of the annular chambers preferably amount to 25 to 120% of the diameter of the

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semiconductor wafers to be polished.

As an alternative to the illustration shown in Fig. 2, the annular chambers may also be inherently structured (for example in meandering form). It is also possible to set a defined radial temperature profile on the polishing plate by providing regions of a specific temperature in other ways from that described above, for example by integrating heating and cooling elements in the polishing plate. These may be operated by induction or by a power supply which is also accommodated in the polishing plate.

Figures 3a, 3b and 4a, 4b diagrammatically illustrate how the geometry of semiconductor wafers can be influenced by employing the invention. The figures reflect the result of exemplary embodiments.

After a polishing run in a device in accordance with Fig. 1, semiconductor wafers with a positive wedge shape were obtained. During the polishing run, temperature-control medium flowed through the annular chambers with its temperature in the annular chambers Z1 to Z5 controlled in the following way: Z1=30°C, Z2=30°C, Z3=40°C, Z4=30°C and Z5=30°C (Fig. 3a). By changing the temperatures in the annular chambers (Z1=40°C, Z2=40°C, Z3=30°C, Z4=40°C and Z5=40°C) it was possible, after a following polishing run, to obtain semiconductor wafers with virtually plane-parallel sides (Fig. 3b).

After a polishing run in a device in accordance with Fig. 1, semiconductor wafers with a negative wedge shape were obtained. During the polishing run, temperature-control medium flowed through the annular chambers, with its temperature in the annular chambers Z1 to Z5 controlled in the following way: Z1=30°C, Z2=30°C, Z3=40°C, Z4=30°C and Z5=30°C (Fig. 4a). By changing the temperatures in the annular chambers (Z1=20°C, Z2=20°C, Z3=50°C, Z4=20°C and Z5=20°C) it was possible, after a following polishing run, again to obtain semiconductor wafers with virtually plane-parallel sides (Fig. 4b).

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Patent claims

1. A process for polishing semiconductor wafers, in which at least one side of at least one semiconductor wafer is pressed against a polishing plate, over which a polishing cloth is stretched, and is polished, the semiconductor wafer and the polishing plate executing a relative movement, wherein the semiconductor wafer passes over at least two regions on the polishing plate during the polishing, which regions have defined radial widths and are at different temperatures, and temperature-control means are provided in the polishing plate, with the aid of which the number, the radial widths and the temperatures of the regions are fixed before the semiconductor wafers are polished.
2. The process as claimed in claim 1, wherein, in plan view of the polishing plate, the regions form concentric rings.
3. The process as claimed in claim 1 or claim 2, wherein the number, the radial widths and the temperatures of the regions are fixed as a function of the result of a measurement, which is carried out during a preceding polishing run, of the radial temperature profile of the polishing plate.
4. The process as claimed in claim 1 or claim 2, wherein the number, the radial widths and the temperatures of the regions are fixed as a function of the result of an analysis of the geometry of previously polished semiconductor wafers.
5. The process as claimed in one of claims 1 to 4, wherein the number, the radial widths and the temperatures of the regions are fixed automatically with the aid of a computer.
6. The process as claimed in one of claims 1 to 5, wherein the temperatures of the regions are changed during the polishing.
7. The process as claimed in one of claims 1 to 6, wherein the polishing is selected from a group of polishing processes which comprises single side polishing,



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double side polishing, single wafer polishing and batch polishing.

5 8. A device for polishing semiconductor wafers, having at least one polishing plate over which a polishing cloth is stretched, which has a chamber system, which is accommodated in the polishing plate, comprising concentrically arranged annular chambers through which a temperature-control medium flows, which is at a defined, adjustable temperature in each annular chamber.

10 9. The device as claimed in claim 8, which has a master computer which, on the basis of transmitted process data, controls the temperature of the temperature-control medium in each annular chamber.

15 10. The device as claimed in claim 8 or claim 9, wherein each annular chamber has a radial width of from 25 to 120% of the diameter of the semiconductor wafers.

