CLAIMS

1. An integrated circuit, comprising:

at least one photodetection region configured to generate charge carriers in response to receiving incident photons; and

at least one charge storage region configured to receive the charge carriers from the photodetection region,

wherein:

charge carriers stored in the at least one charge storage region indicate timing information and spectral information of the incident photons; and

the at least one charge storage region comprises first and second charge storage regions, charge carriers stored in the first charge storage region indicate the timing information, and charge carriers stored in the second charge storage region indicate the spectral information.

2. The integrated circuit of claim 1, wherein the timing information comprises luminescence lifetime information.

3. The integrated circuit of claim 1, wherein the spectral information comprises wavelength information.

4. The integrated circuit of claim 3, wherein the at least one photodetection region is configured to receive a first plurality of incident photons having first spectral characteristics and a second plurality of incident photons having second spectral characteristics, and the spectral information indicates a difference between the first and second spectral characteristics.

5. The integrated circuit of claim 4, wherein the spectral information indicates a difference between a wavelength of the first plurality of incident photons and a wavelength of the second plurality of incident photons.

6. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 600 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 600nm.

7. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 600 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 700nm.

8. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 700 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 700nm.

9. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 550 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 600nm.

10. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 550 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 550nm.

11. The integrated circuit of claim 1, wherein the first and second charge storage regions have different depths in a first direction in which the at least one photodetection region is configured to receive the incident photons.

12. The integrated circuit of claim 11, wherein the at least one photodetection region comprises a photodetection region configured to generate and transfer the charge carriers to the first and second charge storage regions.

13. The integrated circuit of claim 11, wherein the at least one photodetection region comprises first and second photodetection regions configured to generate first and second charge carriers, respectively, and the first charge storage region is configured to receive the first charge carriers and the second charge storage region is configured to receive the second charge carriers.

14. The integrated circuit of claim 11, further comprising:

a first charge transfer region disposed between the at least one photodetection region and the first charge storage region; and

a second charge transfer region disposed between the at least one photodetection region and the second charge storage region,

wherein the first charge transfer region is positioned, at least in part, in the first direction, before or after the second charge transfer region.

15. The integrated circuit of claim 14, further comprising:

a third charge transfer region configured to receive the charge carriers from the at least one photodetection region,

wherein the third charge transfer region is positioned, at least in part, in the first direction, before or after the first and/or second charge transfer region(s).

16. The integrated circuit of claim 1, further comprising a pixel comprising the at least one photodetection region and the at least one charge storage region, wherein the pixel is 10 microns by 10 microns or smaller.

17. An integrated circuit, comprising:

at least one photodetection region configured to generate first charge carriers in response to receiving incident photons in a first direction;

at least one charge storage region configured to receive the first charge carriers from the at least one photodetection region and positioned at a first depth in the first direction; and

a region positioned at a second depth in the first direction and configured to generate second charge carriers responsive to the incident photons,

wherein the first charge carriers indicate lifetime information of the incident photons, and the second charge carriers indicate spectral information of the incident photons.

18. The integrated circuit of claim 17, wherein the at least one photodetection region comprises:

a first photodetection region configured to transfer the first charge carriers to a first charge storage region of the at least one charge storage region; and

a second photodetection region comprising the region positioned at the second depth in the first direction, wherein the second photodetection region is configured to transfer the second charge carriers to a second charge storage region of the at least one charge storage region.

19. The integrated circuit of claim 18, further comprising:

a first transfer gate configured to bias a first transfer channel between the first photodetection region and the first charge storage region; and

a second transfer gate configured to bias a second transfer channel between the second photodetection region and the second charge storage region.

20. The integrated circuit of claim 17, wherein the at least one charge storage region comprises:

a first charge storage region configured to receive the first charge carriers from the at least one photodetection region and positioned at the first depth in the first direction; and

a second charge storage region comprising the region positioned at the second depth in the first direction, wherein the second charge storage region is configured to generate and store the second charge carriers responsive to the incident photons.

21. The integrated circuit of claim 20, wherein:

the second depth is positioned after the first depth in the first direction; and

the second charge storage region is configured to receive the incident photons.

22. The integrated circuit of claim 17, wherein the integrated circuit further comprises a first transfer gate configured to bias a first transfer channel electrically coupling the at least one photodetection region to the first charge storage region.

23. The integrated circuit of claim 22, further comprising:

a third charge storage region configured to receive the charge carriers and positioned at a third depth that is before the second depth in the first direction; and

a second transfer gate configured to bias a second transfer channel electrically coupling the at least one photodetection region.

24. The integrated circuit of claim 23, wherein the second charge storage region is disposed, at least in part, between the at least one photodetection region and the third charge storage region.

25. The integrated circuit of claim 32, wherein the spectral information comprises wavelength information.

26. A method of operating the integrated circuit of any one of claims 1 to 25, the method comprising:

detecting, using at least one processor, a first number of charge carriers stored in the first charge storage region;

detecting, using the at least one processor, a second number of charge carriers stored in the second charge storage region; and

combining, using the at least one processor, the first number and second numbers to determine the lifetime or timing information and/or the spectral information.

27. The method of claim 26, wherein the act of combining includes adding and/or subtracting by the at least one processor.

28. A system, comprising:

the integrated circuit of any one of claims 1 to 25; and

a control circuit configured to provide control signals to transfer gates of the integrated circuit to control time-gating of charge carriers from the at least one photodetection region to the at least one charge storage region.