

Description

Capacitor in a semiconductor arrangement, and method for its production

The invention relates to a capacitor in a semiconductor arrangement, in particular in a DRAM memory arrangement, having an electrode structure containing a plurality of elements which are arranged at a distance from one another and are electrically interconnected by means of a connection structure, having a capacitor dielectric and having a counter-electrode. The invention further relates to a method for the production of a capacitor in a semiconductor arrangement.

A large number of integrated circuits require capacitors. Analog/digital converters, digital/analog converters and filter circuits come into consideration along with the typical example of a dynamic memory cell. Measures for reducing the intrinsically high space requirement of a capacitor are necessary, in particular, in the context of the miniaturization of structures on account of the increased integration level or because it is necessary to reduce the area of the chip. The dynamic semiconductor memory may serve as a typical example here; with this memory the area required by the single-transistor memory cell that is usually used is reduced from memory generation to memory generation as the storage density increases. At the same time, the minimum capacitance of the storage capacitor must be retained.

In dynamic semiconductor memory arrangements, a single-transistor memory cell comprises a read-out transistor and a capacitor. The information stored in the capacitor, that is to say the electric charge, can be read out via a bit line by driving the read-out transistor via a word line. For the reliable storage of the charge and the simultaneous distinguishability of the information read out, the storage capacitor must have a minimum capacitance. The lower limit for the capacitance of the storage capacitor is currently regarded as 20 fF.

In order to achieve this capacitor capacitance, the dielectric must have the smallest possible thickness and the capacitor must have the largest possible area.

Whereas both the read-out transistor and the capacitor were realised as planar components up to the 1 Mbit memory generation, starting with the 4 Mbit memory generation arrangements are known in which the capacitor is arranged in a trench (trench capacitor). The electrodes of the capacitor are arranged along the surface of the trench. The overall result is that the effective area of the capacitor is enlarged in comparison with a planar arrangement on the surface of the substrate.

A further possibility for increasing the capacitance while retaining or reducing the space requirement of the capacitor is to design the latter as a stacked capacitor. In this case, a structure of polysilicon, for example a crown structure or a cylinder, is formed via the word lines and makes contact with the substrate. The polysilicon structure forms the memory node which is provided with the capacitor dielectric and the capacitor plate, the so-called cell plate. The concept has the advantage that it is compatible with a logic process.

The free space above the substrate surface is utilized for the capacitor. In this case, the entire cell area can be covered by the polysilicon structure as long as the structures of neighbouring memory cells are insulated from one another. Known key words in this context are: fin stacked capacitor and crown stacked capacitor.

EP-A-0 415 530 discloses a semiconductor memory arrangement having a stacked capacitor as storage capacitor. The stacked capacitor comprises a polysilicon structure having a plurality of polysilicon layers which are arranged essentially parallel one above the other and are connected to one another via at least one lateral support. The lateral support is produced with the aid of a polysilicon layer, which is subsequently etched back to leave an essentially vertically arranged web which connects the polysilicon layers arranged one above the

other. The structure is formed by alternately depositing polysilicon layers and silicon oxide layers, which can be selectively etched with respect to the said polysilicon layers, on the surface of the substrate by structuring these layers, by producing the lateral supports on at least one side of the structure and by selectively etching out the silicon oxide layers. The polysilicon structures are in this case doped with arsenic. Silicon oxide is subsequently formed as the capacitor dielectric by means of thermal oxidation, on which dielectric the cell plate made of doped polysilicon is deposited.

US-A-5,240,871 discloses a capacitor having electrode layers lying one above the other, in which capacitor insulation layers which are etched at different rates are applied to a polysilicon layer and are subsequently structured and etched to form a supporting framework. Afterwards, doped polysilicon is deposited and then a silicon nitride layer, and this is followed by the formation of the cell plate.

The invention is based on the problem of specifying a capacitor in a semiconductor memory arrangement which enables a high component density in conjunction with reduced process complexity and space requirement. A production method for such a capacitor is also intended to be specified.

This problem is solved by a capacitor having the features of Claim 1 and by a method for the production of a capacitor having the features of Claim 6.

The critical advantage of the invention is that the thickness of the capacitor when arranged horizontally or the width of the capacitor when arranged vertically is less than in the case of known capacitors. The capacitor can be used, in particular, in DRAM semiconductor arrangements, since it takes up a small thickness and a small area for the required minimum cell capacitance of 20 fF. It can be estimated that a capacitor of this type can also be used to realise the storage capacitances of future DRAM generations, which will impose even more stringent demands regarding their area requirement. For



this purpose, it is merely necessary to increase the number of layers given a reduced layer area. Moreover, it is possible to reduce the thickness or the width of the capacitor by reducing the layer thickness and the dielectric thickness. The capacitor furthermore has the advantage that its electrode structure can be connected, in the case of p-channel transistors, directly to the drain of the transistor with the aid of a contact hole. However, other ways of making contact between the electrode structure and other circuit elements are also possible. For example, in the case of an n-channel selection transistor, the electrode structure can make contact with the drain of the transistor via an intermediate metal layer, for example made of tantalum, titanium, titanium nitride, or a silicide layer or a contact hole filling, for example with tungsten.

The method according to the invention has the significant advantage over known methods that fewer process steps are necessary, without having to accept losses in other respects.

Refinements of the invention are characterized in subclaims.

It is provided that the capacitor in a semiconductor arrangement has an electrode structure containing a plurality of elements which are arranged at a distance from one another and are electrically interconnected by means of a connection structure, the elements of the electrode structure and the associated connection structure being composed completely of p-doped material with a doping $> 10^{20} \text{ cm}^{-3}$. In this case, the elements of this electrode structure can be arranged in a planar manner one above the other or next to one another. The connection structure extends at least at one edge in the transverse direction with respect to the surface of the elements. On the other hand, the elements of the electrode structure can have a pot-shaped design and be nested one in the other, the connection structure being connected within the pot-shaped region to a carrier of the capacitor arrangement and to the bottom part or the

bottom parts of the elements. The connection structure may preferably be designed as a bar-like supporting element centrally within the pot-shaped electrode structure.

In the method for the production of a capacitor, a base layer is first of all produced on a surface of a carrier arrangement, which base layer contains a p⁺-type layer to which a layer sequence consisting alternately of a weakly doped and a heavily doped p-conducting layer is subsequently applied. After this, the layer sequence is anisotropically etched to form an opening, which reaches at least as far as the p⁺-type layer of the base layer. A p⁺-conducting zone, which connects the layer sequence, is then produced at least in one edge region of the opening. The weakly doped, p-conducting layers of the layer sequence are subsequently etched selectively with respect to the p⁺-type layers, the dielectric is deposited and a counter-electrode formed.

In this case, the base layer can be produced in such a way that it contains only a p⁺-type layer or a p⁺-type layer having an oxide and/or nitride layer situated underneath. Depending on the desired structure of the capacitor, the p⁺-type zone in the opening is produced by implanting ions, that is to say boron ions, at an oblique angle or by applying a p⁺-conducting material. The important point here is that the layer sequence is not completely covered by a p⁺-type zone, in order to enable the etchant to attack the weakly doped p-type material for the following selective etching.

The selective etching is carried out with the aid of an alkaline etchant, for example an ethylenediamine/pyrocatechol or potassium hydroxide solution. After the weakly doped, p-conducting layer materials have been etched out, a dielectric, for example an ONO dielectric, is applied and a conductive material is subsequently conformally deposited as counter-electrode.

The base layer can be produced on a planarized surface of an insulator. Provided that a contact hole to a connection area situated underneath is provided in the

insulator, this contact hole can likewise be filled with the p⁺-type material of the base layer. In addition to this vertical contact-making of the electrode structure, contact can be made by means of lateral connections. The base layer and subsequently the electrode structure can, on the other hand, be produced in a trench of an insulation layer or of a silicon layer. If appropriate, a silicon oxide and/or a silicon nitride layer are/is provided underneath the p⁺-type partial layer of the base layer.

The production of the capacitor is based on the insight that the etching rate of p⁺-doped silicon compared with weakly doped silicon in alkaline etching solutions is extremely low. From the publication H. Seidel et al.: Anisotropic Etching of Crystalline Silicon in Alkaline Solutions, J. Electrochem. Vol. 137, No. 11, Nov. 1990, pp. 3626 to 3632, the etching rate of p-doped silicon in an ethylenediamine/pyrocatechol [sic] solution is constant up to a concentration of 10^{19} cm^{-3} and then sharply decreases. At a concentration of $2 \cdot 10^{20} \text{ cm}^{-3}$, the etching rate is only less than one thousandth of the etching rate at 10^{19} cm^{-3} .

The invention is explained in more detail below using exemplary embodiments with reference to figures, in which:

FIG 1a to FIG 1f show the production of a first exemplary embodiment of a capacitor,

FIG 2 shows a diagrammatic cross-section through a second exemplary embodiment of a capacitor,

FIG 3 shows a diagrammatic plan view of possible geometric arrangements, and

FIG 4a to c show a diagrammatic production [sic] through a third exemplary embodiment of a capacitor.

According to FIG 1a, a carrier arrangement is provided which has an insulating layer 1 at its surface. Further elements of a semiconductor arrangement, for example transistors, can be arranged underneath the insulating layer. A contact hole 2 is provided within the insulating layer 2 [sic], flush with the surface, and is

filled with a metallizing material. Tungsten, tantalum, titanium, titanium nitride or doped polysilicon can be provided as the filling material. If used, n-doped polysilicon must be siliconized so that a metallic intermediate layer appears on the surface. The contact hole 2 filled with a material of metallic conductivity forms the connection contact for the electrode structure to be produced. A glass layer, for example BPSG, may be provided as the insulating layer 1 of the carrier arrangement, which glass layer affords the advantage of a planar surface due to flowing of the glass. However, it is also possible to provide an insulating layer which is planarized by a polishing step, for example CMP.

A base layer 3, which is a heavily doped, p-conducting layer in the exemplary embodiment, is subsequently produced on the surface of the carrier arrangement and contact hole 2. The doping level depends on the selection of the etching solution to be used later, and should be selected in such a way that the etching rate is extraordinarily low. For example, it is expedient to select a boron concentration $> 10^{20} \text{ cm}^{-3}$ for an ethylenediamine/pyrocatechol solution. The thickness of the base layer may be 300 nm, for example. A layer sequence consisting alternately of a p⁻-type layer and a p⁺-type layer is subsequently applied to the heavily doped, p-conducting layer of the base layer 3. The heavily doped layers 5 and 7 are in this case doped in a manner corresponding to the heavily doped, p-conducting layer of the base layer. The weakly doped, p-conducting layers 4 and 6 have a doping permitting a high etching rate with regard to the selectively acting etchant. For example, the boron doping with the above-described ethylenediamine/pyrocatechol solution is about 10^{19} cm^{-3} or less.

The layer thickness are selected in such a way that the weakly doped, p-conducting layers are thicker than the heavily doped, p-conducting layers. For example, the p⁻-type layers have a thickness of 30 nm and the p⁺-type layers 5 and 7 have a thickness of 10 nm.

The layers 3 to 7 are conformally deposited. Possible deposition methods are chemical deposition from the vapour phase at low pressures, in particular hot wall or cold wall LPCVD, or molecular beam epitaxy. The layer sequence can be applied in situ in one and the same reactor. For this purpose, it is necessary to set different process parameters for the p⁻-doped layers 4 and 6 in comparison with the p⁻-doped polysilicon layers 3, 5 and 7.

In accordance with FIG 1b, a mask (not illustrated) is subsequently produced and is used to etch the layer sequence 3 to 7 anisotropically, to form one or more openings 8. KOH can be used as etchant. In the FIG, the openings 8 are etched through down to the insulating layer of the carrier arrangement 1. This produces separated islands, in each of which a capacitor can be produced. However, it is not always necessary to etch the openings down to the p⁻-conducting layer of the base layer. If the base layer 3 is not etched through completely, a large-area capacitor arrangement is produced. The polysilicon layer sequence is structured in such a way that the stacks are round or angular in plan view, FIG 3.

In the next step, a heavily doped, p-conducting zone, which connects the layer sequence 3 to 7, is produced in an edge region of the opening 8. Implantation of BF₃ ions at an oblique angle takes place for this purpose, for example at an angle of 8° to the vertical. As an alternative here, it is possible also to implant the other side of the opening shown in FIG 1b with boron ions. The implantation has the effect that, in the edge region of the opening which is situated under the bombardment of boron ions, a limited zone of the weakly doped, p-conducting layers 4 and 6 are [sic] heavily doped, the doping corresponding to the doping of the remaining p⁻-doped polysilicon layers. A temperature step is then provided in order to ensure that the implanted boron ions are activated, that is to say occupy the appropriate lattice sites in the polysilicon layer 4 and

6. In this case it is necessary that diffusion does not take place from the heavily doped zones into the weakly doped zones. The temperature step can preferably be carried out with the aid of an RTA (Rapid Thermal Annealing) process. The selected temperature is about 850 to 900°C.

FIG 1c shows the structure produced after the temperature step. Due to the implantation of boron ions at an oblique angle into the openings 8, a p⁺-type zone 9, which connects the p⁺-type layers 3, 5 and 7 to one another, has been produced in the edge region of each opening. In the exemplary embodiment, the p⁺-type zones have the form of a reversed "E". On the edge region of the openings 8 which is opposite the zones 9, on the other hand, the originally produced layer sequences 3 to 7 is [sic] preserved, with the result that the weakly doped layers 4 and 6 point freely to the opening.

If a structured layer sequence which is round in plan view is produced by the anisotropic etching step by which the openings 8 are produced, then the zones 9 extend with a decreasing thickness over a specific part of the periphery of the stack. The effect that can be achieved by a rectangular stack is that only one side of the stack or else two sides of the stack are p⁺-doped at the edge, as a result of which the zones 9 are either present only on one side of the stack or else cover two sides of the stack at an angle. The diameter of a stack shaped in this way or the width is about 1 μm . FIG 3 shows examples of the design of the structured and doped stacks according to FIG 1c. The implantation direction is indicated in each case. In the examples shown in FIG 3, a very robust structure results for the capacitor to be produced.

In the next step, the arrangement is selectively etched isotropically using an alkaline etchant. A suitable etching solution is, for example, ethylenediamine/pyrocatechol. Given the selected doping, the alkaline etching solutions have the property that the weakly doped, p-conducting layers are etched more strongly than

the p⁺-doped layers, with a selectivity of 100:1 to 1000:1. The structure produced after the etching process is a structure according to FIG 1d, in which only the p⁺-doped regions have remained and are interconnected in such a way that a supporting structure is formed. The structure is designated by 10.

With the next step, in accordance with FIG 1e, the capacitor dielectric is conformally deposited. The dielectric may be formed from silicon oxide and/or silicon nitride. An ONO dielectric layer, which is composed of a first silicon oxide layer, a silicon nitride layer and a second silicon oxide layer, is preferably provided. An overall layer thickness of about 10 nm is envisaged for the capacitor dielectric. For higher capacitances to be produced, however, the thickness of the capacitor dielectric can also be selected to be smaller, for example 3 nm.

The counter-electrode of the capacitor 12 is produced on the capacitor dielectric by means of conformal deposition, for example as p⁺-doped polysilicon. The deposition methods used can be the same as those which have already been employed for the production of the layer sequence.

The counter-electrode 12 can, if appropriate, be structured and made contact with using customary methods of semiconductor technology.

FIG 2 shows a second exemplary embodiment of the capacitor, the capacitor being provided as a storage capacitor in a DRAM semiconductor arrangement. In this case, the carrier arrangement contains the selection transistors for the storage capacitance underneath the insulating layer 1. Insulated regions are formed in a substrate 20 with the aid of field oxide regions 21. An insulated region contains two selection transistors 30 and 40, which have a common source zone 22. Extending on both sides of the source zone 22 is the channel region, which is controlled by a gate 32 and 42, respectively, which is insulated on all sides in cross-section, as the word line. The transistors have respective drain regions

31 and 41 to the field oxide 21. Each drain of a memory cell, which is formed by a selection transistor and a capacitor, is connected to the electrode structure of a capacitor via a contact hole in the insulating layer. For example, the drain 31 of the transistor 30 is connected to the electrode 33 of a first capacitor K1, and the drain 41 of the transistor 40 is connected to the electrode 43 of the capacitor K2. In contrast with the exemplary embodiment of FIG 1, the electrode structure 33 and 43 is produced in that the contact holes 2 in the carrier layer 1 are first of all produced as self-aligned, overlapping contacts to the drain zones of the respective transistor, and that the p'-doped base layer is produced afterwards by means of conformal deposition, by which the contact hole is filled. In the exemplary embodiment of FIG 2, the source and drain zones 22, 31 and 41 are provided as p'-doped regions, corresponding to p-channel selection transistors. In the case of n-channel selection transistors, the contact hole 2 must have an intermediate layer having a metallicly conductive material, for example tungsten, tantalum, titanium, titanium nitride or a silicide. The word lines 23 for the next memory cells are arranged above the field oxide region 21. The word lines 23, 32 and 42 are preferably composed of heavily doped polysilicon or polycide. The source zone 22 makes contact with the bit line 50 with the aid of a self-aligned overlapping contact, the said bit line being composed of tungsten or polycide. In the said memory arrangement of FIG 2, all of the capacitors have a common counter-electrode 34, the so-called cell plate.

FIG 4 shows a further exemplary embodiment of the capacitor, which in this case is designed as a pot-shaped arrangement. An insulator layer 60 is first of all formed on a carrier 1 having a contact hole 2 filled, for example, with metal, which insulator layer is subsequently structured to produce an opening down to the carrier layer 1 or the filled contact hole 2. First of all, a base layer 61 made of heavily doped p-conducting

polysilicon and thereafter a layer sequence consisting alternately of a weakly doped and a heavily doped p-conducting layer are applied by means of conformal deposition in the manner portrayed. The weakly doped layers are designated as 62, 64 and 66, and the heavily doped layers as 63 and 65. The structure produced initially is one in which the layers 61 to 66 are situated one in the other in a pot-shaped manner, the layers applied later having smaller bottom and edge dimensions than the layers applied first. An opening 70 which reaches down to the base layer 61 is produced in the middle of the layer sequence by means of a mask technique and a following anisotropic etching step. As a result, the layer sequence is exposed in the bottom region, FIG 4a.

Afterwards, the opening 70 is at least partially filled with a heavily doped p-conducting material. This can be done in a manner corresponding to that for the layers 63 and 65. As an alternative, it is possible to select implantation at an angle given a sufficiently large opening in comparison with the edge height of the layers. As an alternative to producing an opening and filling the opening with p⁺-type material, it is possible to dope the region, defined by the mask opening, at the bottom of the layer sequence with p⁺-type atoms by means of a mask and one or more following implantation steps. It is preferable to provide a plurality of implantation steps in such a way that the doping maximum in each case lies in a p⁺-type layer region. A p⁺-type support is produced which is defined in the bottom region by the opening in the mask.

The p⁺-doped zones have a doping concentration of at least 10^{20} cm^{-3} , while the weakly doped p⁻-type zones 62, 64 and 66 have a doping concentration of at most 10^{19} cm^{-3} . A temperature step may follow, for example an RTA step, so that no diffusion can take place from the p⁺-doped layers. The structure is subsequently selectively and anisotropically etched in an alkaline etching solution. In the process, the p⁺-doped layers remain,

whereas the p'-doped layers are etched out. The selectivity of the etching process is in this case high enough to produce a support structure as in FIG 4b, which resembles a chandelier. In contrast with the exemplary embodiment of FIG 1, the middle, heavily doped p-conducting zone 70 is produced in such a way that the opening 70 is completely filled in the bottom region of the layer sequence. The deposition takes place conformally using the deposition methods which have already been mentioned, and is followed by structuring. The zone 71 therefore connects the layer sequence 61 to 66, which can be discerned in FIG 1, in the bottom region of the layer sequence.

In accordance with FIG 4c, a dielectric 73, for example in the form of an ONO dielectric, and a counter-electrode 74, for example made of p'-doped polysilicon, are subsequently produced by means of conformal deposition. The dielectric and counter-electrode 74 can subsequently be structured.

If desired, it is possible, as in FIG 2, to deposit the base layer by means of conformal deposition in the contact hole 2 as well. Furthermore, it is possible to arrange a capacitor of the type shown in FIG 4 in a silicon substrate and to connect the electrode structure at the trench edge to a semiconductor arrangement, for example a selection transistor of a DRAM arrangement. In this case, as in the case of known trench capacitors, the counter-electrode 74 can be designed as a continuous cell plate. If the capacitor is arranged as a trench capacitor in a silicon substrate, it suffices, in the case of a p-type substrate, to produce the base zone by doping the trench region more heavily. In an n-doped substrate, provision is made to insulate the heavily doped, p-conducting layer of the base layer 61 from the substrate by means of an insulating layer. A layer of this type can be formed from a silicon oxide and/or silicon nitride.



Patent Claims

1. Capacitor in a semiconductor arrangement, in particular a DRAM memory arrangement, having an electrode structure (10) containing a plurality of elements which are arranged at a distance from one another and are electrically interconnected by means of a connection structure (9), having a capacitor dielectric (11) and having a counter-electrode (12), characterized in that the elements of the electrode structure and the connection structure is [sic] composed completely of p-conducting material with a doping concentration of at least 10^{20} cm^{-3} .
2. Capacitor according to Claim 1, characterized in that the elements of the electrode structure are arranged one above the other or next to one another.
3. Capacitor according to Claim 1, characterized in that the elements of the electrode structure have a pot-shaped design.
4. Capacitor according to Claim 3, characterized in that the connection structure contains a supporting element (71) which is arranged within the pot-shaped electrode structure and is connected to a substrate and to the bottom part of the electrode structure.
5. Capacitor according to Claim 3 or 4, characterized in that a plurality of elements of the electrode structure are nested one in the other in a pot-shaped manner, and a bar-like supporting element (71) within the pot-shaped electrode structure connects the bottom parts of the elements to one another.
6. Method for the production of a capacitor in a semiconductor arrangement, having the following steps:
 - a base layer, which contains a heavily doped, p-conducting layer (3, 61), is produced on a surface of a carrier arrangement,
 - a layer sequence (4-7; 62-66) consisting alternately of a weakly doped and a heavily doped p-conducting layer is applied to a surface of the heavily doped, p-conducting layer (3, 61),



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- the layer sequence is structured by means of anisotropic etching, forming in the process at least one opening (8; 70) which reaches down to the base layer,
- a heavily doped p-conducting zone (9), which connects the layer sequence, is produced at least in one edge region of the opening,
- the weakly doped, p-conducting layers of the layer sequence are etched selectively with respect to the heavily doped p-conducting layer sequence,
- a capacitor dielectric (11) is conformally deposited, and
- a conductive layer (12) is conformally deposited on the capacitor dielectric.

7. Method according to Claim 6, characterized in that the base layer is produced by means of a heavily doped, p-conducting layer (3, 61) which is produced by areal doping of a semiconductor zone or by deposition of a doped semiconductor material.

8. Method according to Claim 7, characterized in that the base layer is produced by means of an oxide layer and/or a nitride layer which is applied before the heavily doped, p-conducting layer.

9. Method according to one of Claims 6 to 8, characterized in that the base layer is applied to a planarized surface of a carrier layer.

10. Method according to one of Claims 6 to 9, characterized in that the heavily doped, p-conducting zone in the opening (8) is effected by implanting ions at an oblique angle into the layer sequence consisting of weakly doped and heavily doped p-conducting layers.

11. Method according to Claim 10, characterized in that boron fluoride ions are implanted.

12. Method according to one of Claims 6 to 9, characterized in that the heavily doped, p-conducting zone in the opening (70) is produced by applying a heavily doped, p-conducting material.

13. Method according to one of Claims 6 to 12, characterized in that a temperature step takes place after the production of the heavily doped, p-conducting



zone.

14. Method according to one of Claims 6 to 13, characterized in that the selective etching takes place isotropically by means of an alkaline etchant.

15. Method according to one of Claims 6 to 13, characterized in that an ethylenediamine/pyrocatechol solution or a potassium hydroxide solution is used as the etchant.

16. Method according to one of Claims 6 to 15, characterized in that silicon oxide and/or silicon nitride is conformally deposited as the capacitor dielectric (11).

17. Method according to one of Claims 6 to 16, characterized in that the layer sequence is applied one above the other or next to one another.

18. Method according to one of Claims 6 to 16, characterized in that the layer sequence is nested one in the other in a pot-shaped manner.

19. Method according to one of Claims 6 to 18, characterized in that a counter-electrode (12) made of heavily doped, p-conducting material is produced on the capacitor dielectric (11).

20. Method according to either of Claims 1 and 2, characterized in that the connection structure (9) is arranged at least at one edge of the elements and extends transversely with respect to the surface of the elements.

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