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(54) ELECTRONIC TIMER DEVICE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 31-1 6-chome Kameido, Koto-ku, Tokyo, Japan do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:

5 This invention relates to electronic timer devices.

According to the present invention there is provided an electronic timer device comprising: timekeeping means for producing an electronic timing signal; memory means for memorising time periods relating to at least two events and connected to receive said timing signal; selecting means for selecting the memory means appropriate to the event to be timed; and digital display means
10 for displaying the remainder of each time period of the event being timed.

Preferably the timer device includes alarm means for producing an alarm when each time period has elapsed.

The timer device may include an electro-optical display device for displaying an indication representative of the event being timed.

15 In the preferred embodiment the memory means comprises a plurality of counters each of which memorises a respective predetermined time period, control means being provided to control operation of some of the counters in dependence upon the event being timed.

Each counter may be a down-counter.

The control means may be a shift register.

20 The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figures 1 and 2 are external views of one embodiment of an electronic timer device according to the present invention, and

Figure 3 is a block diagram of the timer device of Figures 1 and 2.

25 Figures 1 and 2 are external views of one embodiment of an electronic timer device according to the present invention. A case 1 has a substantially annular portion 2 within which is located a display device 3. The display device 3 is composed, for example, liquid crystal display elements, or light emitting diodes and consists of a 4-digit display portion 4 for displaying time digitally and a display portion 5 which displays an indication representative of an event, or game being timed. The
30 case 1 carries a manually operable push-button 6 which is operated to start counting of time, a manually operable push-button 7 operated to stop counting of the time, a manually operable change-over switch button 8 which selects the event to be timed, and a manually operable push-button 9 to reset the timer device. The timer device of Figures 1 and 2 is designed for timing basketball and association football, although it may be modified to time rugby football and other
35 games and events. In Figure 1 the display portion 5 displays an indication representative of basketball to indicate that basketball is being timed and in Figure 2 the display portion 5 displays an indication representative of association football, to indicate that association football is being timed.

Referring now to Figure 3, the timer device of Figures 1 and 2 have an oscillator circuit 10 which employs, for example, a quartz vibrator and generates a standard time signal of relatively
40 high frequency. The standard time signal is frequency divided by a frequency divider 11 which

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produces a pulsiform 1-second signal i.e. a signal consisting of 1 pulse each second. The 1-second signal is fed to a clock terminal CL of each of three counters 13, 14, 15 via a switch 12. The switch 12 is an ON-OFF switch controlled by the push-button 7 and normally is in the ON or closed condition.

- 5 The counters 13, 14, 15 are respectively provided with memory functions of 40 minutes, 20 minutes and 10 minutes. Thus the counter 13 counts in the 60 and 40 counting modes, the counter 14 counts in the 60 and 20 counting modes, and the counter 15 counts in the 60 and 10 counting modes. The 60 counting modes relate to the counting of seconds and the 40, 20 and 10 counting modes relate to the counting of minutes. The counters, 13, 14, 15 are each down-counters
10 the contents of which are displayed digitally by the display portion 4 of the display device 3 through a gate circuit 16 and a decoder/driver circuit 17.

A switch 18 is controlled by the push-button 6 and is normally in the OFF or open condition and goes to the ON or closed condition whenever the push-button 6 is depressed.

- One contact of the switch 18 is connected to a voltage supply terminal 19, the electric potential
15 of which corresponds to logic 1. The other contact of the switch 18 is earthed to a potential which corresponds to logic 0 through a resistor 20 and is also connected to one input terminal of an OR circuit 21. The OR circuit 21 has four input terminals, the other three input terminals being supplied with signals from the counters 13, 14, 15.

- The output from the OR circuit 21 is fed to a clock terminal CL of shift register 22, to a
20 control terminal of an alarm device 23, and to one input terminal of a two-input AND circuit 24. The shift register 22 counts in the four counting mode. An output terminal Q₄ of the shift register 22 is connected to the other input terminal of the AND circuit 24 and to one input terminal of an OR circuit 28, the other input terminal of which is connected to an output terminal Q₂ of the shift register 22. The output terminal of the AND circuit 24 is connected to a reset
25 terminal R of the shift register 22 via a two-input OR circuit 25. The shift register 22 responds to a reset pulse applied to the reset terminal R and the output terminals Q₁ - Q₄ become 1,0,0,0. The alarm device 23 which may be a buzzer generates and alarm when an output signal from the OR circuit 21 is logic 1.

- The other input terminal of the OR circuit 25 is connected to one terminal of a switch 26
30 which is earthed to a potential which corresponds to logic 0 through a resistor 27. The other terminal of the switch 16 is connected to the voltage supply terminal 19. The switch 26 is controlled by the push-button 9 and is normally in the OFF or open condition and is in the ON or closed condition when the push-button 9 is depressed. When the switch 26 is in the ON or closed condition a reset pulse of logic 1 is produced by the OR circuit 25 to reset the shift
35 register 22.

- As mentioned above, the output terminals Q₂, Q₄ of the shift register 22 are fed to the OR circuit 28, the output of which is fed to one input terminal of each of two two-input NAND circuits 29, 30. Between the other input terminals of the NAND circuits 29, 30 is connected an
40 inverter 31. The input side of the inverter 31 is connected to one terminal switch 32 which is earthed to a potential corresponding logic 0 via a resistor 32. The other terminal of the switch 32 is connected to the voltage supply terminal 19. The switch 32 is an ON - OFF switch controlled by the change-over switch button 8. When the switch 32 is in the ON or closed condition, the display portion 5 displays the indication representative of basket-ball and when the switch 32 is in the OFF or open conditions, the display portion 5 displays the indication representative of
45 association-football. The input side and the output side of the inverter 31 are connected to a driver circuit 35 the output signal of which is fed to the display portion 5 of the display device 3. When the switch 32 is in the ON or closed position, the input side of the inverter 31 becomes logic 1 and the indication representative of basket-ball is displayed by the display portion 5 through the driver circuit 35 as shown in Figure 1. When the switch 32 is in the OFF or open
50 condition, the output side of the inverter 31 is logic 1 and the indication representative of association football is displayed by the display portion 5 as shown in Figure 2.

- An output terminal of NAND circuit 29 is connected to a reset terminal R of the counter 13 and an output terminal of the NAND circuit 30 is connected to a reset terminal R of the counter 14. The output terminal Q₃ of the shift register 22 is connected to a reset terminal R of the
55 counter 15 through an inverter 34.

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The operation of the timer device illustrated in the drawings will now be described.

When the switch 32 is operated to the ON or closed condition, an indication representative of basketball is displayed by the display portion 5 as shown in Figure 1. If the switch 18 is momentarily operated to the ON or closed condition when the event to be timed starts, a clock pulse is fed to the clock terminal CL of the shift register 22 through the OR circuit and the output terminal Q₂ of the shift register 22 becomes logic 1. As a result, both of the input terminals of the NAND circuit 30 become logic 1 and the output terminal of the NAND circuit 30 becomes logic 0 and resetting of the counter 14 is released. Accordingly, the counter 14 counts the pulses of the one-seconds signal fed to the clock terminal CL thereof from the divider 11. When the resetting of the counter 14 is released the display portion 14 displays 20:00 i.e. 20 minutes representing the time of the first half of a basketball game through the gate circuit 16 and the decoder/driver circuit 17. As time elapses, the remainder of the time period is displayed by the display portion 4.

In the case of a time out or where it is desired to temporarily stop the counter 14, the switch 12 is moved to the OFF or open condition, so that the one-seconds signal is no longer fed to the counter 14. When the event is restarted, the switch 12 is moved to the ON or closed condition and the remainder of the time period is once more displayed by the display portion 4. When a half-time break is reached, after 20 minutes in the case of basketball, the display portion 4 displays 00:00 and a signal produced from the counter 14 is fed to the shift register 22 through the OR circuit 21 and the output terminal Q₃ of the shift register 22 becomes logic 1. At this time an output signal from the OR circuit 21 is applied to the alarm generating circuit 23 and the alarm sounds, providing an indication of the termination of the first half of the event. Simultaneously, with the output terminal Q₃ of the shift register 22 becoming logic 1, the resetting of the counter 15 is released and the counter 15 starts counting the pulses of the one-second signal. After 10 minutes has elapsed, representing half-time break in the case of basketball the counter 14 is reset. The contents of the counter 15 are displayed digitally by the display portion 4 during the half-time break and when the half-time break is over, a borrow signal from the counter 15 is fed to the clock terminal CL of the shift register 22 to cause the output terminal Q₄ to become logic 1. The counter 15 is thus reset and the resetting of the counter 14 is released. When the second half of the event is over, a signal from the counter 14 is fed to the shift register 22. Simultaneously, the output terminal of the AND circuit 24 becomes logic 1 and a reset pulse is fed to the reset terminal R of the shift register 22 through the OR circuit 25. Thus the output terminal Q₁ of the shift register 22 becomes logic 1, and the event is over. The shift register 22 may be reset at any time if the switch 26 is moved to the ON or closed condition and counting of the time ceases.

In the case where the event being timed is association football, the switch 32 is in the OFF or open condition. The game of association football consists of two halves of 40 minutes each and a 10 minutes half-time break. The counter 13 and the counter 15 operate similarly to the case of basketball responded to the output from the shift register 22, whilst, as shown in Figure 2, an indication representative of association football is displayed by the display portion 5.

As mentioned above, the timing of basketball, or association football, is selected by operation of the switch 32 and the time periods the first half, half-time break and second half, of the event are automatically counted. It is convenient to a user of the timer device that display portion 4 displays the remainder of each time period. An alarm is produced by the alarm device 23 whenever the time displayed by the display portion 4 is 00:00.

The illustrated embodiment is suitable for basketball and association football, but it is possible to construct a timer device which can be used for other events, or more than two events by altering the counting capacity of the counters 12, 13, 14 or increasing the number of counters or the number of bits of the shift register, or altering the control system of the outputs.

With the timer device illustrated above, the time periods of an event can be counted without error and the remainder of each time period can be read directly. The alarm device produces an audible sound when the time displayed by the display portion 4 is 00:00 so that there is no possibility that the end of each half, and half-time is overlooked. Furthermore, any indication representative of the event being timed is displayed to prevent, or reduce the possibility of mis-selection.

WHAT WE CLAIM IS:

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The operation of the timer device illustrated in the drawings will now be described.

When the switch 32 is operated to the ON or closed condition, an indication representative of basketball is displayed by the display portion 5 as shown in Figure 1. If the switch 18 is momentarily operated to the ON or closed condition when the event to be timed starts, a clock pulse is fed to the clock terminal CL of the shift register 22 through the OR circuit and the output terminal Q₂ of the shift register 22 becomes logic 1. As a result, both of the input terminals of the NAND circuit 30 become logic 1 and the output terminal of the NAND circuit 30 becomes logic 0 and resetting of the counter 14 is released. Accordingly, the counter 14 counts the pulses of the one-seconds signal fed to the clock terminal CL thereof from the divider 11. When the resetting of the counter 14 is released the display portion 14 displays 20:00 i.e. 20 minutes representing the time of the first half of a basketball game through the gate circuit 16 and the decoder/driver circuit 17. As time elapses, the remainder of the time period is displayed by the display portion 4.

In the case of a time out or where it is desired to temporarily stop the counter 14, the switch 12 is moved to the OFF or open condition, so that the one-seconds signal is no longer fed to the counter 14. When the event is restarted, the switch 12 is moved to the ON or closed condition and the remainder of the time period is once more displayed by the display portion 4. When a half-time break is reached, after 20 minutes in the case of basketball, the display portion 4 displays 00:00 and a signal produced from the counter 14 is fed to the shift register 22 through the OR circuit 21 and the output terminal Q₃ of the shift register 22 becomes logic 1. At this time an output signal from the OR circuit 21 is applied to the alarm generating circuit 23 and the alarm sounds, providing an indication of the termination of the first half of the event. Simultaneously, with the output terminal Q₃ of the shift register 22 becoming logic 1, the resetting of the counter 15 is released and the counter 15 starts counting the pulses of the one-second signal. After 10 minutes has elapsed, representing half-time break in the case of basketball the counter 14 is reset. The contents of the counter 15 are displayed digitally by the display portion 4 during the half-time break and when the half-time break is over, a borrow signal from the counter 15 is fed to the clock terminal CL of the shift register 22 to cause the output terminal Q₄ to become logic 1. The counter 15 is thus reset and the resetting of the counter 14 is released. When the second half of the event is over, a signal from the counter 14 is fed to the shift register 22. Simultaneously, the output terminal of the AND circuit 24 becomes logic 1 and a reset pulse is fed to the reset terminal R of the shift register 22 through the OR circuit 25. Thus the output terminal Q₁ of the shift register 22 becomes logic 1, and the event is over. The shift register 22 may be reset at any time if the switch 26 is moved to the ON or closed condition and counting of the time ceases.

In the case where the event being timed is association football, the switch 32 is in the OFF or open condition. The game of association football consists of two halves of 40 minutes each and a 10 minutes half-time break. The counter 13 and the counter 15 operate similarly to the case of basketball responded to the output from the shift register 22, whilst, as shown in Figure 2, an indication representative of association football is displayed by the display portion 5.

As mentioned above, the timing of basketball, or association football, is selected by operation of the switch 32 and the time periods the first half, half-time break and second half, of the event are automatically counted. It is convenient to a user of the timer device that display portion 4 displays the remainder of each time period. An alarm is produced by the alarm device 23 whenever the time displayed by the display portion 4 is 00:00.

The illustrated embodiment is suitable for basketball and association football, but it is possible to construct a timer device which can be used for other events, or more than two events by altering the counting capacity of the counters 12, 13, 14 or increasing the number of counters or the number of bits of the shift register, or altering the control system of the outputs.

With the timer device illustrated above, the time periods of an event can be counted without error and the remainder of each time period can be read directly. The alarm device produces an audible sound when the time displayed by the display portion 4 is 00:00 so that there is no possibility that the end of each half, and half-time is overlooked. Furthermore, any indication representative of the event being timed is displayed to prevent, or reduce the possibility of mis-selection.

WHAT WE CLAIM IS:





1. An electronic timer device comprising: timekeeping means for producing an electronic timing signal; memory means for memorising time periods relating to at least two events and connected to receive said timing signal; selecting means for selecting the memory means appropriate to the event to be timed; and digital display means for displaying the remainder of each time period of the event being timed.
2. A timer device as claimed in claim 1 including alarm means for producing an alarm when each time period has elapsed.
3. A timer device as claimed in claim 1 or 2 including an electro-optical display device for displaying an indication representative of the event being timed.
- 10 4. A timer device as claimed in any preceding claim in which the memory means comprises a plurality of counters each of which memorises a respective predetermined time period, control means being provided to control operation of some of the counters in dependence upon the event being timed.
5. A timer device as claimed in claim 4 in which each counter is a down-counter.
- 15 6. A timer device as claimed in claim 4 or 5 in which the control means is a shift register.
7. An electronic timer device substantially as herein described with reference to and as shown in the accompanying drawings.

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