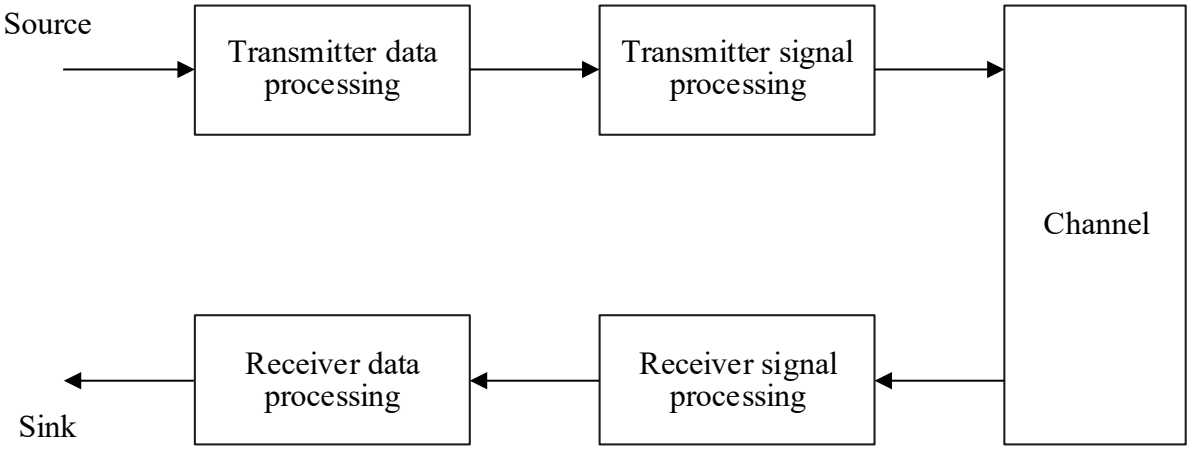

Source
Transmitter data processing
Transmitter signal processing
Channel
Receiver data processing
Receiver signal processing
Sink

FIG. 1

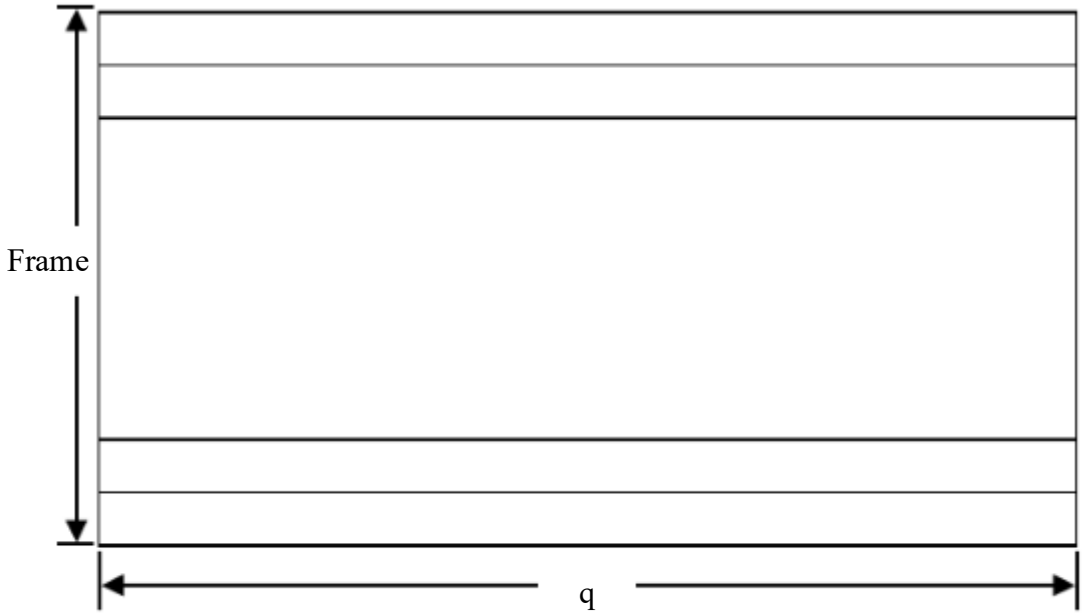

Frame
q

FIG. 2

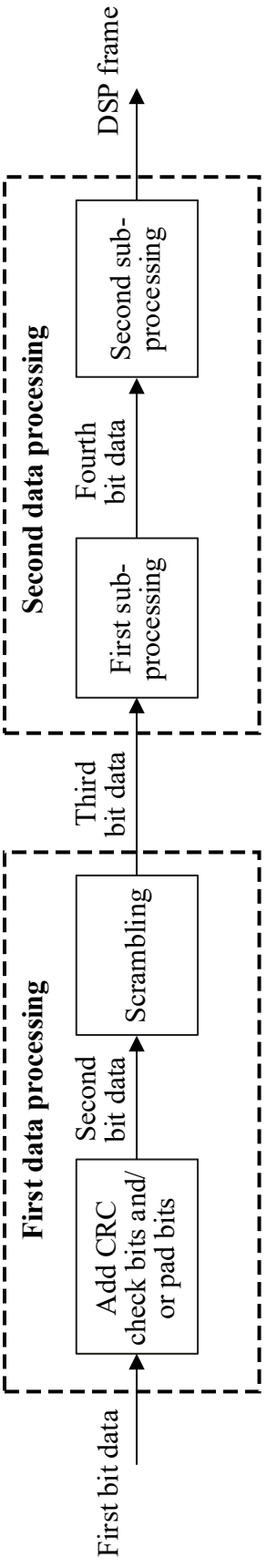

First bit data
First data processing
Add CRC check bits and/ or pad bits
Second bit data
Scrambling
Third bit data
Second data processing
First sub-processing
Fourth bit data
Second sub-processing
DSP frame

FIG. 3

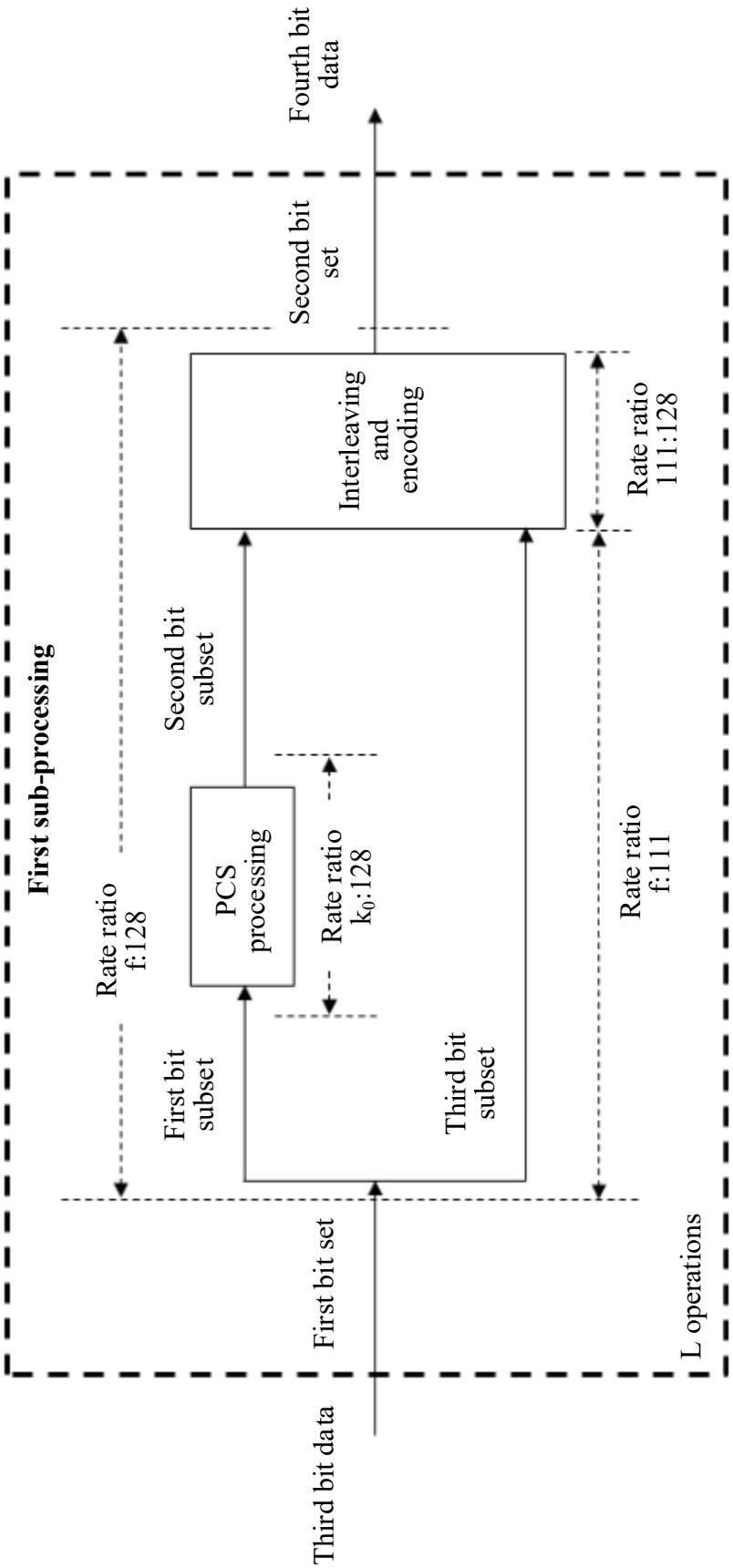

Fourth bit data
Second bit set
Interleaving and encoding
Rate ratio 111:128
First sub-processing
Second bit subset
PCS processing
Rate ratio k_0:128
Rate ratio f:128
Rate ratio f:111
First bit subset
Third bit subset
First bit set
L operations
Third bit data

FIG. 4

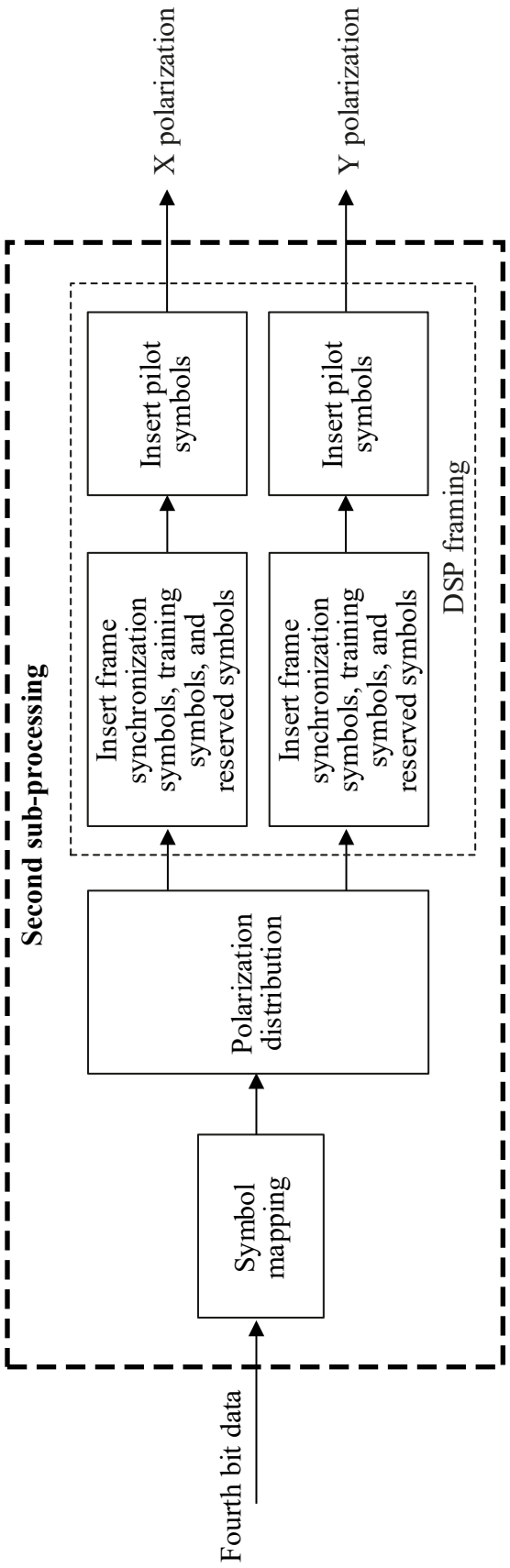

Fourth bit data
Second sub-processing
Symbol mapping
Polarization distribution
DSP framing
Insert frame synchronization symbols, training symbols, and reserved symbols
Insert frame synchronization symbols, training symbols, and reserved symbols
Insert pilot symbols
Insert pilot symbols
X polarization
Y polarization

FIG. 5a

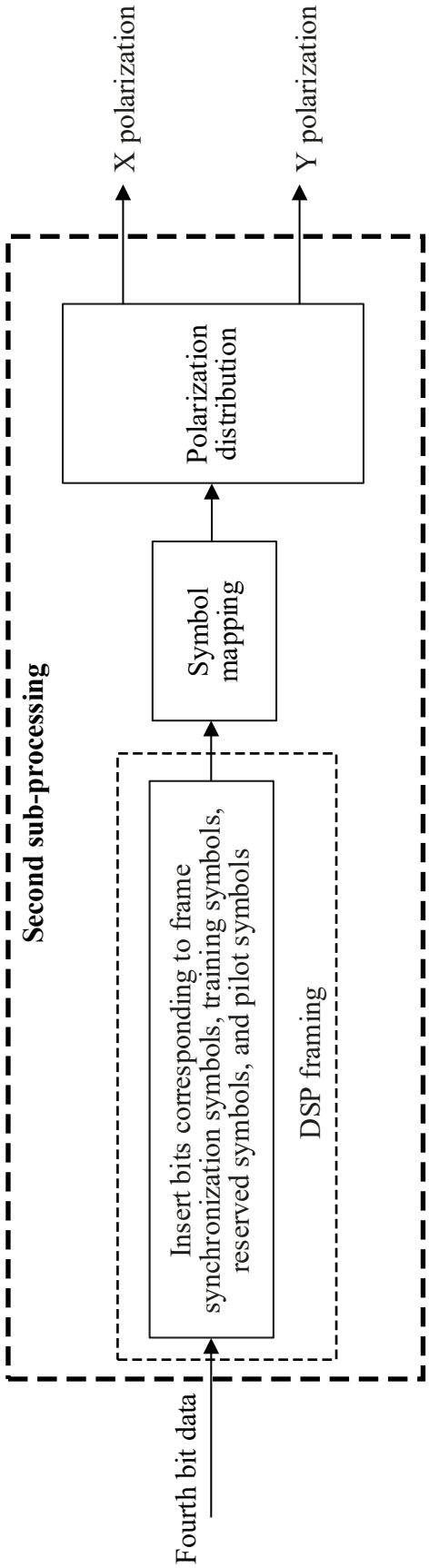

Fourth bit data
Second sub-processing
DSP framing
Insert bits corresponding to frame synchronization symbols, training symbols, reserved symbols, and pilot symbols
Symbol mapping
Polarization distribution
X polarization
Y polarization

FIG. 5b

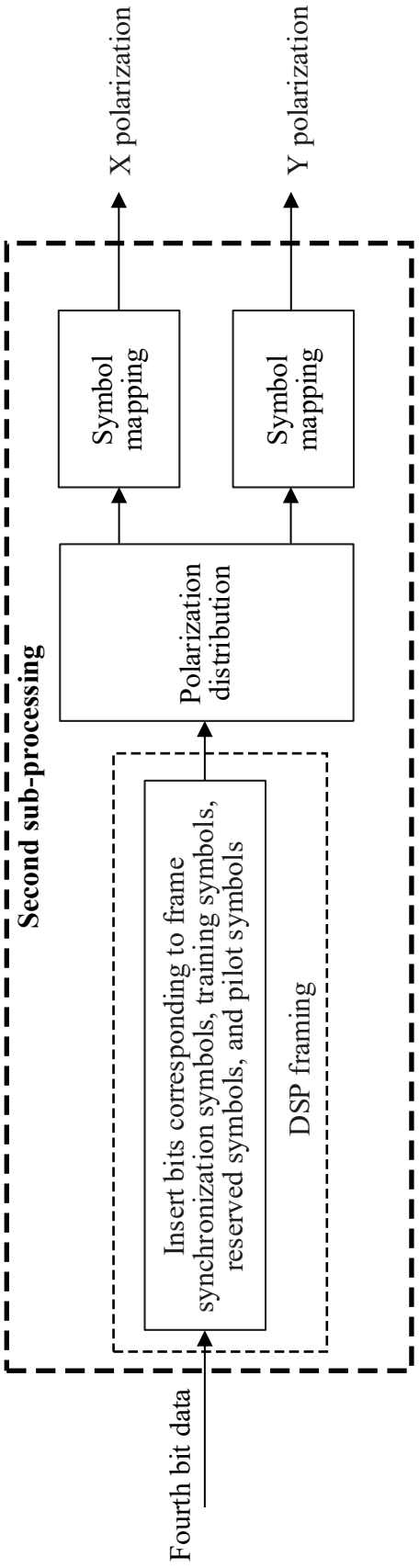

Fourth bit data
Second sub-processing
DSP framing
Insert bits corresponding to frame synchronization symbols, training symbols, reserved symbols, and pilot symbols
Polarization distribution
Symbol mapping
Symbol mapping
X polarization
Y polarization

FIG. 5c

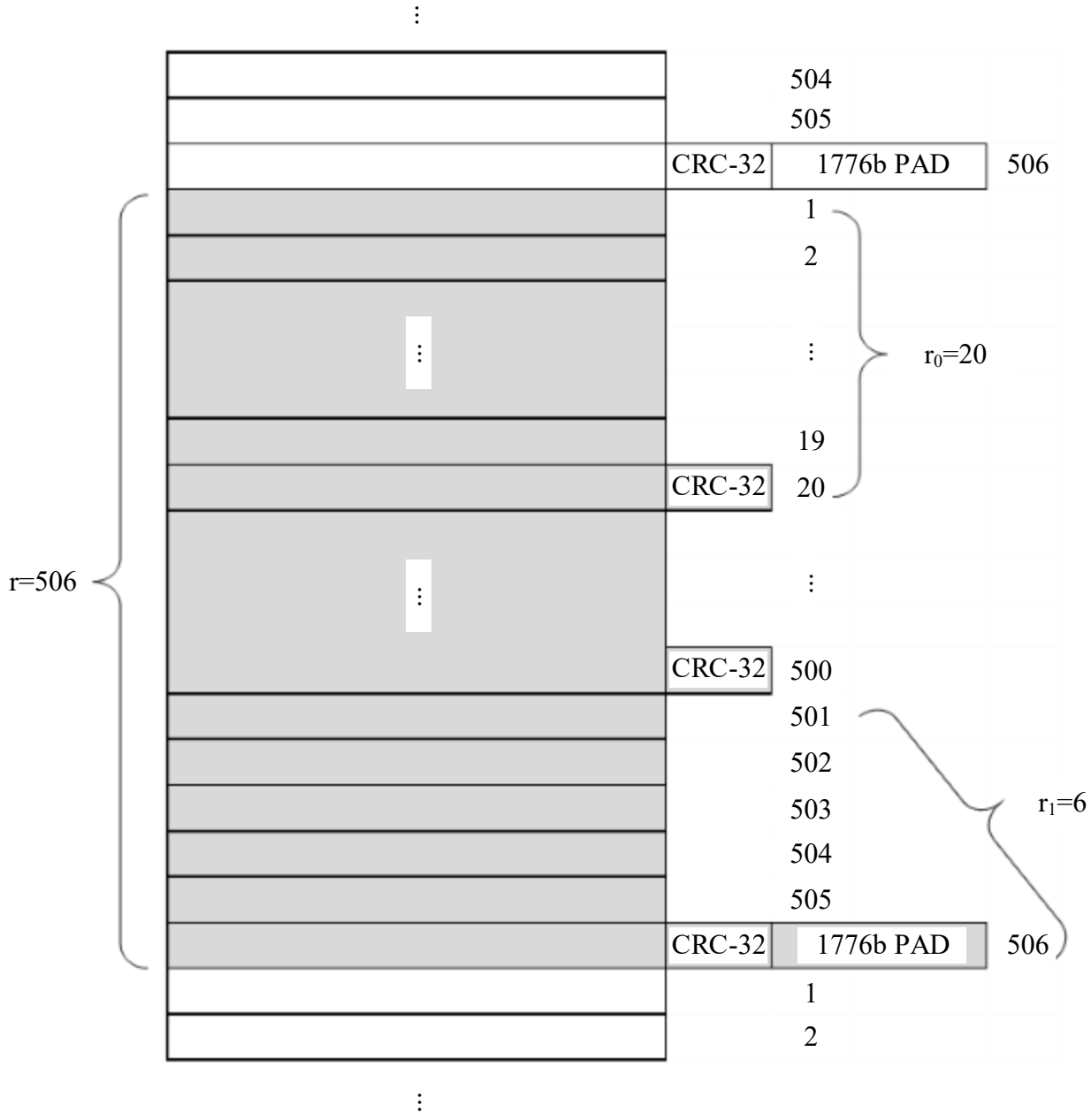

504
505
CRC-32
1776b PAD
506
1
2
r_0=20
19
CRC-32
20
r=506
CRC-32
500
501
502
503
504
505
r_1=6
CRC-32
1776b PAD
506
1
2

FIG. 6

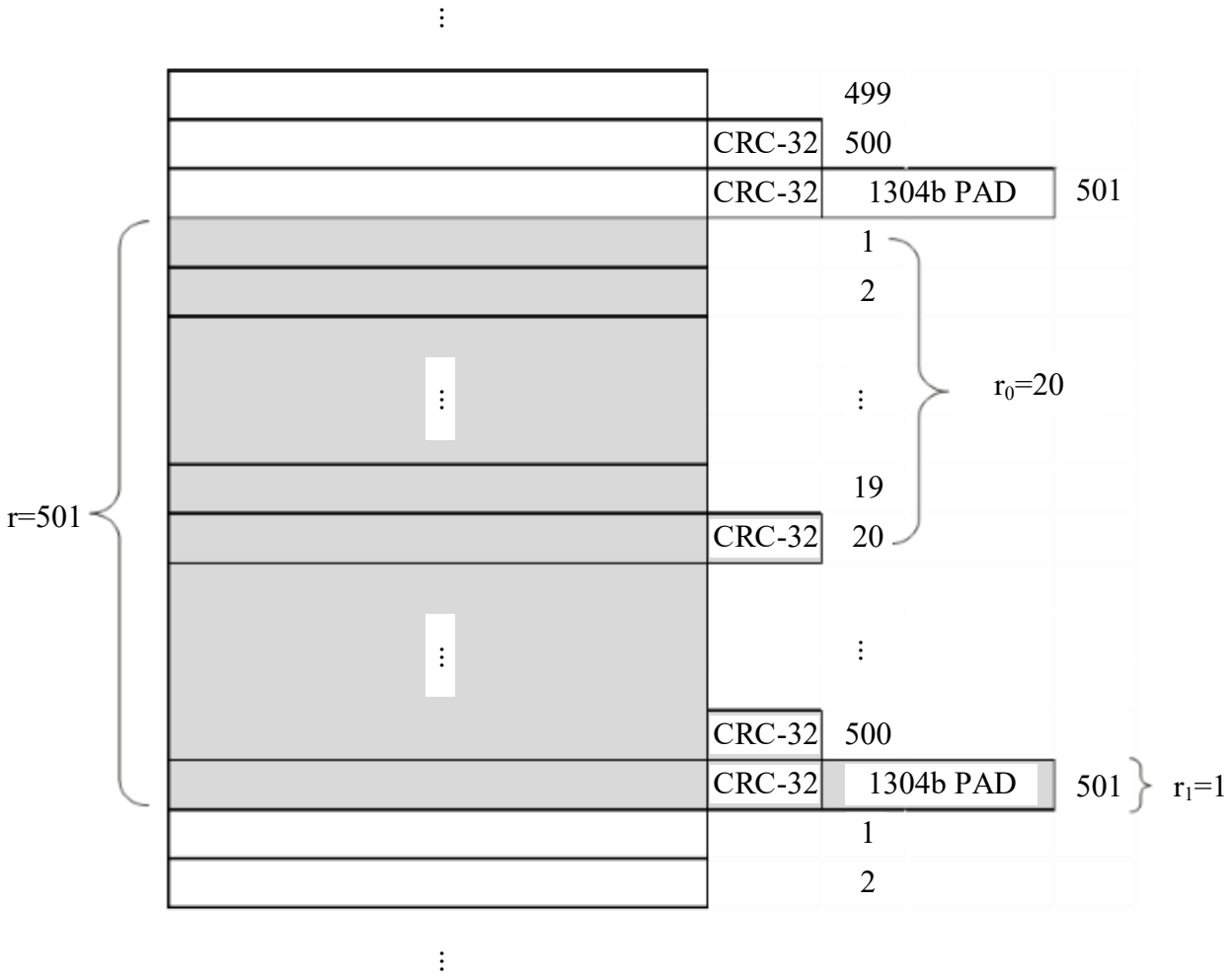

499
CRC-32
500
CRC-32
1304b PAD
501
1
2
r=501
r0=20
19
CRC-32
20
CRC-32
500
CRC-32
1304b PAD
501
r1=1
1
2

FIG. 7

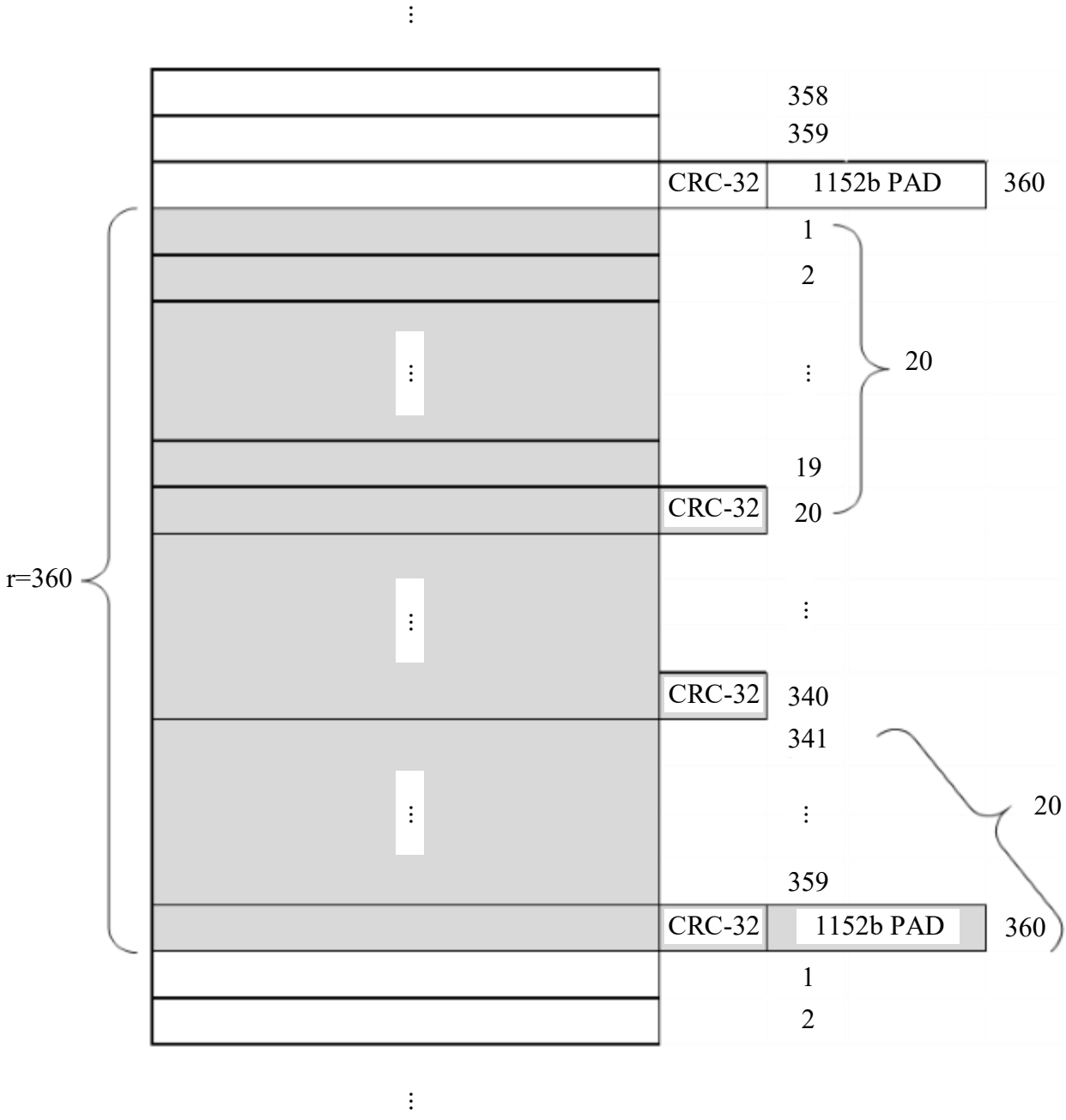

358
359
CRC-32
1152b PAD
360
1
2
20
19
CRC-32
20
r=360
CRC-32
340
341
20
359
CRC-32
1152b PAD
360
1
2

FIG. 8

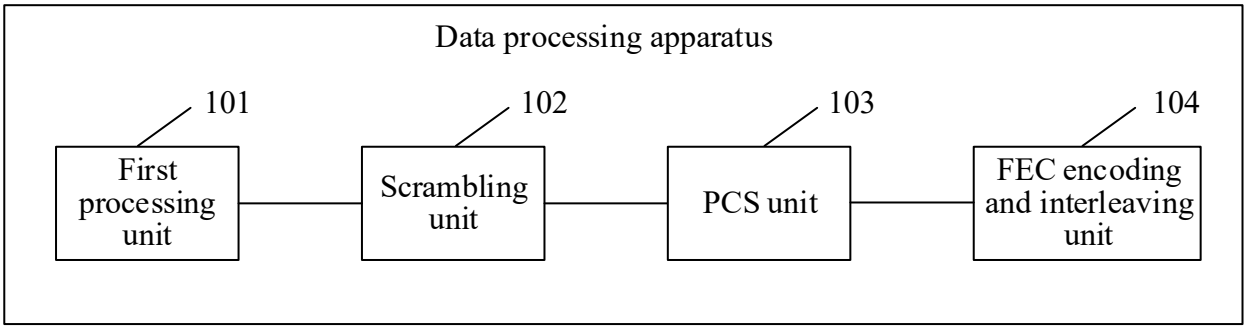

Data processing apparatus
101
First processing unit
102
Scrambling unit
103
PCS unit
104
FEC encoding and interleaving unit

FIG. 9

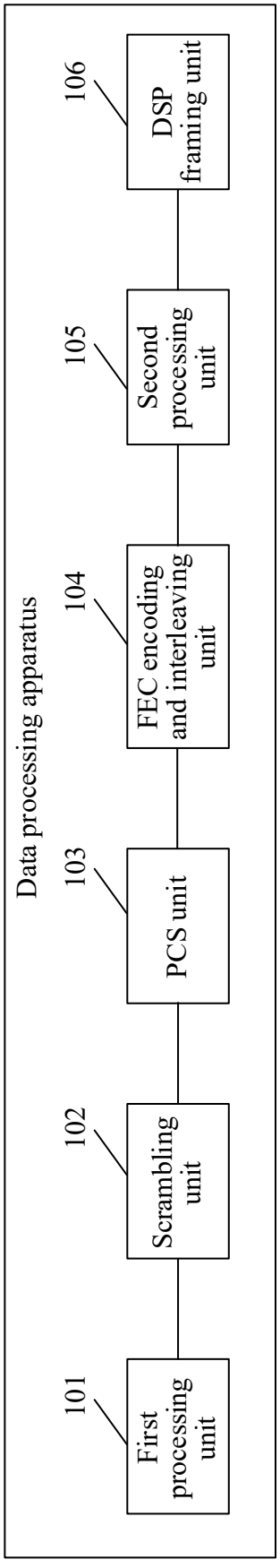

Data processing apparatus
101
First processing unit
102
Scrambling unit
103
PCS unit
104
FEC encoding and interleaving unit
105
Second processing unit
106
DSP framing unit

FIG. 10

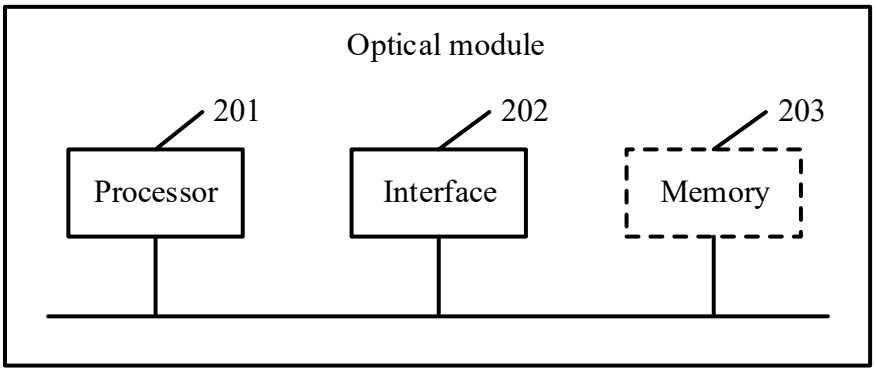

Optical module
201
202
203
Processor
Interface
Memory

FIG. 11

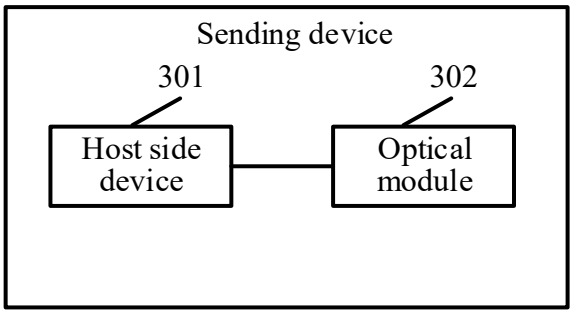

Sending device
301
302
Host side device
Optical module

FIG. 12