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(54) CAMERAS HAVING ELECTRONIC EXPOSURE CONTROL

(71) We, AGFA-GEVAERT AKTIENGESELLSCHAFT, a body corporate organised according to the Laws of Federal Republic of Germany, of Leverkusen, Federal Republic of Germany, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a camera having electronic exposure control means comprising means for determining the brightness of the prevailing illumination including a photo-sensitive element, a diaphragm aperture control circuit and an exposure time control circuit.

It is an object of the invention to provide an improved camera of the type referred to above in which the electronic exposure control means gives an exposure time-diaphragm aperture programme control using only one photosensitive element. Furthermore it should be possible to construct a substantial proportion of the exposure control means using integrated circuitry.

Using one photosensitive element for an exposure time-diaphragm-programme control requires that a signal determined by the prevailing illumination for controlling the diaphragm aperture must be stored.

The invention provides a camera including a photo-sensitive element which is arranged to receive ambient light and to provide an electrical signal which depends on the light received, a first threshold detector which is arranged to receive the electrical signal and to provide an output signal which changes value abruptly as the electrical signal crosses a first threshold value, a second threshold detector which is arranged to receive the electrical signal and to provide an output signal which changes value abruptly as the electrical signal crosses a second threshold value, a bistable device electronic store which is arranged to

receive the output signals from the threshold detectors and to store digital information corresponding to the combined threshold detector outputs, a diaphragm aperture control circuit which is connected to the output terminals of the bistable device electronic store and is arranged to provide set aperture adjustments appropriate to the ambient lighting level and in accordance with the contents of the bistable device electronic store, and an exposure time control circuit which includes the photo-sensitive element and a switch which is arranged to initiate exposure and to freeze the contents of the bistable device electronic store when operated.

In an embodiment of the invention, the bistable device electronic store includes two gated bistable devices having data input terminals and gate terminals, the data input terminals of which are connected to the output terminals of the respective threshold detectors, and the gate terminals of which are connected to the exposure initiation switch.

Preferably, the diaphragm aperture control circuit provides two set aperture adjustments, and one of the set aperture adjustments alters the exposure time control circuit by introducing an auxiliary capacitor into the said circuit. Preferably one of the set aperture adjustments is appropriate to an average ambient lighting level, and the other set aperture adjustment is appropriate to a high ambient lighting level. In conditions of low ambient lighting a small aperture which is the one appropriate to a high ambient lighting level is used to give good depth of focus.

The diaphragm aperture control circuits may include an EXCLUSIVE-OR gate, the input terminals of which are connected to the output terminals of the bistable device electronic store.

In an embodiment of the invention, the first and second threshold detectors are provided by first and second operational

amplifiers, the first operational amplifier having its inverting input terminal connected to a first potential divider which sets the first threshold value, and the second operational amplifier having its inverting terminal connected to a second potential divider which sets the second threshold level.

Preferably, the photo-sensitive element is arranged in series with a resistor and a battery when the exposure initiation switch is closed, and the photo-sensitive element is arranged in series with a main capacitor and the battery when the exposure initiation switch is open. The exposure time control circuit may include a threshold switch having its input terminal connected to the main capacitor and having its output terminal connected to a shutter-operating relay, and a transistor which is also connected to the shutter-operating coil and is arranged to hold the shutter closed when the exposure initiation switch is closed.

An embodiment of the invention may include a first electroluminescent display device which is connected to a part of the bistable device electronic store and is arranged to be energised when that part of the bistable device electronic store includes a logical "1", and a second electroluminescent display device which is connected to the said part of the bistable device electronic store and is arranged to be energised when that part of the bistable device electronic store includes a logical "0".

One form of electronic exposure control means for a camera constructed in accordance with the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figures 1a and 1b are a circuit diagram of the control means, and

Figure 2 is a diagram of one component of the control means.

Referring now to Figure 1a of the accompanying drawings, a power supply 1 is connected to the circuit by a contact 2 which remains closed until the end of an exposure control process, and a contact 3 which is closed when the camera is brought into use. Connected in series across the power supply 1 are a photoresistor 7, a capacitor 8 and a variable resistor 12. A transistor 9 is arranged across the capacitor 8 so that when it is switched through it will bridge the capacitor, and a further capacitor 11 and a switch 10 are arranged in parallel with the capacitor 8. A further transistor 13 is arranged in parallel with the resistor 12 so that when it is switched through it will bridge the resistor. Connected to the tapping between the photoresistor 7 and the capacitor 8 is the input of a trigger device 4, the output of which is connected to a shutter control magnet 5. The output of the trigger

device 4 is also connected to the collector of a transistor 6 the base of which is connected to the base of the transistor 9. A potential divider formed of two resistors 15 and 16 is connected across the power supply 1 by a switch 14 which is, in its normal state closed. The tapping between the two resistors 15 and 16 is connected to the base of the transistor 9 and this transistor 9 is switched when the potential divider 15 and 16 is connected in. Also connected to the tapping between the two resistors 15 and 16 is the base of a transistor 17, the collector of which is connected to the base of the transistor 13 and to a resistor 18 and which together with the resistor 18 inverts the signal applied to the base of the transistor 13.

The tapping between the variable resistor 12 and the capacitors 8 and 11 is connected to the non-inverting input of an operational amplifier 19. The inverting input of the operational amplifier 19 is connected to a potential divider comprising two resistors 20 and 21. The output of the operational amplifier 19 is connected through a resistor 22 to the positive pole of the power supply 1. The resistors 20 and 21 are so matched that the operational amplifier 19 is blocked when the resistance of the photoresistor corresponds to a brightness above a lower usable value, and is switched through when the brightness falls below this value.

The output of the operational amplifier 19 is also connected to the SET input 23 of a D-flip-flop 24. A tapping taken between the resistor 15 and the switch 14 is connected to the clock input 25 of the D-flip-flop 24. An inverting output of the D-flip-flop 24 is indicated by 26.

Referring now to Fig. 2, the D-flip-flop 24 comprises four NAND-gates 27, 28, 29 and 30. The SET input 23 is connected to the first input of a NAND-gate 27, the second input of which is connected to the clock input 25. The output of the NAND-gate 27 is connected to the input of a NAND-gate 28 the second input of which is connected to the clock input 25. The output of the NAND-gate 27 is also connected to the first input of a NAND-gate 29. The output of the NAND-gate 28 is connected to the second input of a NAND-gate 30, the first input of which is connected to the output of the NAND-gate 29. The second input of the NAND-gate 29 is connected to the output of the NAND-gate 30. The output of the NAND-gate 30 also represents the inverting output 26 of the D-flip-flop.

As a result of the above-mentioned linkage of the four NAND-gates 27 to 30 the switching and storage behaviour of the D-flip-flop is as follows: Assuming that there is a potential "L" at the clock input 25, and that a SET signal having potential "O" is applied to the input 23, then a potential "L" is

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appears at the inverting output 26. If a potential "L" is now applied at the SET input 23, there is a potential "O" at the output 26. When there is a clock potential "L" present at the input 25, the inverse of the SET potential applied to the input 23 appears at the output 26. If the clock potential at the input 25 is reduced to "O", this has no effect on the output 26. If at the same time the potential at the SET input 23 is altered, this too has no effect at the output 26. Thus the potential at the output 26 remains stored until the clock potential at the input 25 is returned to the value "L".

Referring again to Fig. 1a, the output 26 of the D-flip-flop 24 is connected through a resistor 31 to the base of a transistor 32, connected between the collector and emitter of which are a light emitting diode 33 and a resistor 34 in series. The light emitting diode 33 when lit gives an indication that the prevailing illumination will give adequate exposure and emits green light. The output 26 of the D-flip-flop 24 is also connected through a resistor 35 to the base of a transistor 36, the emitter of which is connected to the negative pole of the power supply 1. A resistor 37 is connected between the collector of the transistor 36 and the positive pole of the power supply 1. The collector of the transistor 36 is also connected to the base of a transistor 38, connected between the collector and emitter of which are luminous diode 39 and a resistor 40 in series. The luminous diode 39 which is red, gives an indication that the prevailing illumination is inadequate for exposure. The output 26 is also connected to a terminal 41. The negative pole of the power supply 1 is connected to a terminal 42 and the positive pole to a terminal 43.

The tapping between the resistor 12 and the two capacitors 8 and 11 is connected to the non-inverting input of an operational amplifier 44, the inverting input of which is connected to a potential divider comprising resistors 45, 46 and 47. A resistor 48 is connected to the output circuit of the operational amplifier 44.

The resistors 45, 46 and 47 are so matched with one another, that when the brightness of the prevailing illumination is above average the operational amplifier 44 is blocked and when below average it is switched through. The output of the operational amplifier 44 is connected to the SET input 25' of a D-flip-flop 24' and the clock input 23' is connected to the tap between the resistor 15 and the switch 14. The inverting output of the D-flip-flop 26' is connected to a terminal 49. The D-flip-flop 24' has the same design as the D-flip-flop 24 (Fig. 2).

Referring to Fig. 1b the terminal 49 is connected to a first input 50 of an exclusive-OR-circuit 51 and the terminal 41 is con-

nected to a second input 52 of the exclusive-OR-circuit 51.

The exclusive-OR-circuit 51 includes four NAND-gates 53, 54, 55 and 56. The input 50 is connected to the first inputs of the NAND-gates 53 and 54 respectively and the input 52 is connected to the second inputs of the NAND-gates 53 and 55 respectively. The first input of the NAND-gate 55 is connected to the second input of the NAND-gate 54 and to the output of the NAND-gate 53. The outputs of the NAND-gates 54 and 55 are connected to the two inputs of the NAND-gate 56 and the output of the NAND-gate 56 is connected to the output 57 of the exclusive-OR-circuit 51.

If the two inputs 50 and 52 have the potential "O", then the potential "O" is also present at the output 57. If the two inputs 50 and 52 have complementary potential values, then the potential "L" is present at the output 57. If the two inputs 50 and 52 have the potential "L" then the potential at the output 57 is "O".

The output 57 of the exclusive-OR-circuit 51 is connected to the input of a threshold sensitive amplifier 58, to the output of which is connected a diaphragm control magnet 59 which has a mechanical connection 60 to the switch 10 (Fig. 1a) and a mechanical connection 61 to a diaphragm member 62.

The method of operation is as follows:

When the switches 2, 3 and 14 are closed, the transistors 6, 9 and 17 are biased on. The capacitor 8 is thus bridged. Since the transistor 13 is biased off, the photoresistor 7 and the resistor 12 act as a potential divider. If the brightness of the prevailing illumination is greater than an average value, then the two operational amplifiers 19 and 44 are biased off. Consequently, the potential "L" is present at the SET inputs 23 and 25' of the two D-flop-flips 24 and 24'. As a result there is a potential "O" at each of the outputs 26 and 26'. The potential "O" is also present at the inputs 50 and 52 of the exclusive-OR-circuit and consequently at its output 57 too, there is the potential "O".

The threshold value amplifier 58 is therefore, biased off and the diaphragm control magnet 59 de-energised. A diaphragm aperture f5.6, for example is set by a mechanical connection (not illustrated) and the switch 10 is opened. Since the transistor 32 is biased off, the luminous diode 33 lights up, indicating to the user of the camera that the prevailing illumination is adequate. The transistor 38 is biased on so that the luminous diode 39 cannot light up.

If the brightness of the prevailing illumination is less than or equal to the average brightness value but still greater than the lower usable brightness value, then the operational amplifier 44 is biased on while the operational amplifier 19 is biased

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off. Consequently a potential "O" is applied to the SET input 25' of the D-flip-flop 24', whereas the potential "L" is present at the SET input 23 of the D-flip-flop 24. At the output 26' of the D-flip-flop 24' and at the input 50 of the exclusive-OR-circuit 51 there is the potential "L", whereas at the input 52 of the exclusive-OR-circuit 51 the potential "O" is present. Consequently the potential at the output 57 of the exclusive-OR-circuit has the value "L", which results in the threshold value amplifier 58 being biased on and consequently in the diaphragm control magnet 59 being energised. This results in a diaphragm aperture f2.8 being set, in a manner not illustrated. The switch 10 is closed by means of the mechanical connection 60, and the capacitor 11 is connected in parallel to the capacitor 8. The diaphragm aperture f2.8 is thus taken into account in the determination of the exposure time.

If the brightness falls below the lower usable brightness value, the operational amplifier 19 is also biased on. Consequently there is potential "O" at the SET input 23 of the D-flip-flop 24, and a potential "L" at the output 26. The luminous diode 33 is extinguished, while the luminous diode 39 lights up. There is a potential "L" at the two inputs 50 and 52 of the exclusive-OR-circuit 51 so that there is a potential "O" at the output 57. The threshold value amplifier 58 is biased off so that the diaphragm control magnet 59 is de-energised and the diaphragm aperture f5.6 re-set.

To take an exposure the switch 14 is opened in a manner not illustrated so that the transistor 13 is biased on and the resistor 12 thus bridged, whereas the transistor 9 is biased off and the capacitor 8 thus released for charging. The potentials at the SET inputs 23 and 25' as well as at the clock inputs 25 and 23' of the D-flip-flops 24 and 24' take the value "O". The potential value originally at the outputs 26 and 26' does not, however, alter since with the ceasing of the clock signal the initial state of the D-flip-flop is retained.

Only when the clock signal assumes the potential "L" when the switch 14 is closed again is the D-flip-flop 24 or 24' reconnected in readiness for storage.

WHAT WE CLAIM IS:—

1. A camera including a photo-sensitive element which is arranged to receive ambient light and to provide an electrical signal which depends on the light received, a first threshold detector which is arranged to receive the electrical signal and to provide an output signal which changes value abruptly as the electrical signal crosses a first threshold value, a second threshold detector which is arranged to receive the

electrical signal and to provide an output signal which changes value abruptly as the electrical signal crosses a second threshold value, a bistable device electronic store which is arranged to receive the output signals from the threshold detectors and to store digital information corresponding to the combined threshold detector outputs, a diaphragm aperture control circuit which is connected to the output terminals of the bistable device electronic store and is arranged to provide set aperture adjustments appropriate to the ambient lighting level and in accordance with the contents of the bistable device electronic store, and an exposure time control circuit which includes the photo-sensitive element and a switch which is arranged to initiate exposure and to freeze the contents of the bistable device electronic store when operated.

2. A camera as claimed in claim 1, wherein the bistable device electronic store includes two gated bistable devices having data input terminals and gate terminals, the data input terminals of which are connected to the output terminals of the respective threshold detectors, and the gate terminals of which are connected to the exposure initiation switch.

3. A camera as claimed in claim 1 or claim 2, wherein the diaphragm aperture control circuit provides two set aperture adjustments, and one of the set aperture adjustments alters the exposure time control circuit by introducing an auxiliary capacitor into the said circuit.

4. A camera as claimed in claim 3, wherein one of the set aperture adjustments is appropriate to an average ambient lighting level, and the other set aperture adjustment is appropriate to a high ambient lighting level.

5. A camera as claimed in any one of claims 1 to 4, wherein the diaphragm aperture control circuit includes an EXCLUSIVE-OR gate, the input terminals of which are connected to the output terminals of the bistable device electronic store.

6. A camera as claimed in any one of claims 1 to 5, wherein the first and second threshold detectors are provided by first and second operational amplifiers, the first operational amplifier having its inverting input terminal connected to a first potential divider which sets the first threshold value, and the second operational amplifier having its inverting terminal connected to a second potential divider which sets the second threshold level.

7. A camera as claimed in any one of claims 1 to 6, wherein the photo-sensitive element is arranged in series with a resistor and a battery when the exposure initiation switch is closed, and the photo-sensitive element is arranged in series with a main

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off. Consequently a potential "O" is applied to the SET input 25' of the D-flip-flop 24', whereas the potential "L" is present at the SET input 23 of the D-flip-flop 24. At the output 26' of the D-flip-flop 24' and at the input 50 of the exclusive-OR-circuit 51 there is the potential "L", whereas at the input 52 of the exclusive-OR-circuit 51 the potential "O" is present. Consequently the potential at the output 57 of the exclusive-OR-circuit has the value "L", which results in the threshold value amplifier 58 being biased on and consequently in the diaphragm control magnet 59 being energised. This results in a diaphragm aperture f2.8 being set, in a manner not illustrated. The switch 10 is closed by means of the mechanical connection 60, and the capacitor 11 is connected in parallel to the capacitor 8. The diaphragm aperture f2.8 is thus taken into account in the determination of the exposure time.

If the brightness falls below the lower usable brightness value, the operational amplifier 19 is also biased on. Consequently there is potential "O" at the SET input 23 of the D-flip-flop 24, and a potential "L" at the output 26. The luminous diode 33 is extinguished, while the luminous diode 39 lights up. There is a potential "L" at the two inputs 50 and 52 of the exclusive-OR-circuit 51 so that there is a potential "O" at the output 57. The threshold value amplifier 58 is biased off so that the diaphragm control magnet 59 is de-energised and the diaphragm aperture f5.6 re-set.

To take an exposure the switch 14 is opened in a manner not illustrated so that the transistor 13 is biased on and the resistor 12 thus bridged, whereas the transistor 9 is biased off and the capacitor 8 thus released for charging. The potentials at the SET inputs 23 and 25' as well as at the clock inputs 25 and 23' of the D-flip-flops 24 and 24' take the value "O". The potential value originally at the outputs 26 and 26' does not, however, alter since with the ceasing of the clock signal the initial state of the D-flip-flop is retained.

Only when the clock signal assumes the potential "L" when the switch 14 is closed again is the D-flip-flop 24 or 24' reconnected in readiness for storage.

WHAT WE CLAIM IS:—

1. A camera including a photo-sensitive element which is arranged to receive ambient light and to provide an electrical signal which depends on the light received, a first threshold detector which is arranged to receive the electrical signal and to provide an output signal which changes value abruptly as the electrical signal crosses a first threshold value, a second threshold detector which is arranged to receive the

electrical signal and to provide an output signal which changes value abruptly as the electrical signal crosses a second threshold value, a bistable device electronic store which is arranged to receive the output signals from the threshold detectors and to store digital information corresponding to the combined threshold detector outputs, a diaphragm aperture control circuit which is connected to the output terminals of the bistable device electronic store and is arranged to provide set aperture adjustments appropriate to the ambient lighting level and in accordance with the contents of the bistable device electronic store, and an exposure time control circuit which includes the photo-sensitive element and a switch which is arranged to initiate exposure and to freeze the contents of the bistable device electronic store when operated.

2. A camera as claimed in claim 1, wherein the bistable device electronic store includes two gated bistable devices having data input terminals and gate terminals, the data input terminals of which are connected to the output terminals of the respective threshold detectors, and the gate terminals of which are connected to the exposure initiation switch.

3. A camera as claimed in claim 1 or claim 2, wherein the diaphragm aperture control circuit provides two set aperture adjustments, and one of the set aperture adjustments alters the exposure time control circuit by introducing an auxiliary capacitor into the said circuit.

4. A camera as claimed in claim 3, wherein one of the set aperture adjustments is appropriate to an average ambient lighting level, and the other set aperture adjustment is appropriate to a high ambient lighting level.

5. A camera as claimed in any one of claims 1 to 4, wherein the diaphragm aperture control circuit includes an EXCLUSIVE-OR gate, the input terminals of which are connected to the output terminals of the bistable device electronic store.

6. A camera as claimed in any one of claims 1 to 5, wherein the first and second threshold detectors are provided by first and second operational amplifiers, the first operational amplifier having its inverting input terminal connected to a first potential divider which sets the first threshold value, and the second operational amplifier having its inverting terminal connected to a second potential divider which sets the second threshold level.

7. A camera as claimed in any one of claims 1 to 6, wherein the photo-sensitive element is arranged in series with a resistor and a battery when the exposure initiation switch is closed, and the photo-sensitive element is arranged in series with a main



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capacitor and the battery when the exposure initiation switch is open.

5 8. A camera as claimed in claim 7, wherein the exposure time control circuit includes a threshold switch having its input terminal connected to the main capacitor and having its output terminal connected to shutter-operating relay, and a transistor which is connected to the shutter-operating coil and is arranged to hold the shutter closed when the exposure initiation switch is closed.

10 9. A camera as claimed in any one of claims 1 to 8, and including a first electroluminescent display device which is connected to a part of the bistable device electronic store and is arranged to be

energised when that part of the bistable device electronic store includes a logical "1", and a second electroluminescent display device which is connected to the said part of the bistable device electronic store and is arranged to be energised when that part of the bistable device electronic store includes a logical "0".

20 25 10. A camera substantially as described herein with reference to and as illustrated by the accompanying drawings.

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