Apparatus and Method for Implementing a Constant Transconductance Circuit

Field of the Invention

This invention relates to constant transconductance circuits and, more specifically, to a MOSFET biasing circuit for generating constant transconductance that is independent of process variations, power supply voltage and temperature changes.

Background

The transconductance of a metal oxide semiconductor field effect transistor (MOSFET) is an important parameter in analog circuit designs. The transconductance of a MOSFET biasing circuit or the like field effect transistor is a measure of the rate of change in the drain-to-source current in response to a change in the gate-to-source voltage of the MOSFET. The transconductance affects the performance parameters like noise, gain, and frequency response of analog blocks such as operational amplifiers, which are dependent on the MOSFET biasing circuit. Hence it is important to have constant transconductance that is substantially independent of temperature, manufacturing process, and power supply voltage fluctuations associating with the MOSFET biasing circuit. Examples of the constant transconductance biasing circuits include those proposed in publications by J.M. Steininger, "Understanding Wide-band MOS Transistors," IEEE Circuits and MOSFETs, Vol. 6, No. 3, pp. 26-31, May 1990; J. Ryan et al., "A Magnetic Field Sensitive Amplifier with Temperature Compensation," ISSCC Digest of Technical Papers, pp. 124-125, February 1992; and D. Johns and K. Martin, "Analog Integrated Circuit Design," Wiley, 1997, pp. 248-250.

FIG. 1 shows a prior art constant transconductance biasing circuit 100 employing an off-chip resistor R as proposed by Steininger. The principle of operation of the constant transconductance biasing circuit, as shown in FIG. 1, is based on the difference between the gate-to-source voltages of two same or different-sized field

effect transistors (FET) M3 and M4 being equal to the voltage across the off-chip resistor R. The current flowing through the FET M3 and the off-chip resistor R is the same or proportional to the current flowing through the FET M4. The currents flowing through the FETs M3 and M4 and the off-chip resistor R are provided by FETs M5 and M6. This results in constant transconductance that is proportional to the geometric ratios of M3 and M4 and the inverse value of the off-chip resistor R. Thus, the transconductance is independent of changes in process, temperature, and power supply voltage.

However, there are disadvantages in using the off-chip resistor R in this case. These include the off-chip resistor R taking up valuable circuit board space and using an additional input-output pin of a chip comprising the constant transconductance biasing circuit, which could otherwise be used for other much needed functions such as for controlling or sensing. Further, using the off-chip resistor R also gives rise to noise injection problem. With an on-chip resistor, on the other hand, it is difficult to achieve an accurate resistance and it suffers from large resistance variations, in some cases exceeding 50%, due to manufacturing process fluctuations and temperature changes. The variations in resistance give rise to difficulties in precisely determining and controlling the absolute value of the transconductance provided by the constant transconductance biasing circuit.

There are a number of proposals for constant transconductance circuits. For example, in U.S. Pat. 4,484,089 by Visawanathan, a switched capacitor arrangement for conductance control of variable conductance elements is proposed. The transconductance of a MOSFET is matched to an effective conductance C_1/T of a capacitor C_1 that is switched at a clock rate of 1/T. The disadvantage of this proposal lies in its requirement for precise external digital clock inputs to switch the capacitor on and off at predetermined intervals.

Another example is proposed in U.S. Pat. 5,973,524 by Martin. A phase-lock-loop circuit is used to automatically trim an on-chip resistor used in a constant transconductance biasing circuit. The phase-lock-loop includes an oscillator of which the frequency is controlled by the constant transconductance biasing circuit and a

phase frequency detector that compares the oscillator output frequency with an external reference frequency. The output of the phase frequency detector is connected to a loop filter for controlling the on-chip resistor in the constant transconductance bias circuit. The disadvantage of this proposal lies in its requirement for a high precision external reference frequency.

Yet another example is found in U.S. Pat. 5,777,518 by Bailey, which proposes a biasing circuit that includes a pair of MOSFETs. The first MOSFET is biased in a triode-operating region with a constant reference drain-to-source terminal voltage and with a constant first reference drain-to-source terminal current. The second MOSFET is biased in a saturation-operating region by a circuit that derives a gate-to-source terminal bias voltage from the gate terminal voltage of the first MOSFET and a reference voltage. A second reference current flows into the drain terminal of the second MOSFET, and a corresponding bias current is derived by mirroring the second reference current. The mirrored reference current is used to bias an amplifier MOSFET and thereby for maintaining a substantially constant transconductance over a range of variations in power supply voltage, temperature and process. The disadvantage of this proposal lies in its requirement for matching the pair of MOSFETs that is operating in different regions.

It is therefore desirable to provide a constant transconductance circuit that does not require external components, or a precise clock signal, or the like.

Summary

In accordance with a first aspect of the invention, there is disclosed a circuit for generating constant transconductance in an integrated circuit including a reference voltage source and a reference current source. The circuit comprises a current source for providing a biasing current, a transconductance generating circuit that is connected to the current source for receiving the biasing current therefrom, and a resistance generating circuit that is connected to the transconductance generating circuit for providing an equivalent resistance through which the biasing current flows, thereby

generating a biasing voltage, whereby the transconductance generating circuit generates an output biasing voltage having constant transconductance.

In a second aspect of the invention, there is disclosed a method for generating constant transconductance in an integrated circuit including a reference voltage source and a reference current source. The method comprises the steps of providing a biasing current using a current source, connecting a transconductance generating circuit to the current source for receiving a biasing current therefrom, and connecting a resistance generating circuit to the transconductance generating circuit for providing an equivalent resistance through which the biasing current flows, thereby generating a biasing voltage, whereby the transconductance generating circuit generates an output biasing voltage having constant transconductance.

Brief Descriptions of The Drawings

Embodiments of the invention are described hereinafter with reference to the following drawings, in which:

FIG. 1 shows a prior art electrical schematic diagram of a constant transconductance biasing circuit; and

FIG. 2 shows an example of a preferred way of implementing a constant transconductance generating circuit according to an embodiment of the invention.

Detailed Description

A constant transconductance generating circuit that is independent of variations in process, power supply voltage, and temperature without making use of an off-chip resistor is described hereinafter. A description of an embodiment of the invention is made with reference to the figures of the drawings.

A constant transconductance generating circuit 200 according to an embodiment of the invention is shown in FIG. 2. The constant transconductance generating circuit

200 produces a biasing voltage (V_{bias}) for biasing on-chip MOSFET amplifiers (not shown) with constant transconductance. The constant g_m generating circuit 200 comprises an on-chip resistor equivalent circuit 210 or the like resistance generating circuit, a current mirror circuit 240 or the like transconductance generating circuit and a current source 250. The current mirror circuit 240 includes a pair of MOSFETs M3 and M4 biased to operate in the saturation region. This is achieved by passing a pair of equal or proportional currents I_b generated by the current source 250 to the respective drain terminals of the MOSFETs M3 and M4 as shown in FIG. 2. The gate terminals of the MOSFETs M3 and M4 are interconnected and are connected to the drain terminal of the MOSFET M4 to derive a biasing operating voltage therefrom. For easy understanding, it is assumed that the current source 250 provides equal currents I_b to the pair of MOSFETs M3 and M4, hereinafter.

The general principle of operation of a constant transconductance generating circuit is based on the difference between the gate-to-source voltages of two same or different-sized field effect transistors (FET) A and B being equal to the voltage across the off-chip resistor R that is connected to the FET A. The current flowing through the FET A and the off-chip resistor R is the same or proportional to the current flowing through the FET B. The currents flowing through the FETs A and B, and the off-chip resistor R are provided by a current source. This results in constant transconductance that is proportional to the geometric ratios of the FETs A and B and the inverse value of the off-chip resistor R. Thus, the transconductance is independent of changes in process, temperature, and power supply voltage. The requirement to generate constant transconductance can also be generally described using the following expression:

$$V_{GS_B} = V_{GS_A} + I_{D_A}R \tag{1}$$

where V_{GS_B} is the gate-to-source voltage of the FET B, V_{GS_A} is the gate-to-source voltage of the FET A, I_{D_A} is the drain current of the FET A, and R is the resistance of the off-chip resistor R connected in series to the FET A. The gate terminals of the FETs A and B, and the drain of the FET B are interconnected. Therefore, the current

mirror circuit 240, the current source circuit 250 and the on-chip resistor equivalent circuit 210 are connected, as shown in FIG. 2, to produce the relationship as described by equation (1) to generate constant transconductance required. In this case, the general equation (1) can be expressed as follows:

$$V_{GS_M4} = V_{GS_M3} + I_b R \tag{2}$$

where V_{GS_M4} is the gate-to-source voltage of the MOSFET M4, V_{GS_M3} is the gate-to-source of the MOSFET M3, I_b is the drain current of the MOSFET M3, and R is the resistance provided by the on-chip resistor equivalent circuit 210 connected in series to the source terminal of the MOSFET M3.

From equation (2) above, it can be shown that with the drain currents of the MOSFETs M3 and M4 being equal, the transconductance of the MOSFET M4 is:

$$g_{m4} = 2\frac{\left[1 - \sqrt{(W/L)_4/(w/L)_3}\right]}{R} \tag{3}$$

where g_{m4} is the transconductance of the MOSFET M4, W and L represent the channel width and length of the MOSFETs, respectively, $(W/L)_3$ and $(W/L)_4$ are the aspect ratios of the MOSFETs M3 and M4, respectively, and R is the resistance provided by the on-chip resistor equivalent circuit 210 connected in series to the source terminal of the MOSFET M3.

Equation (3) shows that the transconductance of the MOSFET M4 is determined by the W/L ratios and R only, and it is independent of power supply voltages, process parameters and temperatures.

In the preferred embodiment, the on-chip resistor equivalent circuit 210 replaces the off-chip resistor R, typically used in a conventional constant transconductance generating circuit. The on-chip resistor equivalent circuit 210 includes an operational amplifier 202, a MOSFET M1, a MOSFET M2, a reference voltage source (V_{ref}) 220,

and a reference current source (I_{ref}) 230. V_{ref} 220 and I_{ref} 230 are readily available onboard a circuit into which the constant transconductance generating circuit 200 is integrated. The operational amplifier 202 is connected in a feedback configuration with the inverting terminal connected to V_{ref} 220, the non-inverting terminal connected to the drain terminal of M1, and the output terminal connected to the gate terminal of M1. With this feedback configuration, the operational amplifier 202 is biased to maintain the gate-to-source voltage (V_{GS_M1}) of M1 such that the drain voltage of M1 is substantially equal to V_{ref} 220 with respect to the source terminal of M1, which is connected to a ground node. The drain terminal of M1 is also connected to I_{ref} 230, and thus, M1 is biased to operate in the triode region. This way of biasing M1 allows the gate-to-source voltage (V_{GS_M1}) of M1 to assume a value that provides M1 with a resistance R_{M1} being equal to the V_{ref}/I_{ref} ratio. This relationship can be expressed in terms of the geometries and properties of M1 as follows:

$$R_{M1} = \frac{V_{ref}}{I_{ref}} = \frac{1}{\mu_n C_{ox} (W/L)_1 (V_{GS_M1} - V_{TH})} \quad (4)$$

where μ_n is the mobility of electrons near the silicon surface, C_{ox} is the gate capacitance per unit area, and V_{TH} is the threshold voltage of M1.

Having established the resistance R_{M1} of M1 to be the ratio of V_{ref} and I_{ref}, M2 may be biased to mirror the resistance of M1. This is achieved by applying the same gate-to-source voltage (V_{GS_M1}) of M1 across the gate and source terminals of M2, as shown in FIG. 2. M2 is also biased to operate in the triode region with the source terminal of M2 connected to the ground node and the drain terminal connected to the source terminal of M3. The sizes of M1 and M2 may be different in which case the resistances of M1 and M2 are different. However, for easy understanding, the sizes of M1 and M2 are assumed to be the same and the resistance R_{M2} of M2 is equal to the resistance R_{M1} of M1, and is expressed as follows:

$$R_{M2} = \frac{1}{\mu_n C_{ox} (W/L)_2 (V_{GS_M1} - V_{TH})} \quad (5)$$

The mobility of electrons near the silicon surface (μ_n), the gate capacitance per unit area (C_{ox}), and the threshold voltage (V_{TH}) of M2 are substantially the same as those of M1 since both MOSFETs are made of the same semiconductor material and under go the same fabrication process.

Solving equation (4) for V_{GS_M1}:

$$V_{GS_M1} = \frac{1}{\mu_n C_{ox} (W/L)_2 R_{M1}} + V_{TH} \tag{6}$$

and substituting the result of equation (6) into equation (5) yields:

$$R_{M2} = \frac{(W/L)_1}{(W/L)_2} R_{M1} = \frac{(W/L)_1 V_{ref}}{(W/L)_2 I_{ref}} \tag{7}$$

Substituting equation (7) into equation (3) to replace the value of R yields:

$$g_{m4} = 2\left[1 - \sqrt{(W/L)_4 / (W/L)_3}\right] \frac{(W/L)_2 I_{ref}}{(W/L)_1 V_{ref}} \tag{8}$$

The resulting transconductance g_{m4} of M4 is dependent only on V_{ref}, I_{ref}, and the ratios of the geometries of M1, M2, M3, and M4. All of these parameters are known and can be accurately obtained. Furthermore, these parameters are independent of process variations, power supply and temperature changes.

Although the foregoing description discloses a preferred embodiment, it will be apparent to one skilled in the art in view of this disclosure that numerous changes, modifications and combinations can be made without departing from the scope and spirit of the invention. For example, although the MOSFETs M1 and M2 used are N-channel MOSFETs, it will be apparent that the circuits can be implemented using P-

channel MOSFETs. Similarly, a current mirror having a different configuration may be used to replace the current mirror circuit 240.

Claims:

1. A circuit for generating constant transconductance in an integrated circuit including a reference voltage source and a reference current source, the circuit comprising:

a current source for providing a biasing current;

a transconductance generating circuit connected to the current source for receiving the biasing current therefrom; and

a resistance generating circuit connected to the transconductance generating circuit for providing an equivalent resistance through which the biasing current flows, thereby generating a biasing voltage, whereby the transconductance generating circuit generates an output biasing voltage having constant transconductance.

2. The circuit as in claim 1, wherein the transconductance generating circuit comprises:

first and second field effect transistors (FET), each having source, drain and gate terminals, wherein the gate terminals of the first and second FETs and the drain of the second FET are interconnected, each of the drain terminals of the first and second FETs are connected to the current source for receiving the biasing current therefrom, the source terminal of the second FET is connected to a reference potential, and the source terminal of the first FET is connected to the resistance generating circuit, thereby providing a condition for generating constant transconductance in accordance with:

$$V_{GS_2} = V_{GS_1} + I_{D_1}R$$

where V_{GS_2} represents the gate-to-source voltage of the second FET, V_{GS_1} represents the gate-to-source of the first FET, I_{D_1} represents the current flowing through the drain terminal of the first FET, and R represents the equivalent resistance provided by the resistance generating circuit.

3. The circuit as in claim 1, wherein the resistance generating circuit for generating the equivalent resistance comprises:

an operational amplifier having inverting input, non-inverting input and output terminals; and

third and fourth field effect transistors (FET) each having source, drain and gate terminals,

wherein the operational amplifier is connected in a feedback configuration with the non-inverting input terminal being connected to the drain terminal of the third FET,

the inverting input terminal being connected to the reference voltage source (V_{ref}) and the output terminal being connected to the gate terminal of the third FET for maintaining a constant biasing voltage substantially equal to V_{ref};

the third FET being biased to operate in a triode region with the drain terminal being connected to the reference current source (I_{ref}) and the source terminal being connected to a reference potential, thereby generating a first resistance substantially equal to the V_{ref}/I_{ref} ratio; and

the fourth FET being biased to operate in a triode region with the gate terminal being connected to the gate terminal of the third FET for mirroring the first resistance to generate a second resistance, the source terminal being connected to the reference potential and the drain terminal being connected to the transconductance generating circuit, wherein the second resistance being the equivalent resistance.

4. The circuit as in claim 3, wherein the transconductance generating circuit comprises:

first and second field effect transistors (FET), each having source, drain and gate terminals, wherein the gate terminals of the first and second FETs and the drain of the second FET are interconnected, each of the drain terminals of the first and second FETs are connected to the current source for receiving the biasing current therefrom, the source terminal of the second FET is connected to a reference potential, and the source terminal of the first FET is connected to the drain terminal of the fourth FET, thereby providing a condition for generating constant transconductance in accordance with:

$$V_{GS_2} = V_{GS_1} + I_{D_1}R$$

where V_{GS_2} represents the gate-to-source voltage of the second FET, V_{GS_1} represents the gate-to-source of the first FET, I_{D_1} represents the current flowing through the drain terminal of the first FET, and R represents the equivalent resistance provided by the resistance generating circuit.

5. The circuit as in claim 3, wherein the equivalent resistance R provided by the resistance generating circuit is prescribed by:

$$R = \frac{(W/L)_3 V_{ref}}{(W/L)_4 I_{ref}}$$

where W and L represent the channel width and length of the FETs, respectively, $(W/L)_3$ and $(W/L)_4$ represent the aspect ratios of the third and fourth FETs, respectively, and V_{ref} and I_{ref} represent the reference voltage and reference current sources, respectively.

6. A method for generating constant transconductance in an integrated circuit including a reference voltage source and a reference current source, the method comprising the steps of:

providing a biasing current using a current source;

connecting a transconductance generating circuit to the current source for receiving the biasing current therefrom; and

connecting a resistance generating circuit to the transconductance generating circuit for providing an equivalent resistance through which the biasing current flows, thereby generating a biasing voltage, whereby the transconductance generating circuit generates an output biasing voltage having constant transconductance.

7. The method as in claim 6, wherein the step of connecting the transconductance generating circuit to the current source comprises the steps of:

providing first and second field effect transistors (FET), each having source, drain and gate terminals;

interconnecting the gate terminals of the first and second FETs and the drain terminal of the second FET;

connecting each of the drain terminals of the first and second FETs to the current source for receiving the biasing current therefrom;

connecting the source terminal of the second FET to a reference potential; and

connecting the source terminal of the first FET to the resistance generating circuit, thereby providing a condition for generating constant transconductance in accordance with:

$$V_{GS_2} = V_{GS_1} + I_{D_1}R$$

where V_{GS_2} represents the gate-to-source voltage of the second FET, V_{GS_1} represents the gate-to-source of the first FET, I_{D_1} represents the current flowing through the drain terminal of the first FET, and R represents the equivalent resistance provided by the resistance generating circuit.

8. The method as in claim 6, wherein the step of connecting the resistance generating circuit to the transconductance generating circuit comprises the steps of:

providing an operational amplifier having inverting input, non-inverting input and output terminals;

providing third and fourth field effect transistors (FET) each having source, drain and gate terminals;

connecting the operational amplifier in a feedback configuration with the non-inverting input terminal being connected to the drain terminal of the third FET, the inverting input terminal being connected to the reference voltage source (V_{ref}) and the output terminal being connected to the gate terminal of the third FET for maintaining a constant biasing voltage substantially equal to V_{ref};

biasing the third FET to operate in a triode region with the drain terminal being connected to the reference current source (I_{ref}) and the source terminal being connected to a reference potential, thereby generating a first resistance substantially equal to the V_{ref}/I_{ref} ratio; and

biasing the fourth FET to operate in a triode region with the gate terminal being connected to the gate terminal of the third FET for mirroring the first resistance to generate a second resistance, the source terminal being connected to the reference potential and the drain terminal being connected to the transconductance generating circuit, wherein the second resistance being the equivalent resistance.

9. The method as in claim 8, wherein the step of connecting the transconductance generating circuit to the current source comprises the steps of:

providing first and second field effect transistors (FET), each having source, drain and gate terminals;

interconnecting the gate terminals of the first and second FETs and the drain terminal of the second FET;

connecting each of the drain terminals of the first and second FETs to the current source for receiving the biasing current therefrom;

connecting the source terminal of the second FET to a reference potential; and

connecting the source terminal of the first FET to the drain terminal of the fourth FET, thereby providing a condition for generating constant transconductance in accordance with:

$$V_{GS_2} = V_{GS_1} + I_{D_1}R$$

where V_{GS_2} represents the gate-to-source voltage of the second FET, V_{GS_1} represents the gate-to-source of the first FET, I_{D_1} represents the current flowing through the drain terminal of the first FET, and R represents the equivalent resistance provided by the resistance generating circuit.

10. The method as in claim 8, wherein the step of connecting the resistance generating circuit to the transconductance generating circuit further comprises the step of providing the equivalent resistance R that is prescribed by:

$$R = \frac{(W/L)_3 V_{ref}}{(W/L)_4 I_{ref}}$$

where W and L represent the channel width and length of the FETs, respectively, $(W/L)_3$ and $(W/L)_4$ represent the aspect ratios of the third and fourth FETs, respectively, and V_{ref} and I_{ref} represent the reference voltage and reference current sources, respectively.