

Claims:

1. A method of preparing a multilayer structure, the method comprising:

depositing a layer of silicon dioxide on a back surface of a single crystal semiconductor handle wafer, wherein the single crystal semiconductor handle wafer comprises two major, parallel surfaces, one of which is the back surface of the single crystal semiconductor handle wafer and the other of which is a front surface of the single crystal semiconductor handle wafer, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle wafer, a central axis perpendicular to the front surface and the back surface of the single crystal semiconductor handle wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor handle wafer;

bonding the front surface of the single crystal semiconductor handle wafer to a dielectric layer in contact with a front surface of a single crystal semiconductor donor wafer to thereby form a bonded structure, wherein the single crystal semiconductor donor wafer comprises two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor donor wafer and the other of which is a back surface of the single crystal semiconductor donor wafer, a circumferential edge joining the front and back surfaces of the single crystal semiconductor donor wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor donor wafer, and further wherein the bulk region comprises a cleave plane;

mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor wafer to thereby prepare a cleaved structure comprising the layer of silicon dioxide in contact with the back surface of the single crystal semiconductor handle wafer, the single crystal semiconductor handle wafer, the dielectric layer in contact with the front surface of the single crystal semiconductor handle wafer, and a single crystal semiconductor device layer, wherein the single crystal semiconductor device layer comprises an exposed surface; and

smoothing the exposed surface of the single crystal semiconductor device layer to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 2 angstroms to thereby prepare the multilayer structure.

2. The method of claim 1 wherein the single crystal semiconductor handle wafer comprises a single crystal silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method or the float zone method.

3. The method of claim 1 wherein the layer of silicon dioxide deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 1000 angstroms and 20,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

4. The method of claim 1 wherein the layer of silicon dioxide deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 1000 angstroms and 5000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

5. The method of claim 1 wherein a layer of silicon dioxide is deposited on the front surface of the single crystal semiconductor handle wafer simultaneously with deposition of the layer of silicon dioxide on the back surface of the single crystal semiconductor handle wafer, and the method further comprises removing the layer of silicon dioxide deposited on the front surface of the single crystal semiconductor handle wafer prior to the bonding step.

6. The method of claim 1 wherein the single crystal semiconductor device layer is between 40 angstroms and 1000 angstroms thick, as measured along the central axis of the single crystal semiconductor handle wafer.

7. The method of claim 1 wherein the single crystal semiconductor device layer comprises single crystal silicon.

8. The method of claim 1 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.5 angstroms.

9. The method of claim 1 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.0 angstroms.

10. The method of claim 1 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.2 angstroms.

11. The method of claim 1 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.0 angstroms.

12. The method of claim 1 wherein the exposed surface of the single crystal semiconductor device layer is smoothed by epitaxial smoothing.

13. A method of preparing a multilayer structure, the method comprising:
depositing a layer of silicon nitride on a back surface of a single crystal semiconductor handle wafer, wherein the single crystal semiconductor handle wafer comprises two major, parallel surfaces, one of which is the back surface of the single crystal semiconductor handle wafer and the other of which is a front surface of the single crystal semiconductor handle wafer, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle wafer, a central axis perpendicular to the front surface and the back surface of the single crystal semiconductor handle wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor handle wafer;

bonding the front surface of the single crystal semiconductor handle wafer to a dielectric layer in contact with a front surface of a single crystal semiconductor donor wafer to thereby form a bonded structure, wherein the single crystal semiconductor donor wafer comprises two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor donor wafer and the other of which is a back surface of the single crystal semiconductor donor wafer, a circumferential edge joining the front and back surfaces of the single crystal semiconductor donor wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor donor wafer, and further wherein the bulk region comprises a cleave plane;

mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor wafer to thereby prepare a cleaved structure comprising the layer of silicon nitride in contact with the back surface of the single crystal semiconductor handle wafer, the single crystal semiconductor handle wafer, the dielectric layer in contact with the front surface of the single crystal semiconductor handle wafer, and a single crystal semiconductor device layer, wherein the single crystal semiconductor device layer comprises an exposed surface; and

smoothing the exposed surface of the single crystal semiconductor device layer to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 2 angstroms to thereby prepare the multilayer structure.

14. The method of claim 13 wherein the single crystal semiconductor handle wafer comprises a single crystal silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method or the float zone method.

15. The method of claim 13 wherein the layer of silicon nitride deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 500 angstroms and 20,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

16. The method of claim 13 wherein the layer of silicon nitride deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 1000 angstroms and 5000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

17. The method of claim 13 wherein the single crystal semiconductor device layer is between 40 angstroms and 1000 angstroms thick, as measured along the central axis of the single crystal semiconductor handle wafer.

18. The method of claim 13 wherein the single crystal semiconductor device layer comprises single crystal silicon.

19. The method of claim 13 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.5 angstroms.

20. The method of claim 13 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.0 angstroms.

21. The method of claim 13 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.2 angstroms.

22. The method of claim 13 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.0 angstroms.

23. The method of claim 13 wherein the exposed surface of the single crystal semiconductor device layer is smoothed by epitaxial smoothing.

24. A method of preparing a multilayer structure, the method comprising:
depositing a layer of polycrystalline silicon carbide on a back surface of a single crystal semiconductor handle wafer, wherein the single crystal semiconductor handle wafer comprises two major, parallel surfaces, one of which is the back surface of the single crystal semiconductor handle wafer and the other of which is a front surface of the single crystal semiconductor handle wafer, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle wafer, a central axis perpendicular to the front surface and the back surface of the single crystal semiconductor handle wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor handle wafer;

bonding the front surface of the single crystal semiconductor handle wafer to a dielectric layer in contact with a front surface of a single crystal semiconductor donor

wafer to thereby form a bonded structure, wherein the single crystal semiconductor donor wafer comprises two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor donor wafer and the other of which is a back surface of the single crystal semiconductor donor wafer, a circumferential edge joining the front and back surfaces of the single crystal semiconductor donor wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor donor wafer, and further wherein the bulk region comprises a cleave plane;

mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor wafer to thereby prepare a cleaved structure comprising the layer of polycrystalline silicon carbide or the layer of carbon-doped silicon in contact with the back surface of the single crystal semiconductor handle wafer, the single crystal semiconductor handle wafer, the dielectric layer in contact with the front surface of the single crystal semiconductor handle wafer, and a single crystal semiconductor device layer, wherein the single crystal semiconductor device layer comprises an exposed surface; and

smoothing the exposed surface of the single crystal semiconductor device layer to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 2 angstroms to thereby prepare the multilayer structure.

25. The method of claim 24 wherein the layer of polycrystalline silicon carbide comprises between 5 atomic % and 50 atomic % carbon.

26. The method of claim 24 wherein the single crystal semiconductor handle wafer comprises a single crystal silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method or the float zone method.

27. The method of claim 24 wherein the layer of polycrystalline silicon carbide deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 500 angstroms and 50,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

28. The method of claim 24 wherein the layer of polycrystalline silicon carbide deposited on the back surface of the single crystal semiconductor handle wafer

has a thickness between 500 angstroms and 20,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

29. The method of claim 24 wherein the layer of polycrystalline silicon carbide deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 500 angstroms and 5,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

30. The method of claim 24 wherein the layer of polycrystalline silicon carbide deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 40 angstroms and 1000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

31. The method of claim 24 wherein the single crystal semiconductor device layer comprises single crystal silicon.

32. The method of claim 24 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.5 angstroms.

33. The method of claim 24 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.0 angstroms.

34. The method of claim 24 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.2 angstroms.

35. The method of claim 24 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.0 angstroms.

36. The method of claim 24 wherein the exposed surface of the single crystal semiconductor device layer is smoothed by epitaxial smoothing.

37. A method of preparing a multilayer structure, the method comprising:
depositing a layer of boron-doped silicon on a back surface of a single crystal semiconductor handle wafer, wherein the single crystal semiconductor handle wafer comprises two major, parallel surfaces, one of which is the back surface of the single crystal semiconductor handle wafer and the other of which is a front surface of the single crystal semiconductor handle wafer, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle wafer, a central axis perpendicular to the front surface and the back surface of the single crystal semiconductor handle wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor handle wafer;

bonding the front surface of the single crystal semiconductor handle wafer to a dielectric layer in contact with a front surface of a single crystal semiconductor donor wafer to thereby form a bonded structure, wherein the single crystal semiconductor donor wafer comprises two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor donor wafer and the other of which is a back surface of the single crystal semiconductor donor wafer, a circumferential edge joining the front and back surfaces of the single crystal semiconductor donor wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor donor wafer, and further wherein the bulk region comprises a cleave plane;

mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor wafer to thereby prepare a cleaved structure comprising the layer of boron-doped silicon in contact with the back surface of the single crystal semiconductor handle wafer, the single crystal semiconductor handle wafer the dielectric layer in contact with the front surface of the single crystal semiconductor handle wafer , and a single crystal semiconductor device layer, wherein the single crystal semiconductor device layer comprises an exposed surface; and

smoothing the exposed surface of the single crystal semiconductor device layer to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 2 angstroms to thereby prepare the multilayer structure.

38. The method of claim 37 wherein the single crystal semiconductor handle wafer comprises a single crystal silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method or the float zone method.

39. The method of claim 37 wherein the layer of boron-doped silicon deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 500 angstroms and 50,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

40. The method of claim 37 wherein the layer of boron-doped silicon deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 1000 angstroms and 20,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

41. The method of claim 37 wherein the layer of boron-doped silicon deposited on the back surface of the single crystal semiconductor handle wafer comprises a boron dopant concentration between 1×10^{17} atoms/cm³ and 1×10^{22} atoms/cm³.

42. The method of claim 37 wherein the layer of boron-doped silicon deposited on the back surface of the single crystal semiconductor handle wafer comprises a boron dopant concentration between 1×10^{18} atoms/cm³ and 1×10^{21} atoms/cm³.

43. The method of claim 37 wherein the single crystal semiconductor device layer is between 40 angstroms and 1000 angstroms thick, as measured along the central axis of the single crystal semiconductor handle wafer.

44. The method of claim 37 wherein the single crystal semiconductor device layer comprises single crystal silicon.

45. The method of claim 37 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.5 angstroms.

46. The method of claim 37 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.0 angstroms.

47. The method of claim 37 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.2 angstroms.

48. The method of claim 37 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.0 angstroms.

49. The method of claim 37 wherein the exposed surface of the single crystal semiconductor device layer is smoothed by epitaxial smoothing.

50. A method of preparing a multilayer structure, the method comprising:
depositing a layer of silicon oxynitride on a back surface of a single crystal semiconductor handle wafer, wherein the single crystal semiconductor handle wafer comprises two major, parallel surfaces, one of which is the back surface of the single crystal semiconductor handle wafer and the other of which is a front surface of the single crystal semiconductor handle wafer, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle wafer, a central axis perpendicular to the front surface and the back surface of the single crystal semiconductor handle wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor handle wafer;

bonding the front surface of the single crystal semiconductor handle wafer to a dielectric layer in contact with a front surface of a single crystal semiconductor donor

wafer to thereby form a bonded structure, wherein the single crystal semiconductor donor wafer comprises two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor donor wafer and the other of which is a back surface of the single crystal semiconductor donor wafer, a circumferential edge joining the front and back surfaces of the single crystal semiconductor donor wafer, and a bulk region between the front and back surfaces of the single crystal semiconductor donor wafer, and further wherein the bulk region comprises a cleave plane, and further wherein the bonded structure comprises the layer of silicon oxynitride deposited on the back surface of the single crystal semiconductor handle wafer, the single crystal semiconductor handle wafer, the dielectric layer in contact with the front surface of the single crystal semiconductor handle wafer, and the single crystal semiconductor donor wafer;

mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor wafer to thereby prepare a cleaved structure comprising the layer of silicon oxynitride in contact with the back surface of the single crystal semiconductor handle wafer, the single crystal semiconductor handle wafer, the dielectric layer in contact with the front surface of the single crystal semiconductor handle wafer, and a single crystal semiconductor device layer, wherein the single crystal semiconductor device layer comprises an exposed surface; and

smoothing the exposed surface of the single crystal semiconductor device layer to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 2 angstroms to thereby prepare the multilayer structure.

51. The method of any preceding claim, wherein the single crystal semiconductor handle wafer comprises a material selected from the group consisting of silicon, silicon carbide, silicon germanium, gallium arsenide, gallium nitride, indium phosphide, indium gallium arsenide, germanium, and combinations thereof.

52. The method of claim 50 wherein the single crystal semiconductor handle wafer comprises a single crystal silicon wafer sliced from a single crystal silicon ingot grown by the Czochralski method or the float zone method.

53. The method of claim 50 wherein the layer of silicon oxynitride deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 500 angstroms and 20,000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

54. The method of claim 50 wherein the layer of silicon oxynitride deposited on the back surface of the single crystal semiconductor handle wafer has a thickness between 1000 angstroms and 5000 angstroms, as measured along the central axis of the single crystal semiconductor handle wafer.

55. The method of claim 50 wherein the single crystal semiconductor device layer is between 40 angstroms and 1000 angstroms thick, as measured along the central axis of the single crystal semiconductor handle wafer.

56. The method of claim 50 wherein the single crystal semiconductor device layer comprises single crystal silicon.

57. The method of claim 50 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.5 angstroms.

58. The method of claim 50 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of less than 1.0 angstroms.

59. The method of claim 50 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.2 angstroms.

60. The method of claim 50 wherein the exposed surface of the single crystal semiconductor device layer is smoothed to a root mean square surface roughness over a 30 micrometer by 30 micrometer surface region of between 0.8 angstroms and 1.0 angstroms.

61. The method of claim 50 wherein the exposed surface of the single crystal semiconductor device layer is smoothed by epitaxial smoothing.