

Description

The invention relates to a circuit for amplifying and/or attenuating a signal which circuit has an input terminal for receiving an input signal and an output terminal for supplying an output signal, which circuit also comprises an amplifier stage having an inverting input, a non-inverting input, an output which is coupled to the output terminal, a first voltage divider having n taps ($n \geq 2$), which is arranged between the input terminal and a first connection terminal of the circuit and whose taps are connected to a first controllable switching unit for coupling individual ones of these taps to the non-inverting input, and a controllable negative feedback loop from the output terminal to the inverting input comprising a second voltage divider having m taps ($m \geq 2$) which is arranged between the output terminal and a second connection terminal of the circuit and whose taps are connected to a second switching unit for coupling individual ones of these taps to the inverting input of the amplifier. Such a circuit is known from the article "Operationsverstärker-Schaltungen" Elektronik, Vol. 19, No. 11, Arbeitsblatt, No. 52, November 1970, pp 401—404, which shows in Fig. 8 an amplifier arrangement wherein the second connection terminal of the second voltage divider forms the second input of the amplifier. The amplifier can be arranged as an inverting amplifier by grounding the input terminal and applying the input signal to the second connection terminal or can be arranged as a non-inverting amplifier by grounding the second connection terminal and applying the input signal to the input terminal. In both cases the amplification factor is almost fully determined by the setting of the second voltage divider which controls the negative feedback. The first voltage divider only serves to keep the input impedance at the non-inverting input equal to that at the inverting input so as to keep the input offset-voltage of the amplifier low. To this end the resistors of the first voltage divider have the same resistance values as the resistors of the second voltage divider and the first and second switching units are controlled in such manner that corresponding taps of the first and second voltage divider are always connected to the non-inverting and inverting inputs respectively. So, the transmission of the known circuit can only be changed by changing the negative feedback of the amplifier.

German Patent Specification No. 22 62 089 describes a circuit for amplifying and/or attenuating a signal which circuit operates as a treble or bass control. The circuit comprises two differential amplifiers with negative feedback from the output to the inverting input of the amplifier. The negative feedback and consequently the transmission of the circuit is changed in that the current distributions in the two differential amplifiers are changed in opposite senses by varying a direct voltage. This known circuit, however, exhibits a high noise level when

the quiescent current in the differential amplifiers is low and exhibits substantial distortion when the quiescent current is high.

It is the object of the invention to provide a circuit which offers the possibility of obtaining different transmission characteristics with a minimum of additional circuitry. According to the invention the circuit is characterized in that the first and second connection terminals are connected to a point of constant potential, optionally via an impedance each, and in that the control of the first switching unit is independent of the control of the second switching unit. If the state of the first switching unit is changed so that another tap of the first voltage divider (for example a tap which is situated nearer the input terminal) is connected to the non-inverting input of the amplifier stage the gain factor of the circuit is varied (in the present example: increased). Alternatively, the state of the second switching unit may be changed so that another tap of the second voltage divider (for example a tap which is situated nearer the output terminal) is connected to the inverting input of the amplifier stage. The negative feedback is then varied (increased), which means that the gain factor of the circuit is varied (reduced). At least one voltage divider, but suitably both voltage dividers, may comprise a series arrangement of a plurality of resistors, the ends of the series arrangement and the junction points of the resistors each constituting a tap. If the first and the second connection terminals are then each connected to the point of constant potential directly or via a resistor the circuit will operate as a frequency-independent volume control. However, if the circuit has a frequency-dependent transmission factor from the input terminal of the circuit to the non-inverting input of the amplifier stage and/or from the output to the inverting input of the amplifier stage, the circuit will operate as a frequency-dependent volume control, i.e. as a controllable filter.

An embodiment of the invention, which embodiment operates as a frequency-dependent volume control, is characterized in that the ends of the series arrangement corresponding to the first voltage divider are coupled to the input terminal of the circuit and to the first connection terminal respectively and the ends of the series arrangement corresponding to the second voltage divider are coupled to the output of the amplifier stage and to the second connection terminal respectively, and said impedance comprises at least a capacitance arranged between the first connection terminal and the second connection terminal respectively and the point of constant potential. In this way a treble control circuit is obtained. Preferably, the first connection terminal is connected to the second connection terminal via a series arrangement of two resistors, and said capacitance is connected between the junction point of the two resistors and the point of constant potential. This permits one capacitance to be dispensed with, which is favourable in the case of integration.

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A further embodiment of the invention, which embodiment operates as a frequency-dependent volume control circuit, is characterized in that the ends of the series arrangement corresponding to the first voltage divider are coupled to the input terminal of the circuit and to the first connection terminal respectively and the ends of the series arrangement corresponding to the second voltage divider are coupled to the output of the amplifier stage and to the second connection terminal respectively, and first and second capacitances are connected between the input terminal of the circuit and one of the taps of the first voltage divider and between the output of the amplifier stage and one of the taps of the second voltage divider respectively. In this way a bass-control circuit is obtained.

In a preferred embodiment of the invention the first and second switching units are incorporated in a combined switching unit, which combined switching unit comprises $n+m-1$ differential amplifiers, which differential amplifiers each have a first input and a second input for receiving a difference signal, a first output and a second output for supplying two output signals which are in phase opposition and which are dependent on the difference signal, and a control input for receiving a control signal, the first inputs of n of the differential amplifiers being each coupled to an associated tap of the first voltage divider, and the first inputs of the remaining $m-1$ differential amplifiers being all coupled to the tap of the first voltage divider which is situated nearest the input terminal of the circuit, the second inputs of said n differential amplifiers being all coupled to the tap of the second voltage divider which is situated nearest the output terminal of the circuit, and the second inputs of the remaining $m-1$ differential amplifiers being each coupled to an associated one of the remaining taps of the second voltage divider, the first outputs and the second outputs of the differential amplifiers being coupled to the inverting input and the non-inverting input of the amplifier stage respectively, and the combined switching unit comprises means for selectively energizing individual ones of the differential amplifiers, which means are coupled to the control inputs of all the differential amplifiers. If in this embodiment n is equal to m and the two voltage dividers are made identical a fully symmetrical control can be obtained.

Embodiments of the invention will now be described in more detail, by way of example, with reference to the Figures. Of the Figures

Figure 1 shows a first embodiment,

Figure 2a to Figure 2c show the circuit of Figure 1 in more detail for three positions of the switching unit,

Figure 3 shows the frequency response of the circuit shown in Figure 1 for a number of positions of the switching units,

Figure 4 shows a second embodiment,

Figure 5a to Figure 5c show the circuit of Figure 4 in more detail for three positions of the switching units,

Figure 6 shows the frequency response of the circuit shown in Figure 4 for a number of positions of the switching units, and

Figure 7 shows a combined switching unit which it is possible to use in a circuit in accordance with the invention.

Figure 1 shows a first circuit for amplifying and/or attenuating a signal, which circuit has an input terminal 1 for receiving an input signal and an output terminal 2 for supplying an output signal. The circuit comprises an amplifier stage 3 having an inverting input and a non-inverting input and an output. A first voltage divider 5 is arranged between the input terminal 1 and a first connection terminal 4. The first voltage divider 5 comprises ($n=$) six taps 6.1 to 6.6. The six taps are connected to a first controllable switching unit 7 for connecting individual ones of the taps 6.1 to 6.6 to the non-inverting input of the amplifier stage 3. The connection of a tap to the non-inverting input by the switching unit 7 is schematically represented by a switch 8. The switch 8 can be controlled by a control signal applied to a control input 9. A second voltage divider 11 is arranged between the output terminal 2 and a second connection terminal 10. The second voltage divider 11 comprises ($m=$) six taps 12.1 to 12.6 which are connected to a second controllable switching unit 13 for connecting individual ones of the taps 12.1 to 12.6 to the inverting input of the amplifier stage 3. The switching function in the switching unit 13 is schematically represented by a switch 14 which can be controlled by means of a control signal applied to a control input 15. The first and second connection terminals, 4 and 10 respectively, are coupled to a point of constant potential 18 (for example earth), optionally via impedances 16 and 17 respectively. Depending on the type of components in the voltage dividers 5 and 11 and the impedance 16 and 17 (if present) it is possible to obtain a specific transmission characteristic from the input terminal 1 to the output terminal 2. Figure 1 shows the voltage dividers 5 and 11 as comprising series arrangements of a number of resistors 19.1 to 19.5 and 20.1 to 20.5, arranged between input terminal 1 and the first connection terminal 4 and between the output terminal 2 and the second connection terminal 10 respectively, the ends of the series arrangements and the junction points of the resistors each constituting a tap. If the connection terminals 4 and 10 respectively are connected to the point of constant potential 18 directly or via a resistor, the circuit operates as a frequency-independent volume control circuit. However, in Figure 1 the impedances 16 and 17 comprise a series arrangement of a resistor 21 and a capacitance 22 and a series arrangement of a resistor 23 and a capacitance 24 respectively. The circuit then operates as a treble control circuit. This will be explained hereinafter by means of Figures 2a to 2c and Figure 3.

The circuit shown in Figure 1 with the switches 8 and 14 in the positions shown, that is connected to the taps 6.1 and 12.6 respectively, is again

shown in Figure 2a. The feedback resistor 25 has a value corresponding to the overall resistance of the series arrangement in the voltage divider 11. For direct voltage and for very low frequencies in the capacitor 24 has an impedance which is high in comparison with resistance 25. The circuit shown in Figure 2a, which generally has a gain factor equal to

$$1 + \frac{R_{25}}{Z_{17}}$$

(assuming that the gain factor of the amplifier stage 3 is very high and Z_{17} and R_{25} are the impedance values of the impedance 17 and the resistance 25 respectively), then has a gain factor equal to unity or 0 dB, because Z_{17} approximates to infinity for frequencies towards zero. For increasing frequencies the impedance Z_{17} decreases. The gain factor then increases. For very high frequencies the capacitance 24 constitutes a short-circuit. The gain factor then becomes

$$1 + \frac{R_{25}}{R_{23}}$$

R_{23} being the resistance of 23. In Figure 3 the curve 30.1 represents the gain factor of the circuit shown in Figure 2a as a function of the frequency.

If the switch 14 is now consecutively connected to the taps 12.5, 12.4, 12.3 and 12.2 the negative-feedback resistance between the output and the inverting input of the amplifier stage 3 decreases, whilst the impedance between the inverting input of the amplifier stage and the point of constant potential increases (when the frequency remains constant). The gain factor of the circuit is consequently reduced. This corresponds to the curves 30.2 to 30.5 in Figure 3. When the switch 14 is connected to the tap 12.1 the circuit shown in Figure 2b is obtained. Then direct negative feedback is applied from the output to the inverting input of the amplifier stage 3. A series arrangement of a resistor 25 (which is the series arrangement of the voltage divider) and the impedance 17 is then situated between the inverting input and the point of constant potential 8. The gain factor of the circuit arrangement is then unity for all frequencies: see the curve 30.6 in Figure 3.

If the switch 8 is consecutively connected to the taps 6.2, 6.3, ..., 6.6 the circuit shown in Figure 2c is obtained, where 26 is the resistance R_{26} between the input terminal 1 and the non-inverting input of the amplifier stage and 27 is the resistance R_{27} between the non-inverting input and the connection terminal 4. $R_{26} + R_{27}$ corresponds to the resistance value of the series arrangement of the voltage divider 5. The gain factor of the circuit shown in Figure 2c is equal to

$$\frac{R_{27} + Z_{16}}{R_{26} + R_{27} + Z_{16}}$$

where Z_{16} is the impedance value of the impedance 16. During switching the resistance R_{26} increases and the resistance R_{27} decreases until in the position in which switch 8 is connected to the tap 6.6 the resistance R_{27} has become zero and R_{26} corresponds to the resistance value in the voltage divider 5. The gain factor of the circuit then varies in accordance with the curves 30.7, 30.8, ..., 30.11 in Figure 3, the curve 30.11 corresponding to the position in which the switch 8 is connected to the tap 6.6. The gain factor is then

$$\frac{Z_{16}}{R_{26} + Z_{16}}$$

For direct voltages and very low frequencies Z_{16} is very high in comparison with R_{26} , the gain factor is equal to 1 (0 dB). For increasing frequencies Z_{16} decreases and for high frequencies it is equal to R_{21} , which is the resistance value of the resistor 21. The gain factor is then

$$\frac{R_{21}}{R_{26} + R_{21}}$$

If the resistance value of 19.1 is selected to be equal to that of 20.1, if the next resistors 19.2 to 19.5 have the same values as 20.2 to 20.5, and if the resistor 21 and the capacitor 22 are selected to be identical to the resistor 23 and the capacitor 24, a treble control is obtained which is fully symmetrical around 0 dB. In general however the resistors 19.1 to 19.5 and 21 and the capacitor 22 may all be selected so that they are not identical to the corresponding resistors 20.1 to 20.5 and 23 and the capacitor 24. If the resistances 21 and 23 are equal and the capacitances 22 and 24 are equal, only one impedance is required which is connected between the interconnected connection terminals 4 and 10 and the point of constant potential 18, which is favourable for integration in an integrated circuit, because space is saved by dispensing with one capacitance and one resistance. Furthermore, it is not necessary to adhere to the circuit arrangement described in the foregoing in which the switch 14 first passes from tap 12.6 to tap 12.1 and subsequently switch 8 from tap 6.1 to tap 6.6. In principle, all combinations of a tap of voltage divider 5 are connected to the non-inverting input and a tap of voltage divider 11 connected to the inverting input of the amplifier stage 3 are possible. In this last-mentioned case the connection terminals 4 and 10 should not be interconnected when the impedances 16 and 17 are equal, because switch 8 connected to tap 6.6 and switch 14 to tap 12.6 will not yield a correctly operating circuit. In this situation the two resistors 21 and 23 must be maintained. However, it is still possible to use only one capacitance arranged between the junction point of the two resistors 21 and 23, which are then connected in series between the connection terminals 4 and 10, and the point of constant potential.

If in the circuit shown in Figure 1 the capacitances in the impedances 16 and 17 are replaced by inductances a bass control circuit is obtained.

Figure 4 shows a circuit which operates as a bass control circuit. Parts in Figures 1 and 4 bearing the same reference numerals are identical. The first and second connection terminals, 4 and 10 respectively, are connected to the point of constant potential 18 via impedances 16 and 17 respectively, each in the form of a resistor. A first capacitance 41 is connected between the input terminal 1 of the circuit and one of the taps (in the present case the tap 6.6) of the first voltage divider 5, and a second capacitance 42 is connected between the output terminal 2 and one of the taps (in the present case 12.6) of the second voltage divider. If the two capacitances are connected to taps other than 6.6 and 12.6 respectively the impedance between the connection terminal 4 or 10 and the point of constant potential may be dispensed with. The operation of the circuit shown in Figure 4 will be explained with reference to Figures 5a, 5b, 5c and 6. The circuit shown in Figure 4 with the switches 8 and 14 in the positions indicated, that is connected to the taps 6.1 and 12.6 respectively, is again shown in Figure 5a. Negative feedback is provided by the parallel arrangement of the resistor 43 and the capacitance 42. The resistor 43 corresponds to the overall resistance of the series arrangement of the voltage divider 11. For direct voltage and for very low frequencies the capacitance 42 has an impedance which is high in comparison with the resistance value R_{43} of 43. The circuit then has a gain factor

$$1 + \frac{R_{43}}{R_{17}}$$

(R_{17} is the resistance value of the resistor 17 and the gain of the amplifier stage is very high). For increasing frequencies the impedance in the negative-feedback loop decreases. For very high frequencies the capacitance 42 constitutes a short-circuit. The gain is then unity (0 dB).

In Figure 6 the curve 60.1 represents the gain factor of the circuit shown in Figure 5a as a function of the frequency. When the switch-14 is connected to the tap 12.1 the circuit shown in Figure 5b is obtained. Now there is direct negative feedback from the output to the inverting input of the amplifier stage 3. The parallel arrangement of the resistor 43 and the capacitance 42 is now connected in series with the resistor 17 between the inverting input and the point of constant potential 18. The gain factor of the circuit is then equal to unity for all frequencies: see the curve 60.6 in Figure 6.

The intermediate curves 60.2, 60.3, 60.4 and 60.5 correspond to the gain factor for a circuit in which the switch 14 is connected to the respective taps 12.5, 12.4, 12.3 and 12.2. The circuit shown in Figure 5c corresponds to the circuit shown in

Figure 4, in which the switch 14 is connected to tap 12.1 and the switch 8 is connected to the tap 6.6. This results in a frequency-dependent voltage divider at the non-inverting input of the amplifier stage 3. For direct voltage and for very low frequencies the impedance of the capacitor 41 is very high compared with that of the resistor 44. The resistance value R_{44} of the resistor 44 corresponds to the overall series resistance in the voltage divider 5. The gain factor of the circuit is then

$$\frac{R_{16}}{R_{44} + R_{16}}$$

in which R_{16} is the resistance value of the resistor 16. For high frequencies the capacitor 41 constitutes a short-circuit. The gain factor is then unity. The curve 60.11 represents the gain factor of the circuit shown in Figure 5c as a function of the frequency. The intermediate curves 60.7, 60.8, 60.9 and 60.10 represent the gain factors as a function of the frequency for the circuit shown in Figure 4 when the switch 14 is connected to the tap 12.1 and the switch 8 to the respective taps 6.2, 6.3, 6.4 and 6.5. For the values of the various resistors and the number of taps the same is valid as stated in the description with reference to Figure 1.

Figure 7 shows a preferred embodiment of the first and second switching units 7 and 13 shown in Figures 1 and 4. The first and second switching units are incorporated in a combined switching unit bearing the reference numeral 70. The combined switching unit comprises a plurality of differential amplifiers, the number of differential amplifiers corresponding to the sum of the number of taps of the first and second voltage dividers, 5 and 11 respectively, minus one, that is $n+m-1$ or eleven in the case of the circuits shown in Figures 1 and 4. The differential amplifiers are designated 71.1 to 71.11 in Figure 7. Each differential amplifier (such as 71.i, i varying from 1 to 11) has first and second inputs (72.i, and 73.i respectively) for receiving a difference signal, first and second outputs (74.i and 75.i respectively) for supplying two output signals which are in phase opposition and which depend on the difference signal, and a control input (76.i) for receiving a control signal. The first inputs of six of the differential amplifiers, namely the inputs 72.1 to 72.6 of the differential amplifiers 71.1 to 71.6, are each coupled to a respective tap of the first voltage divider 5, namely taps 6.1, ..., 6.6. The first inputs of the other differential amplifiers 71.1 to 71.11 are all coupled to the tap 6.1.

The second inputs of said six differential amplifiers 71.1 to 71.6 are all coupled to the tap 12.1. The second inputs of the other differential amplifiers, namely the inputs 73.7 to 73.11, are each coupled to a respective one of the remaining taps of the second voltage divider 11, namely taps 12.2 to 12.6. The first outputs 74.1, 74.2, ... etc of all differential amplifiers are coupled to the inverting input of the amplifier stage 3 and the second

outputs 75.1, 75.2, ..., etc of all differential amplifiers are coupled to the non-inverting input of the amplifier stage 3. Further the combined switching unit 70 comprises means 77 for selectively energizing individual ones of the differential amplifiers. These means 77 are coupled to the control inputs 76.1, 76.2, ..., etc. of all differential amplifiers. Each differential amplifier comprises two transistors, whose bases are connected to the first input and to the second input respectively, whose collectors are connected to the first output and to the second output respectively, and whose emitters are both connected to the control input of the differential amplifier. The means 77 comprise a plurality of (also $n+m-1$, or eleven) transistors 78.1 to 78.11, whose bases are all connected to a point of constant potential 79 and whose collectors are each connected to a control input of an associated differential amplifier. The emitters of all transistors but one receive a high voltage, so that they are turned off. One transistor receives a low voltage, so that it is turned on. The associated differential amplifier is then selected, that is, only the signals on the first and second inputs of this differential amplifier are transferred to the inputs of the amplifier stage 3 by the combined switching unit 70. By consecutively applying a low voltage to the emitters of the transistors 78.1, 78.2, ... to 78.11 the connection scheme as described with reference to Figures 1 and 4 is obtained. This means that when the switch 8 is in the upper position (i.e. coupled to the tap 6.1), it is possible to select one of the taps 12.1 to 12.6 with the switch 14 and when the switch 14 is in the upper position (i.e. coupled to the tap 12.1) it is possible to select one of the taps 6.1 to 6.6 by means of the switch 4.

If in the combined switching unit 70 an arbitrary one of the taps 6.1 to 6.6 is to be combined with an arbitrary one of the taps 12.1 to 12.6, the combined switching unit should be extended to n times m differential amplifiers.

The first inputs of the first n differential amplifiers are then each connected to a respective one of the n taps of the first voltage divider 5 and the second inputs of these first n differential amplifiers are all connected to the first tap (12.1) of the second voltage divider 11. The first inputs of the second set of n differential amplifiers are each connected to a respective one of the n taps of the first voltage divider 5 and the second inputs of this second set of n differential amplifiers are all connected to the second tap (12.2) of the second voltage divider 11. This continues up to the m^{th} set of n differential amplifiers, whose first inputs are each connected to a respective one of the taps of the first voltage divider 5 and whose second inputs are all connected to the m^{th} tap (12.6) of the second voltage divider 11. The means 77 should then also be extended so that it is possible to selectively drive individual ones of said n times m differential amplifiers.

It is to be noted that the invention is not limited to the circuit arrangements as shown in the Figures. The invention also applies to circuit

arrangements which differ from the embodiments shown with respect to points which do not relate to the inventive idea. For example, it is possible to employ field effect transistors (such as MOS transistors) instead of bipolar transistors.

Claims

1. A circuit for amplifying and/or attenuating a signal which circuit has an input terminal for receiving an input signal and an output terminal for supplying an output signal, which circuit also comprises an amplifier stage having an inverting input, a non-inverting input, an output which is coupled to the output terminal, a first voltage divider having n taps ($n \geq 2$), which is arranged between the input terminal and a first connection terminal of the circuit and whose taps are connected to a first controllable switching unit for coupling individual ones of these taps to the non-inverting input, and a controllable negative feedback loop from the output terminal to the inverting input comprising a second voltage divider having m taps ($m \geq 2$) which is arranged between the output terminal and a second connection terminal of the circuit and whose taps are connected to a second switching unit for coupling individual ones of these taps to the inverting input of the amplifier, characterized in that the first and the second connection terminals are connected to a point of constant potential, optionally via an impedance each, and in that the control of the first switching unit is independent of the control of the second switching unit.

2. A circuit as claimed in Claim 1, characterized in that at least one voltage divider comprises a series arrangement of a plurality of resistors, the ends of the series arrangement and the junction points of the resistors each constituting a tap.

3. A circuit as claimed in Claim 1 or 2, characterized in that the circuit has a frequency-dependent transmission factor from the input terminal of the circuit to the non-inverting input of the amplifier stage and/or from the output to the inverting input of the amplifier stage.

4. A circuit as claimed in Claims 2 and 3 wherein each said voltage divider comprises a said series arrangement, characterized in that the ends of the series arrangement corresponding to the first voltage divider are coupled to the input terminal of the circuit and to the first connection terminal respectively and the ends of the series arrangement corresponding to the second voltage divider are coupled to the output of the amplifier stage and to the second connection terminal respectively, and said impedance comprises at least a capacitance arranged between the first connection terminal and the second connection terminal respectively and the point of constant potential.

5. A circuit as claimed in Claim 4, characterized in that the first connection terminal is connected to the second connection terminal via a series arrangement of two resistors, and said capacitance is connected between the junction

outputs 75.1, 75.2, ..., etc of all differential amplifiers are coupled to the non-inverting input of the amplifier stage 3. Further the combined switching unit 70 comprises means 77 for selectively energizing individual ones of the differential amplifiers. These means 77 are coupled to the control inputs 76.1, 76.2, ..., etc. of all differential amplifiers. Each differential amplifier comprises two transistors, whose bases are connected to the first input and to the second input respectively, whose collectors are connected to the first output and to the second output respectively, and whose emitters are both connected to the control input of the differential amplifier. The means 77 comprise a plurality of (also $n+m-1$, or eleven) transistors 78.1 to 78.11, whose bases are all connected to a point of constant potential 79 and whose collectors are each connected to a control input of an associated differential amplifier. The emitters of all transistors but one receive a high voltage, so that they are turned off. One transistor receives a low voltage, so that it is turned on. The associated differential amplifier is then selected, that is, only the signals on the first and second inputs of this differential amplifier are transferred to the inputs of the amplifier stage 3 by the combined switching unit 70. By consecutively applying a low voltage to the emitters of the transistors 78.1, 78.2, ... to 78.11 the connection scheme as described with reference to Figures 1 and 4 is obtained. This means that when the switch 8 is in the upper position (i.e. coupled to the tap 6.1), it is possible to select one of the taps 12.1 to 12.6 with the switch 14 and when the switch 14 is in the upper position (i.e. coupled to the tap 12.1) it is possible to select one of the taps 6.1 to 6.6 by means of the switch 4.

If in the combined switching unit 70 an arbitrary one of the taps 6.1 to 6.6 is to be combined with an arbitrary one of the taps 12.1 to 12.6, the combined switching unit should be extended to n times m differential amplifiers.

The first inputs of the first n differential amplifiers are then each connected to a respective one of the n taps of the first voltage divider 5 and the second inputs of these first n differential amplifiers are all connected to the first tap (12.1) of the second voltage divider 11. The first inputs of the second set of n differential amplifiers are each connected to a respective one of the n taps of the first voltage divider 5 and the second inputs of this second set of n differential amplifiers are all connected to the second tap (12.2) of the second voltage divider 11. This continues up to the m^{th} set of n differential amplifiers, whose first inputs are each connected to a respective one of the taps of the first voltage divider 5 and whose second inputs are all connected to the m^{th} tap (12.6) of the second voltage divider 11. The means 77 should then also be extended so that it is possible to selectively drive individual ones of said n times m differential amplifiers.

It is to be noted that the invention is not limited to the circuit arrangements as shown in the Figures. The invention also applies to circuit

arrangements which differ from the embodiments shown with respect to points which do not relate to the inventive idea. For example, it is possible to employ field effect transistors (such as MOS transistors) instead of bipolar transistors.

Claims

1. A circuit for amplifying and/or attenuating a signal which circuit has an input terminal for receiving an input signal and an output terminal for supplying an output signal, which circuit also comprises an amplifier stage having an inverting input, a non-inverting input, an output which is coupled to the output terminal, a first voltage divider having n taps ($n \geq 2$), which is arranged between the input terminal and a first connection terminal of the circuit and whose taps are connected to a first controllable switching unit for coupling individual ones of these taps to the non-inverting input, and a controllable negative feedback loop from the output terminal to the inverting input comprising a second voltage divider having m taps ($m \geq 2$) which is arranged between the output terminal and a second connection terminal of the circuit and whose taps are connected to a second switching unit for coupling individual ones of these taps to the inverting input of the amplifier, characterized in that the first and the second connection terminals are connected to a point of constant potential, optionally via an impedance each, and in that the control of the first switching unit is independent of the control of the second switching unit.

2. A circuit as claimed in Claim 1, characterized in that at least one voltage divider comprises a series arrangement of a plurality of resistors, the ends of the series arrangement and the junction points of the resistors each constituting a tap.

3. A circuit as claimed in Claim 1 or 2, characterized in that the circuit has a frequency-dependent transmission factor from the input terminal of the circuit to the non-inverting input of the amplifier stage and/or from the output to the inverting input of the amplifier stage.

4. A circuit as claimed in Claims 2 and 3 wherein each said voltage divider comprises a said series arrangement, characterized in that the ends of the series arrangement corresponding to the first voltage divider are coupled to the input terminal of the circuit and to the first connection terminal respectively and the ends of the series arrangement corresponding to the second voltage divider are coupled to the output of the amplifier stage and to the second connection terminal respectively, and said impedance comprises at least a capacitance arranged between the first connection terminal and the second connection terminal respectively and the point of constant potential.

5. A circuit as claimed in Claim 4, characterized in that the first connection terminal is connected to the second connection terminal via a series arrangement of two resistors, and said capacitance is connected between the junction



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point of the two resistors and the point of constant potential.

6. A circuit as claimed in Claims 2 and 3, characterized in that the ends of the series arrangement corresponding to the first voltage divider are coupled to the input terminal of the circuit and to the first connection terminal respectively and the ends of the series arrangement corresponding to the second voltage divider are coupled to the output of the amplifier stage and to the second connection terminal respectively, and first and second capacitances are connected between the input terminal of the circuit and one of the taps of the first voltage divider and between the output of the amplifier stage and one of the taps of the second voltage divider respectively.

7. A circuit as claimed in any of the preceding Claims, characterized in that the first and second switching units are incorporated in a combined switching unit, which combined switching unit comprises $n+m-1$ differential amplifiers, which differential amplifiers each have a first input and a second input for receiving a difference signal, a first output and a second output for supplying two output signals which are in phase opposition and which are dependent on the difference signal, and a control input for receiving a control signal, the first inputs of n of the differential amplifiers being each coupled to an associated tap of the first voltage divider, and the first inputs of the remaining $m-1$ differential amplifiers being all coupled to that tap of the first voltage divider which is situated nearest the input terminal of the circuit, the second inputs of said n differential amplifiers being all coupled to that tap of the second voltage divider which is situated nearest the output terminal of the circuit, and the second inputs of the remaining $m-1$ differential amplifiers being each coupled to an associated one of the remaining taps of the second voltage divider, the first outputs and the second outputs of the differential amplifiers coupled to the inverting input and the non-inverting input of the amplifier stage respectively, and the combined switching unit comprising means for selectively energizing individual ones of the differential amplifiers, which means are coupled to the control inputs of all the differential amplifiers.

Revendications

1. Circuit d'amplification et/ou d'atténuation d'un signal, muni d'une borne d'entrée servant à recevoir un signal d'entrée et d'une borne de sortie servant à fournir un signal de sortie, circuit qui comporte en outre un étage amplificateur muni d'une entrée inverseuse, d'une entrée non inverseuse et d'une sortie qui est couplée à la borne de sortie, un premier diviseur de tension à n prises ($n \geq 2$) qui est disposé entre la borne d'entrée et une première borne de raccordement du circuit et dont les prises sont reliées à une première unité de commutation commandable servant à coupler des prises individuelles parmi

ces prises à l'entrée non inverseuse, et un boucle de contre-réaction commandable connectée entre la borne de sortie et l'entrée inverseuse et comportant un second diviseur de tension à m prises ($m \geq 2$) qui est disposé entre la borne de sortie et une seconde borne de raccordement du circuit et dont les prises sont reliées à une seconde unité de commutation servant à coupler, des prises individuelles parmi ces prises à l'entrée inverseuse de l'amplificateur, caractérisé en ce que la première et la seconde borne de raccordement sont reliées à un point à potentiel constant, le cas échéant chacune à travers une impédance, et en ce que la commande de la première unité de commutation est indépendante de la commande de la seconde unité de commutation.

2. Circuit selon la revendication 1, caractérisé en ce qu'il a au moins un diviseur de tension comportant un montage série d'une pluralité de résistances, les extrémités du montage série et les points communs aux résistances constituant chacune une prise.

3. Circuit selon la revendication 1 ou 2, caractérisé en ce qu'il a un facteur de transmission dépendant de la fréquence à partir de la borne d'entrée du circuit jusqu'à l'entrée non inverseuse de l'étage amplificateur et/ou à partir de la sortie jusqu'à l'entrée inverseuse de l'étage amplificateur.

4. Circuit selon l'une des revendications 2 et 3, dans lequel chacun desdits diviseurs de tension comporte l'un desdits montages séries, caractérisé en ce que les extrémités du montage série correspondant au premier diviseur de tension sont couplées respectivement à la borne d'entrée du circuit et à la première borne de raccordement, en ce que les extrémités du montage série correspondant au second diviseur de tension sont couplées respectivement à la sortie de l'étage amplificateur et à la seconde borne de raccordement et en ce que ladite impédance comporte au moins une capacité disposée entre la première borne de raccordement ainsi que la seconde borne de raccordement d'une part et le point à potentiel constant d'autre part.

5. Circuit selon la revendication 4, caractérisé en ce que la première borne de raccordement est reliée à la seconde borne de raccordement à travers un montage série de deux résistances et en ce que ladite capacité est reliée entre le point commun aux deux résistances et le point à potentiel constant.

6. Circuit selon les revendications 2 et 3, caractérisé en ce que les extrémités du montage série correspondant au premier diviseur de tension sont couplées respectivement à la borne d'entrée du circuit et à la première borne de raccordement, en ce que les extrémités du montage série correspondant au second diviseur de tension sont couplées respectivement à la sortie de l'étage amplificateur et à la seconde borne de raccordement et en ce qu'une première et une seconde capacité sont intercalées, l'une entre la borne d'entrée du circuit et l'une des prises du premier diviseur de tension et, l'autre



entre la sortie de l'étage amplificateur et l'une des prises du second diviseur de tension.

7. Circuit selon l'une quelconques des revendications précédentes, caractérisé en ce que la première et la seconde unité de commutation sont incorporées à une unité combinée de commutation comportant $n+m-1$ amplificateurs différentiels munis chacun d'une première entrée et d'une seconde entrée servant à recevoir un signal de différence, d'une première sortie et d'une seconde sortie servant à fournir deux signaux de sortie qui sont en opposition de phase et qui dépendent du signal de différence, et d'une entrée de commande servant à recevoir un signal de commande, les premières entrées de n amplificateurs différentiels étant couplées chacune à une prise associée du premier diviseur de tension et les premières entrées des $m-1$ amplificateurs différentiels restants étant toutes couplées à la prise du premier diviseur de tension la plus rapprochée de la borne d'entrée du circuit, alors que les secondes entrées desdites n amplificateurs différentiels étant toutes couplées à la prise du second diviseur de tension la plus rapprochée de la borne de sortie du circuit, que les secondes entrées des $m-1$ amplificateurs différentiels sont couplées chacune à une prise associée des prises restantes du second diviseur de tension, que les premières sorties et les secondes sorties des amplificateurs différentiels sont couplées respectivement à l'entrée inverseuse et à l'entrée non inverseuse de l'étage amplificateur et que l'unité combinée de commutation comporte des moyens servant à exciter de façon sélective des amplificateurs individuels parmi les amplificateurs différentiels, moyens qui sont couplés aux entrées de commande de tous les amplificateurs différentiels.

Patentansprüche

1. Signalverstärkungs- und/oder Dämpfungsschaltung mit einem Eingang für den Empfang eines Eingangssignals und einem Ausgang für die Ausgabe eines Ausgangssignals, weiter bestehend aus einer Verstärkerstufe mit einem invertierenden Eingang, mit einem nichtinvertierenden Eingang, mit einem Ausgang in Verbindung mit dem Schaltungsausgang, einem ersten Spannungsteiler mit n Anzapfungen ($n \geq 2$), der zwischen dem Schaltungseingang und einem ersten Verbindungsanschluss der Schaltung angeordnet ist und dessen Anzapfungen an eine erste steuerbare Schalteinheit zum Verbinden einzelner dieser Anzapfungen mit dem nichtinvertierenden Eingang angeschlossen sind, und einem steuerbaren Gegenkopplungsweg vom Schaltungsausgang zum invertierenden Eingang mit einem zweiten Spannungsteiler mit m Anzapfungen ($m \geq 2$), der zwischen dem Schaltungsausgang und einem zweiten Verbindungsanschluss angeordnet ist und dessen Anzapfungen an eine zweite Schalteinheit zum Verbinden einzelner dieser Anzapfungen an den

invertierenden Eingang des Verstärkers angeschlossen sind, dadurch gekennzeichnet, dass die ersten und zweiten Verbindungsanschlüsse an einen Punkt mit konstantem Potential, wahlweise über je eine Impedanz, angeschlossen sind, und dass die Steuerung der ersten Schalteinheit von der Steuerung der zweiten Schalteinheit unabhängig ist.

2. Schaltung nach Anspruch 1, dadurch gekennzeichnet, dass zumindest ein Spannungsteiler eine Serienanordnung mit einer Anzahl von Widerständen enthält und dass die Enden der Serienanordnung und die Knotenpunkte der Widerstände je eine Anzapfung bilden.

3. Schaltung nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass die Schaltung einen frequenzabhängigen Übertragungsfaktor vom Schaltungseingang zum nichtinvertierenden Eingang der Verstärkerstufe und/oder vom Ausgang zum invertierenden Eingang der Verstärkerstufe besitzt.

4. Schaltung nach Anspruch 2 oder 3, in der jeder Spannungsteiler eine erwähnte Serienanordnung enthält, dadurch gekennzeichnet, dass die Enden der Serienanordnung des ersten Spannungsteilers an den Schaltungseingang und an den ersten Verbindungsanschluss und die Enden der Serienanordnung des zweiten Spannungsteilers an den Ausgang der Verstärkerstufe bzw. an den zweiten Verbindungsanschluss angeschlossen sind, und dass die Impedanz zumindest eine Kapazität zwischen dem ersten Verbindungsanschluss bzw. dem zweiten Verbindungsanschluss und dem Punkt mit konstantem Potential enthält.

5. Schaltung nach Anspruch 4, dadurch gekennzeichnet, dass der erste Verbindungsanschluss an den zweiten Verbindungsanschluss über eine Serienanordnung zweier Widerstände angeschlossen ist, und dass die Kapazität zwischen dem Knotenpunkt der beiden Widerstände und dem Punkt mit konstantem Potential angeschlossen ist.

6. Schaltung nach Anspruch 2 oder 3, dadurch gekennzeichnet, dass die Enden der Serienanordnung des ersten Spannungsteilers an den Schaltungseingang bzw. an den ersten Verbindungsanschluss und die Ausläufer der Serienanordnung des zweiten Spannungsteilers an den Ausgang der Verstärkerstufe bzw. an den zweiten Verbindungsanschluss angeschlossen sind, und dass erste und zweite Kapazitäten zwischen dem Schaltungseingang und einer der Anzapfungen des ersten Spannungsteilers und zwischen dem Ausgang der Verstärkerstufe und einer der Anzapfungen des zweiten Spannungsteilers angeschlossen sind.

7. Schaltung nach einem oder mehreren der vorangehenden Ansprüche, dadurch gekennzeichnet, dass die erste und zweite Schalteinheit in eine kombinierte Schalteinheit aufgenommen sind, die $n+m-1$ Differenzverstärker mit je einem ersten Eingang und einem zweiten Eingang für den Empfang eines Differenzsignals, einem ersten Ausgang und einem zweiten Aus-



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gang für die Ausgabe von zwei Ausgangssignalen, die in Gegenphase und anhängig vom Differenzsignal sind, und einem Steuereingang für den Empfang eines Steuersignals enthalten, dass die ersten Eingänge von n Differenzverstärkern mit je einer zugeordneten Anzapfung des ersten Spannungsteilers und die ersten Eingänge der rechtlichen $m-1$ Differenzverstärker mit jener Anzapfung des ersten Spannungsteilers verbunden sind, die sich in der Nähe des Schaltungseingangs befinden, dass die zweiten Eingänge der n Differenzverstärker mit jener Anzapfung des zweiten Spannungsteilers verbunden sind, die sich in der Nähe des

Schaltungsausgangs befinden, und die zweiten Eingänge der rechtlichen $m-1$ Differenzverstärker mit einer zugeordneten Anzapfung der restlichen Anzapfungen des zweiten Spannungsteilers verbunden sind, dass die ersten Ausgänge und die zweiten Ausgänge der Differenzverstärker mit dem invertierenden bzw. dem nichtinvertierenden Eingang der Verstärkerstufe verbunden sind, und dass die kombinierte Schalteinheit Mittel zum selektiven Aktivieren einzelner der Differenzverstärker enthält, was bedeutet, dass sie an die Steuereingänge aller Differenzverstärker angeschlossen sind.

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