

systems beyond 32KB. The 82385 specifications and functional description can be found in the Intel "Microprocessor and Peripheral Handbook" and in "82385 High Performance 32-Bit Cache Controller" (1987). See also "Introduction to the 80386" and the 80386 Hardware Reference Manual (1986) also from Intel.

It is an object of the present invention to ameliorate one or more disadvantages of the prior art.

According to one aspect of the present invention there is provided a multi-bus microcomputer system comprising: a CPU and a cache subsystem connected together by a CPU local bus, said cache subsystem including a cache controller and a cache memory, system bus means connecting said cache controller to a random access memory and a plurality of addressable functional units; wherein said CPU has CPU addressing outputs and said cache controller has addressing inputs; and means connecting some of said CPU addressing outputs to some of said addressing inputs of said cache controller so that said some of said CPU addressing outputs are not connected to corresponding addressing inputs of said cache controller.

According to another aspect of the present invention there is provided a multi-bus microcomputer system comprising: a CPU and a cache subsystem connected together by a CPU local bus; said cache subsystem comprising an 82385 cache controller and a cache memory; said CPU including CPU addressing outputs; means connecting some of said CPU addressing outputs to addressing inputs of said 82385 cache controller so that said CPU addressing outputs are not connected to corresponding 82385 cache controller addressing inputs; system bus means connecting said 82385 cache controller to a random access memory and a plurality of addressable functional units; address logic generator means for generating an addressing input to said cache memory, means connecting at least one of said CPU addressing outputs to said address logic generator means, and means connecting CPU addressing outputs to said cache memory; and wherein said cache memory has a capacity of at least 64 Kbytes.

An embodiment of the present invention to be described later provides an architecture and a method for increasing the cache RAM supportable by an 82385 cache controller to at least 64KB. This architecture can also be used on any cache controller designed to support a given amount of cache RAM and provide the capability of at least doubling that cache RAM. The technique described herein to increase or double the cache RAM size does not require additional tag RAM and only requires a minimal amount of additional support logic.

**CLAIMS****1. A multi-bus microcomputer system comprising:**

a CPU and a cache subsystem connected together by a CPU local bus, said cache subsystem including a cache controller and a cache memory, system bus means connecting said cache controller to a random access memory and a plurality of addressable functional units;

wherein said CPU has CPU addressing outputs and said cache controller has addressing inputs; and

means connecting some of said CPU addressing outputs to some of said addressing inputs of said cache controller so that said some of said CPU addressing outputs are not connected to corresponding addressing inputs of said cache controller.

**2. A multi-bus microcomputer system as recited in claim 1 which further includes:**

address logic generator means for generating an addressing input to said random access memory and means connecting at least one of said CPU addressing outputs to said address logic generator means.

**3. A multi-bus microcomputer system as recited in claim 1 or 2 wherein said cache controller is an 82385 cache controller, and wherein said cache memory has at least 64 Kbyte capacity.****4. A multi-bus microcomputer as recited in claim 2 wherein the addressing input to said random access memory generated by said address logic generator means differs from address signals at said CPU addressing outputs.****5. A multi-bus microcomputer system as recited in claim 1 which further includes:**

address logic generator means for generating an addressing input to said cache memory and means connecting at least one of said CPU addressing outputs to said address logic generator means.

**6. A multi-bus microcomputer system as recited in claim 5 wherein:**

said address logic generator means also generates an addressing input to said random access memory.

7. A multi-bus microcomputer as recited in claim 6 wherein the addressing input to said random access memory generated by said address logic generator means differs from address signals at said CPU addressing outputs.

8. A multi-bus microcomputer as recited in claim 5 wherein the addressing input to said cache memory generated by said address logic generator means differs from address signals at said CPU addressing outputs.

9. A multi-bus microcomputer system comprising:

a CPU and a cache subsystem connected together by a CPU local bus;

said cache subsystem comprising an 82385 cache controller and a cache memory;

said CPU including CPU addressing outputs;

means connecting some of said CPU addressing outputs to addressing inputs of said 82385 cache controller so that said CPU addressing outputs are not connected to corresponding 82385 cache controller addressing inputs;

system bus means connecting said 82385 cache controller to a random access memory and a plurality of addressable functional units;

address logic generator means for generating an addressing input to said cache memory, means connecting at least one of said CPU addressing outputs to said address logic generator means, and means connecting CPU addressing outputs to said cache memory; and

wherein said cache memory has a capacity of at least 64 Kbytes.

10. A multi-bus microcomputer as recited in claim 9 wherein the addressing input to said cache memory generated by said address logic generator means differs from address signals at said CPU addressing outputs.

11. A multi-bus microcomputer system as recited in claim 9 wherein:

said address logic generator means generates an addressing input to said random access memory.

12. A multi-bus microcomputer as recited in claim 11 wherein the addressing input to said random access memory generated by said address logic generator means differs from address signals at said CPU addressing outputs.

13. A multi-bus microcomputer system as recited in claim 11 or 2 which further includes hidden cycle initiating means coupled to said CPU and to said cache controller and responsive to a cache read miss identified by said cache controller for generating a hidden memory read cycle.

14. A multi-bus microcomputer system as recited in claim 11 or 2 wherein CPU addressing outputs A3 through A30 are connected to addressing inputs CCA2 through CCA29 of said cache controller and CPU addressing output A2 is connected to said address logic generator means.

**MICROCOMPUTER SYSTEM EMPLOYING ADDRESS OFFSET MECHANISM TO  
INCREASE THE SUPPORTED CACHE MEMORY CAPACITY**

**ABSTRACT**

The capacity of cache memory (255) supported by a cache controller (260) can be increased by offsetting the relationship between CPU address output terminals and address input terminals of the cache controller and correspondingly doubling the cache line size. In some cases, additional logic generates a hidden memory cycle so as to fetch from memory that number of bytes equal to the new line size regardless of the width of the data bus. The hidden memory cycle is initiated by a read miss and further logic generates a memory address which is not generated by the CPU. The hidden memory cycle is maintained transparent to the CPU and cache controller by inhibiting the change in a READY signal until completion of both the normal memory cycle and the hidden memory cycle.

Fig. 2