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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

Improvements in and relating to Semiconductor Devices

We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices comprising an envelope within which is situated a semiconductor body having electrodes, at least three connection pins passing through the wall of the envelope, the semiconductor body being secured through one of its electrodes to an end portion of one of the said connection pins, hereinafter termed the supporting connection pin, two further electrodes of the semiconductor body being connected through conductors to the two further connecting pins.

The invention further relates to circuit arrangements comprising such semiconductor devices.

The wall of the envelope is to be understood to mean not only the wall of a hollow envelope, but also the surface of a solid envelope for example, a solid envelope of resinous material.

It has been found that when using such a semiconductor device in circuit arrangements, the favourable properties of the circuit element which is realized in the semiconductor body often cannot be used to full advantage, because in some circumstances less favourable properties of the remaining parts of the semiconductor device play too large a part. Some of these undesirable properties are the capacitances which may occur between the various connection pins. In circuit arrangements in which one of the connection pins is common to the electric input and to the electric output of

the circuit, the capacitance which occurs between the connection pin to which the electric signals are applied and the connection pin from which the electric signals are derived may cause a disturbing feedback coupling between the electric input and the electric output of the semiconductor device. For example, when a transistor is used in such a circuit arrangement, for example, a common emitter circuit or a common base circuit, for amplifying electric signals, the possible amplification which can be obtained with the said circuit can be restricted by the said capacitance which causes feedback coupling.

In order to reduce said capacitance which causes feedback coupling between the connection pins, it has already been proposed to use three straight, parallel juxtaposed connection pins in which the central connection pin may be used to screen the two outermost pins from one another. For that purpose the central connection pin is connected to the electrode of the semiconductor body which in the circuit is common to the input circuit and to the output circuit of the semiconductor device. For example, in transistors for use in common emitter circuits, the emitter, and in transistors for use in common base circuits, the base, is connected to the central connection pin.

The result of this screening is that instead of the capacitance which causes the feedback coupling between the two outermost connection pins, which is substantially entirely avoided, capacitances occur between each of the outermost connection pins and the central connection pin. The two latter capacitances occur at the input and at the output, respectively, of the semiconductor device and in most circuits are not annoying or are annoying at least to a considerably smaller extent.

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As already stated the semiconductor body is often secured, through one of its electrodes, to the supporting connection pin. The last-mentioned electrode usually is not the electrode which in a circuit is common to the input circuit and to the output circuit. In that case the two further connection pins consequently are located beside each other on the same side of the supporting connection pin. However there are various reasons why it may be desirable that the two further connection pins extend on opposite sides of the semiconductor body. For example, in the latter case the conductors which connect the further electrodes of the semiconductor body to the further connection pins may both be constructed so as to have a very short length which may be of importance for the behaviour of the semiconductor device at high frequencies, *inter alia* in connection with induction phenomena. In addition, when the two conductors between the semiconductor body and the further connection pins extend in the same direction it may easily occur that the conductors touch each other so that a shortcircuit occurs. In addition it may be highly desirable, from a point of view of manufacture, that the conductors extend in substantially opposite directions. In fact, this enables the four connection points of the two conductors to be located substantially on a straight line. It has been found that four connection points which are located substantially on a straight line can often be mass-produced more rapidly and consequently more cheaply than four connection points which are not located on a straight line.

In order to meet these requirements it has already been proposed to extend the end portion of the supporting connection pin around the extremity of the central connection pin, the one further connection pin, the extremity of the supporting connection pin becoming located between the end portions of the two further connection pins.

However, in this case, the end of the supporting connection pin is no longer screened from further connection pin by the one further connection pin. As a result of this the capacitance which causes feedback coupling is again increased.

The capacitance which causes feedback coupling may also be reduced already in a different manner, namely by using connection pins which extend in different directions, instead of connection pins which are located beside each other. For example, semiconductor devices are known in which two connection pins extend substantially in opposite directions while a third connection pin is arranged at right angles to said pin. However, it will be obvious that in

these cases also further screening is of importance because in fact the end portions of the connection pins extend in the proximity of each other.

The invention is based *inter alia* on the recognition that it is possible, with a comparatively simple configuration of connection pins to avoid the disadvantages of the above described configurations.

According to a first aspect of the invention, a semiconductor device comprises an envelope within which is situated a semiconductor body having electrodes, at least three connection pins passing through the wall of the envelope, the semiconductor body being secured through one of its electrodes to an end portion of one of the connection pins, hereinafter termed the supporting connection pin, two further electrodes of the semiconductor body being connected through conductors to the two further connection pins, one of the two further connection pins comprising a first, electrically screening part which is located between the end portion of the supporting connection pin and a part of the other further connection pin, said one further connection pin also comprising a second part located adjacent the end portion of the supporting connection pin on the opposite side of the semiconductor body to the first, electrically screening part; the conductor which connects the one further connection pin to a further electrode of the semiconductor body being connected to said second part, the said first and second parts being united within the envelope.

This configuration in which the end portion of the supporting connection pin is located between two parts of the one further connection pin gives in a simple manner a good screening of the supporting connection pin and the other further connection pin, while it is not necessary for the two conductors between the semiconductor body and the further connection pins to extend in the same direction.

The conductors may extend substantially in opposite directions, as a result of which the connection points of the conductors to the further connection pins and to the further electrodes of the semiconductor body, viewed in a direction substantially at right angles to the largest cross-section of the semiconductor body, are located substantially on a straight line.

An important advantage of this location of the connection points is that in mass production four connection points located on a straight line can be provided more rapidly and consequently more cheaply than four connection points which are not located on a straight line.

The supporting connection pin, at least the first and second parts of the one further

connection pin which are located on opposite sides of the semiconductor body adjacent the end portion of the supporting connection pin, and the other further connection pin may tie substantially throughout their length inside the envelope in a common plane of intersection.

It has been found that from a point of view of manufacture it is advantageous if the connection pins are located in a common plane as far as possible while in addition a very good screening is obtained.

Alternatively, the directions in which the supporting and the further connection pins pass through the wall of the envelope may be parallel to the same plane. For clearness, sake it is to be noted that if reference is made herein to directions in which the connection pins pass through the wall of the envelope the said directions are all considered in a corresponding manner, that is to say either all of them from within the envelope to outside the envelope or conversely all of them from outside the envelope to within the envelope.

The connection pins may be in the form of wires which are flattened at least at the area where the semiconductor body and the conductors are secured thereto; the major surfaces of the flattened parts of the connection pins being located substantially in one plane. These filamentary connection pins which are comparatively cheap can easily be bent in any desired direction while the semiconductor device can in addition be accommodated in electric circuit arrangements by means of the normally used standardized sockets which are adapted to circular connection pins.

The flattened parts of the connection pins render the connection of the semiconductor body and the conductors to the connection pins possible in a simple manner.

The connection pins may be metal strips the major surfaces of which, at least in as far as the connection pins have a common plane of intersection, are substantially parallel to said plane of intersection.

The connection pins can be manufactured simultaneously from one metal sheet, while, for example, the connection pins may initially be connected together by connection strips which can be removed in a later stage of the manufacture.

The semiconductor device may have various forms, for example, a field-effect transistor either of the *p-n* junction gate or insulated gate form. The device may be a bipolar transistor having an emitter, a base and a collector electrode in which the semiconductor body is connected to the supporting connection pin *via* the collector, while the base and the emitter electrodes of the semiconductor body are connected through the conductors to the further connection

pins.

The semiconductor body may be, for example, that of a planar transistor, a mesa-transistor or an alloy-diffusion transistor which is connected in normal manner to the supporting connection pin, in this case the collector pin. The two conductors may be connected to alloyed or vapour-deposited emitter and base contacts. In transistors which are destined for use in common emitter circuits, the emitter, and in transistors which are destined for use in common base circuits, the base of the semiconductor body is connected to the one further connection pin.

In one preferred form the connection pins pass through the wall of the envelope substantially in the same direction.

In addition the invention is of particular use in transistors which are embedded in an envelope of resinous material. It has been found that the possible amplification which can be obtained with such transistors is smaller than that of a transistor of the same type but having a metal envelope which can be evacuated or is filled, for example, with an inert gas. This is due *inter alia* to the fact that the dielectric constant of the resinous material of the envelope is larger than that of an inert gas or of a vacuum and consequently the capacitance causing feedback coupling which restricts the possible amplification likewise is larger in the case of an envelope of resinous material.

Nevertheless the use of a transistor having an envelope of resinous material in which the transistor is embedded is desirable since a transistor having an envelope of resinous material may be considerably cheaper than a transistor having a metal envelope or having an envelope of an insulating material such as ceramic material, which is filled with a gas, possible under a reduced pressure.

Thus in one form of a transistor in accordance with the invention, the semiconductor body is embedded in a resinous material, the connection pins projecting from said resinous material and the envelope of the transistor consisting exclusively of the said resinous material.

In one form of such a transistor the connection pins inside the envelope of resinous material extend beside one another from a surface of the envelope of resinous material, the one further connection pin being located between the other further connection pin and the supporting connection pin, the supporting connection pin extending around the second part of the one further connection pin, the end portion of the supporting connection pin which supports the semiconductor body being located between the first and second parts of the one further connection pin.

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In one form of a device in accordance with the invention in which the connection pins pass through the wall of the envelope substantially in the same direction, inside the envelope the one further connection pin is divided into two branches, one branch comprising the first, screening part and the other branch comprising the second part of the one further connection pin, the supporting connection pin extending around said other branch, the end portion of the supporting connection pin which supports the semiconductor body being located between the two branches of the one further connection pin, the part of the one further connection pin stemming from the branches being located, at least for part of its length, between a part of the supporting connection pin and a part of the other further connection pin and passing through the wall of the envelope. The separate screening branch which does not convey current may be narrow so that the conductor which connects an electrode of the semiconductor body to the other further connection pin may have a short length, if desired.

A satisfactory screening may alternatively be achieved in another configuration of connection pins in which at least the two parts of the one further connection pin and the other further connection pin lie inside the envelope substantially throughout their length in a common plane of intersection. In this configuration the first, screening part of the one further connection pin adjoins on one side a portion of said pin which passes through the wall of the envelope and adjoins on the opposite side a portion of said pin which lies entirely in the common plane of intersection and which extends around the end portion of the supporting connection pin, this also forming the second part of the one further connection pin.

It will be obvious that in this configuration a satisfactory screening is obtained by means of one suitably shaped connection pin without an additional screening conductor while in addition the two conductors may be substantially in alignment. In addition, as a result of the portion which extends around the end portion of the supporting connection pin, the supporting connection pin is screened somewhat better while the supporting connection pin in this case may be comparatively short so that the surface of said connection pin which also determines the remaining capacitive cross-talk, is comparatively small.

In semiconductor devices which are specially destined for use at very high frequencies it has already been proposed to reduce the capacitances between the connection pins by passing the connection pins in different directions through the wall of the envelope. As was already noted before, devices in ac-

cordance with the invention may have this form because at very high frequencies a good screening becomes more important. In one such semiconductor device in accordance with the invention the direction in which the one further connection pin passes through the wall of the envelope is approximately at right angles to the directions in which the supporting connection pin and the other further connection pin pass through the wall of the envelope.

The expression "approximately at right angles to" should be interpreted to have a wide meaning so that it includes, for example, configurations in which each of the connection pins encloses an angle of 120° with each of the other two connection pins. From a point of view of manufacture, however, two connection pins which extend substantially in opposite directions, will preferably be combined with a third connection pin which extends substantially at right angles to said directions, because such a configuration generally is more favourable in electrical respects and in addition often gives a smaller loss of material.

In one semiconductor device of the last-mentioned form in which the one further connection pin passes through the wall of the envelope approximately at right angles to the directions in which the supporting connection pin and the other further connection pin pass through the wall of the envelope, the one further connection pin is divided inside the envelope into two branches: one branch comprising the first, screening part and the other branch comprising the second part of the one further connection pin, the end portion of the supporting connection pin extending to a position between the two branches and the other further connection pin extending to a position adjacent the first, screening part of the one further connection pin.

A further favourable configuration of a semiconductor device in accordance with the invention is a transistor in which the semiconductor body is connected to the supporting connection pin through the collector, the base and emitter electrodes of the semiconductor body being connected through the conductors to the further connecting pins, the two further connection pins extending in substantially opposite directions from the wall of the envelope, the three connection pins lying substantially throughout their length inside the envelope in a common plane of intersection, a screening conductor is connected to the one further connection pin and extends around the end portion of the collector pin supporting the semiconductor body to a position between the collector pin and the other further connection pin, the free end of the screening conductor constituting the first, screening

part of the one further connection pin.

As already stated the envelope may be of resinous material; the semiconductor body with parts of the connection pins, being embedded in said resinous material. Alternatively, however, an envelope may be used, the space of which contains a gas and the walls of the envelope consist of an electrically insulating material.

According to a second aspect of the invention in a circuit arrangement comprising a semiconductor device in accordance with the invention, the one further connection pin is common to the input circuit and to the output circuit, the input signals being applied to one of the two connection pins constituted by the other further connection pin and the supporting connection pin, and the output signals being derived from the other of the said two connection pins.

Embodiments of the invention will now be described in greater detail, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Fig. 1 shows a plan view of a semiconductor device in accordance with the invention which is shown included in a circuit arrangement in accordance with the invention, in which, for showing the structure inside the envelope, the envelope is not shown while the wall of the envelope is denoted diagrammatically only by a dot-and-dash line;

Fig. 2 shows a cross-sectional view of the said semiconductor device taken on the line II-II of Fig. 1;

Fig. 3 shows a plan view of another semiconductor device in accordance with the invention in which the wall of the envelope is shown diagrammatically only by a dot-and-dash line;

Fig. 4 shows a sectional view taken on the line IV-IV of Fig. 3;

Fig. 5 shows a plan view of a third semiconductor device in accordance with the invention with the upper side of the envelope removed to show the inner construction of the envelope;

Fig. 6 shows a cross-sectional view taken on the line VI-VI in Fig. 5;

Fig. 7 shows a similar cross-sectional view to Fig. 6 of another semiconductor device in accordance with the invention;

Fig. 8 shows a plan view of a further semiconductor device in accordance with the invention, in which the wall of the envelope is diagrammatically shown by a dot-and-dash line;

Fig. 9 is a side elevation of the device shown in Figure 8 viewed in a direction which is denoted by the arrow A in Fig. 8;

Fig. 10 shows a similar plan view to Fig. 8 of another semiconductor device in accordance with the invention but having a different construction; and

Fig. 11 to 14 are circuit diagrams of circuit arrangements in accordance with the invention.

The semiconductor device 1 shown in Fig. 1 and 2 comprises three connection pins 2, 3 and 4 which are passed through the wall 5 of an envelope. The semiconductor body 7 comprising electrodes is secured through one of its electrodes, to an end portion 6 of the supporting connection pin 4, and two further electrodes 14 and 15 of the semiconductor body 7 are respectively connected through conductors 8 and 9 to the two further connection pins 2 and 3. The one connection pin 3 of the two further connection pins 2 and 3 comprises a first, screening part 10 which is located between the end portion 6 of the supporting connection pin 4 and a part 11 of the other further connection pin 2. The one further connection pin 3 comprises, in addition to the first, screening part 10 which electrically screens the parts 6 and 11 from each other, a second part 12 which is located on the opposite side of the semiconductor body 7 to the part 10 adjacent the end portion 6 of the supporting connection pin 4. To this second part 12 there is secured the conductor 9 which connects the one further connection pin 3 to a further electrode of the semiconductor body 7. The two parts 10 and 12 are joined to one another inside the envelope.

The conductors 8 and 9 are substantially in alignment, the connection points 13 and 16 of these connection conductors 8 and 9 to the connection pins 2 and 3 and the further electrodes 14 and 15 of the semiconductor body 7 being located substantially on a common straight line. This is important because four connection points of two conductors 8 and 9 located substantially on a straight line can be obtained by machines much more rapidly in general than the case when the connection points are not located on a common straight line. In Figure 1 the connection points lie on the line II-II. In Figure 2, the electrodes 14 and 15 are located somewhat above the line joining the connection points 13 and 16. The important feature for the manufacture, however, is that the connection points, viewed in a direction at right angles to the largest cross-section of the semiconductor body 7 in Figure 1, in a direction at right angles to the plane of the drawing are located substantially on a straight line.

The parts 10 and 12 of the connection pin 3 and the connection pins 2 and 4 lie on a common plane of intersection, in Figure 1 the plane of the drawing. The connection pins 2, 3 and 4 consist of metal strips the major surfaces of which extend substantially parallel to the common plane of intersection. As a result of this, these connection pins

can be manufactured simultaneously from one metal sheet.

The connection pins 2, 3 and 4 pass through the wall of the envelope substantially in the same direction, the one further connection pin 3 being divided inside the envelope into two branches, one branch comprising the first, screening part 10 and the other branch comprising the second part 12, the supporting connection pin 4 extending around the second part 12 of the other branch, the end portion 6 of the supporting connection pin 4 on which the semiconductor body 7 is secured being located between the two parts 10 and 12 of the one further connection pin 3. The part 17 of the one further connection pin 3 which passes through the wall of the envelope and which stems from the branches is located between the supporting connection pin 4 and the other further connection pin 2. In this configuration the connection pins 2 and 4 are electrically screened from one another not only by the part 10 but also by the part 17 of the connection pin 3.

The semiconductor body 7 may be that, for example, of a planar transistor, a mesa-transistor or an alloy-diffused transistor and may be manufactured, including the envelope, from normal materials in a manner commonly used in semiconductor technology. The conductors 8 and 9 may be connected, for example, by thermocompression bonding, to vapour-deposited or alloyed base and emitter contacts 14 and 15, while the semiconductor body 7 is connected through the collector to the supporting connection pin 4, for example, by soldering and/or alloying.

In accordance with the fact whether the transistor is destined for use in a common base or a common emitter circuit configuration, the base or the emitter, respectively, of the semiconductor body 7 is connected, through the conductor 9 to the one further connection pin 3, and the emitter or the base, respectively, of the semiconductor body 7 is connected through the conductor 8 to the other further connection pin 2.

As envelopes there may be employed the commonly used forms of envelopes, for example, hermetically sealed envelopes in which the connection pins which are passed through the wall of the envelope are insulated electrically from the metal part of the wall, for example, by means of glass. In the present example, the envelope consists of resinous material. The semiconductor body 7 of the transistor is embedded in the resinous material while the connection pins 2, 3 and 4 project from this resinous material only partly and the envelope consists exclusively of this resinous material. The wall 5 of the envelope is constituted by the surface of the embedding of resinous

material. The connection pins 2, 3 and 4 inside the envelope of resinous material extend beside each other from the surface 5, the one further connection pin 3 being located between the other further connection pin 2 and the collector pin 4. The collector pin 4 extends around the second part 12 of the one further connection pin 3, the end portion 6 of the collector pin which supports the semiconductor body 7 being located between the first, screening part 10 and the second part 12 of the one further connection pin 3.

The envelope may consist, for example, of a thermosetting or a thermoplastic plastics or another resinous material which is commonly used in encapsulating semiconductor devices. If desired, the envelope of resinous material may alternatively be constructed from layers of different resinous materials. The dimensions of the envelope of resinous material in this embodiment are 7 x 5 x 4 mms.

The conductors 8 and 9 consist in this embodiment of aluminium wires having a diameter of approximately 20 μ .

The connection pins 2, 3 and 4 may consist of materials commonly used for connection pins, for example, a iron-cobalt-nickel alloy. The width of the connection pins 2, 3 and 4 near the wall 5 of the envelope is in this embodiment approximately 1.2 mms and the thickness of the metal strip is in this embodiment approximately 0.2 mm. The distance between centres of the two adjacent connection pins 2 and 3 is approximately 2.5 mms at the area where they pass through the wall 5 of the envelope. The dimensions of the semiconductor body 7 in this embodiment are approximately 0.4 mm x 0.4 mm x 100 μ .

Experiments carried out have shown that by means of the above described configuration of the connections pins in accordance with the invention the possible amplification of a transistor can be increased by 20 to 30 %.

In the semiconductor device shown in Figures 3 and 4, corresponding components are denoted by the same reference numerals as in Figures 1 and 2. In this embodiment, the directions in which the supporting connection pin 4 and the further connection pins 2 and 3 pass through the wall 5 of the envelope are parallel to the same plane and the direction in which the one further connection pin 3 passes through the wall 5 of the envelope substantially at right angles to the directions in which the supporting connection pin 4 and the other further connection pin 2 pass through the wall 5 of the envelope.

Such a configuration is especially used for high frequencies, because only the ends of the connection pins 2, 3 and 4 come in the

proximity of each other so that the stray capacities between the connection pins are comparatively small.

Inside the envelope the one further connection pin 3 is divided into two branches, one branch comprising the first, screening part 10 and the other branch comprising the second part 12, the end portion 6 of the supporting connection pin 4 extending to a position between the two branches and the other further connection pin 2 extending adjacent the first, screening part 10.

The semiconductor body, the conductors, the connection pins and the envelope may be constructed from the same materials as used in the previously described embodiment.

For use as high frequencies the configuration shown in Figures 3 and 4 is particularly suitable in combination with an envelope consisting of a wall of electrically insulating material, for example, glass, a resinous material or a ceramic material, the space inside the envelope being filled with a gas.

Another semiconductor device in accordance with the invention in which the connection pins pass through the wall of the envelope in different directions will now be described with reference to Figures 5 and 6. This device is a transistor 50 having a supporting connection pin 53, the collector pin, passing through the wall 51 of the envelope on which pin in the proximity of its extremity the semiconductor body 52 is secured through the collector. Two further connection pins 54 and 55 pass through the wall 51 of the envelope and extend approximately in opposite directions from the wall 51 to the proximity of the end of the collector pin 53. The pins 54 and 55 are connected by conductors 56 and 57 to the emitter electrode and the base electrode of the transistor respectively. Inside the envelope the three connection pins 53, 54 and 55 have a common plane of intersection, substantially throughout their length. A screening conductor 58 is connected inside the envelope to the one further connection pin 54, and comprises a part which extends around the end portion of the collector pin 53 supporting the semiconductor body 52 and has a part 59 between the collector pin 53 and the other further connection pin 55, the part 59 constituting the first, electrically screening part of the one further connection pin 54.

In this embodiment also, the connection points 60 to 63 are located substantially on a straight line, in Figure 5 the line VI-VI.

The screening conductor 58 may alternatively consist of an elongation of the connection pin 54 which is bent below the collector pin 53. In that case, the cross-section shown in Figure 7 is obtained instead of the cross-section shown in Figure 6.

This latter embodiment, however, is somewhat more difficult to obtain because the connection pins are no longer located on one plane. Thus if the connection pins are constructed in the form of metal strips, they cannot readily be manufactured simultaneously from one flat metal sheet.

The envelope consists, for example, of a circular box of insulating material, for example, ceramic material. The two halves of the envelope, which each comprise recesses in the edges for the connection pins 53 to 55, are secured together by suitable adhesive means after the interposition of the connection pins. The diameter of the envelope is, for example, approximately 4 mms and the height approximately 1.5 mms.

Figures 8 and 9 show a transistor 80 in which connection pins 81, 82 and 83 are manufactured from metal wires. The filamentary connection pins 81, 82 and 83 are flattened at the area where a semiconductor body 84 and the conductors 85 and 86 are secured thereto, the large connection surfaces of the flattened parts 87, 88 and 89 being substantially located in one plane, in Figure 8 in the plane of the drawing.

These wire-form connection pins will be used, for example, when the semiconductor device is destined to be incorporated in a circuit arrangement by means of the commonly used types of sockets having circular contact sleeves. The diameter of the metal wires is for example, approximately 0.4 mm and they are manufactured, for example, from nickel.

A first screening part 90 of the one further connection pin 82 adjoins on one side a portion 91 of said pin which passes through the wall 93 of the envelope and adjoins on the opposite side a portion 92 of said pin which lies entirely in the common plane of intersection, in Figure 8 the plane of the drawing, and which extends around the end portion 88 of the supporting connection pin 81 thus also constituting the second part 87 of the one further connection pin 82.

It will be obvious that in this case a satisfactory screening is obtained in a particularly simple manner. The elongation 92, 87 of the one further connection pin 91 makes a separate screening conductor superfluous so that branching of the one further connection pin is no longer necessary.

It is shown in Figure 9 that in the present embodiment the connection pins 81, 82 and 83 do not have a common plane of intersection throughout their length inside the wall 92 of the envelope of the transistor 80. The one further connection pin 82 is curved so that the connection pins 81, 82 and 83 outside the envelope are not located in one plane.

This curvature may take place both outside and inside the envelope. In the latter

case, however, it will be effected preferably as near to the wall 93 of the envelope as it is possible, to keep the screening action of the one further connection pin 82 as large as possible.

Such a curvature will be used, for example, when the semiconductor device is destined for being incorporated in a circuit arrangement *via* the commonly used types of sockets in which the contact sleeves are not located on a straight line.

Figure 10 shows a somewhat different embodiment in which corresponding components are denoted by the same reference numerals as in Figure 8. The connection pins 81, 82 and 83 in this embodiment are metal strips of approximately 0.2 mm thickness, while the width of the strips at the area where they are passed through the wall 93 of the envelope, is approximately 1.2 mm. The distance between centres of two connection pins located beside each other, for example, the pins 81 and 82 is approximately 2.5 mm at the area where they pass through the wall 93 of the envelope. Initially the connection pins 81, 82 and 83 are integral with the connection strip 94 which is removed in a subsequent stage of the manufacture, after breaking or cutting along the broken line 95.

The two latter examples of semiconductor devices may further be manufactured from the conventional materials. The conductors may consist, for example, of gold wires, having a diameter of approximately 25μ . The connection pins may be gold-plated. The connection points 96 to 99 may be obtained, for example, by thermo-compression bonds or by ultrasonic welding.

The two latter configurations are also suitable for use in envelopes of resinous material, as a result of which relatively inexpensive transistors having a satisfactory screening are obtained.

The transistors 1; 50 and 80 may be incorporated in a circuit arrangement in accordance with the invention in a manner already shown diagrammatically in Figure 1. The input circuit and the output circuit are denoted only diagrammatically in this figure by the blocks 19 and 20. The one further connection pin 3 is common in the circuit to the input circuit 19 and the output circuit 20 while the input signals are applied to the other further connection pin 2 and the output signals are derived from the supporting connection pin 4.

A common base circuit arrangement is shown diagrammatically in Figure 11, in which the transistor 1; 50; 80 is shown symbolically in normal manner. The base B is common to the input circuit and the output circuit which are to be connected to the terminals P and Q and R and S, respectively. In Figures 1 to 10 this means that the one

further connection pins 3; 54; 82 is connected, through the conductors 9; 56; 85, to the base electrode of the semiconductor body 7; 52; 84 and the other further connection pin 2; 55; 83 is connected through the conductor 8; 57; 86 to the emitter electrode of the semiconductor body 7; 52; 84.

The capacitances C1 and C2 are the capacitances between the other further connection pin 2; 55; 83 and the one further connection pin 3; 54; 82 and that between the supporting connection pin 4; 53; 81 and the one further connection pin 3; 54; 82. These capacitances C1 and C2 which are connected across the electric input and across the electric output of the transistor 1; 50; 80 are usually not annoying in practice.

If sufficient precautions are not taken to obtain a good screening a capacitance C3 will occur between the collector C and the emitter E instead of at least a part of the capacitances C1 and C2. This capacitance C3 which in Figure 11 is denoted by broken lines, in the devices shown in Figures 1 to 10 is the capacitance between the other further connection pin 2; 55; 83 and the supporting connection pin 4; 53; 81, if these connection pins are not screened from one another or are insufficiently screened from one another. The capacitance C3 causes feedback coupling between the output circuit and the input circuit as a result of which, for example, the possible amplification of such a circuit is restricted.

In a circuit arrangement in accordance with the invention comprising a semiconductor device in accordance with the invention, the harmful capacitance C3 is reduced considerably in a simple manner or is even removed while the non-harmful capacitances C1 and C2 are increased.

In addition to a common base arrangement, for example, also a common emitter circuit is possible, see Figure 12. This circuit may be derived from the common base arrangement described by changing the base electrode and the emitter electrode of the semiconductor body 7; 52; 84.

It is to be noted that in circuit arrangements as shown in Figure 11 a reference potential, for example, earth or the chassis of the apparatus in which the circuit arrangement is incorporated is usually set up at the base, and in circuit arrangements as shown in Figure 12 at the emitter.

As already stated within the scope the invention devices other than bipolar transistors are included. For example, the semiconductor body 7 in Figures 1 and 2 may be that of a field-effect transistor in which the semiconductor body 7 is secured to the supporting connection pin 4 through the gate electrode which forms a *p-n* junction with

the channel region. The source electrode and the drain electrode are connected through the conductors 9 and 8, respectively to the one further connection pin 3 and the other connection pin 2. In a circuit arrangement such as is shown in Figure 13 the capacitance C4 by broken lines, is substantially entirely removed.

The semiconductor body 84 in Figures 8 to 10 may be, for example, that of an insulated gate field-effect transistor in which the source electrode is short-circuited to the substrate part of the semiconductor body, through which substrate part the semiconductor body 84 is secured to the supporting connection pin 81. The insulated gate electrode and the source electrode are connected, through the conductors 85 and 86 respectively to the one further connection pin 82 and the other further connection pin 83. The capacitance C5 in a circuit arrangement such as is shown in Figure 14 and comprising such insulated gate field-effect transistor is substantially entirely removed.

In the two last embodiments the input signals in a circuit arrangement are applied to the supporting connection pin 4; 81 while the output signals are derived from the other further connection pin 2; 83. In this case the one further connection pin 3; 82 is common for the input circuit and the output circuit.

Many variations are possible within the scope of the invention as defined in the appended claims. The connection pins need not form one assembly but may be constructed, for example, from a part which pass through the wall of the envelope to which a following part is connected inside the envelope, for example, by welding or soldering, if required at an angle with the first-mentioned part. The envelopes may have any desired shape. The envelope of resinous material need not be rectangular but may be disc-shaped or spherical. In order to obtain a better screening, the screening part 10; 59; 90 may have a larger area at right angles to the plane of the drawing of Figures 1, 3, 5, 8 and 10 than the connection pins 2, 4; 53, 55; 81, 83. This may be achieved, for example, in the devices shown in Figures 1 and 3 by twisting the strip 10, at least through part of its length, so that said part extends with its width at right angles to the plane of the drawing instead of parallel thereto. However, in many cases the strip 10, in the form as shown in Figures 1 and 3, will already provide a satisfactory screening. In the configuration shown in Figures 3 and 5 it may be desirable for example, not to pass the connection pins 2; 54 and 4; 55 accurately in opposite directions through the walls of the envelope, but, for example, in such manner that they are mutually inclined an angle of

approximately 120° to one another. Alternatively, for example, the part 10 in Figure 3 may be elongated and this elongation may pass through the wall 5 of the envelope as a fourth connection pin in a direction opposite to that of the connection pin 3. The one further connection pin 3 then has a double construction, as a result of which the electric input circuit and the electric output circuit in a circuit arrangement which comprises such a semiconductor device can be better separated from one another.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising an envelope within which is situated a semiconductor body having electrodes, at least three connection pins passing through the wall of the envelope, the semiconductor body being secured through one of its electrodes to an end portion of one of the connection pins, hereinafter termed the supporting connection pin, two further electrodes of the semiconductor body being connected through conductors to the two further connection pins, one of the two further connection pins comprising a first, electrically screening part which is located between the end portion of the supporting connection pin and a part of the other further connection pin, said one further connection pin also comprising a second part located adjacent the end portion of the supporting connection pin on the opposite side of the semiconductor body to the first, electrically screening part, the conductor which connects the one further connection pin to a further electrode of the semiconductor body being connected to said second part, the said first and second parts being united within the envelope.

2. A semiconductor device as claimed in Claim 1, wherein the connection points of the conductors to the further connection pins and to the further electrodes of the semiconductor body, viewed in a direction substantially at right angles to the largest cross-section of the semiconductor body, are located substantially on a straight line.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein the supporting connection pin, at least the first and second parts of the one further connection pin which are located on opposite sides of the semiconductor body adjacent the end portion of the supporting connection pin, and the other further connection pin lie substantially throughout their length inside the envelope in a common plane of intersection.

4. A semiconductor device as claimed in any of the preceding Claims, wherein the directions in which the supporting and the further connection pins pass through the wall of the envelope are parallel to the same plane.

5. A semiconductor device as claimed in

the channel region. The source electrode and the drain electrode are connected through the conductors 9 and 8, respectively to the one further connection pin 3 and the other connection pin 2. In a circuit arrangement such as is shown in Figure 13 the capacitance C4 by broken lines, is substantially entirely removed.

The semiconductor body 84 in Figures 8 to 10 may be, for example, that of an insulated gate field-effect transistor in which the source electrode is short-circuited to the substrate part of the semiconductor body, through which substrate part the semiconductor body 84 is secured to the supporting connection pin 81. The insulated gate electrode and the source electrode are connected, through the conductors 85 and 86 respectively to the one further connection pin 82 and the other further connection pin 83. The capacitance C5 in a circuit arrangement such as is shown in Figure 14 and comprising such insulated gate field-effect transistor is substantially entirely removed.

In the two last embodiments the input signals in a circuit arrangement are applied to the supporting connection pin 4; 81 while the output signals are derived from the other further connection pin 2; 83. In this case the one further connection pin 3; 82 is common for the input circuit and the output circuit.

Many variations are possible within the scope of the invention as defined in the appended claims. The connection pins need not form one assembly but may be constructed, for example, from a part which pass through the wall of the envelope to which a following part is connected inside the envelope, for example, by welding or soldering, if required at an angle with the first-mentioned part. The envelopes may have any desired shape. The envelope of resinous material need not be rectangular but may be disc-shaped or spherical. In order to obtain a better screening, the screening part 10; 59; 90 may have a larger area at right angles to the plane of the drawing of Figures 1, 3, 5, 8 and 10 than the connection pins 2, 4; 53, 55; 81, 83. This may be achieved, for example, in the devices shown in Figures 1 and 3 by twisting the strip 10, at least through part of its length, so that said part extends with its width at right angles to the plane of the drawing instead of parallel thereto. However, in many cases the strip 10, in the form as shown in Figures 1 and 3, will already provide a satisfactory screening. In the configuration shown in Figures 3 and 5 it may be desirable for example, not to pass the connection pins 2; 54 and 4; 55 accurately in opposite directions through the walls of the envelope, but, for example, in such manner that they are mutually inclined an angle of

approximately 120° to one another. Alternatively, for example, the part 10 in Figure 3 may be elongated and this elongation may pass through the wall 5 of the envelope as a fourth connection pin in a direction opposite to that of the connection pin 3. The one further connection pin 3 then has a double construction, as a result of which the electric input circuit and the electric output circuit in a circuit arrangement which comprises such a semiconductor device can be better separated from one another.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising an envelope within which is situated a semiconductor body having electrodes, at least three connection pins passing through the wall of the envelope, the semiconductor body being secured through one of its electrodes to an end portion of one of the connection pins, hereinafter termed the supporting connection pin, two further electrodes of the semiconductor body being connected through conductors to the two further connection pins, one of the two further connection pins comprising a first, electrically screening part which is located between the end portion of the supporting connection pin and a part of the other further connection pin, said one further connection pin also comprising a second part located adjacent the end portion of the supporting connection pin on the opposite side of the semiconductor body to the first, electrically screening part, the conductor which connects the one further connection pin to a further electrode of the semiconductor body being connected to said second part, the said first and second parts being united within the envelope.

2. A semiconductor device as claimed in Claim 1, wherein the connection points of the conductors to the further connection pins and to the further electrodes of the semiconductor body, viewed in a direction substantially at right angles to the largest cross-section of the semiconductor body, are located substantially on a straight line.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein the supporting connection pin, at least the first and second parts of the one further connection pin which are located on opposite sides of the semiconductor body adjacent the end portion of the supporting connection pin, and the other further connection pin lie substantially throughout their length inside the envelope in a common plane of intersection.

4. A semiconductor device as claimed in any of the preceding Claims, wherein the directions in which the supporting and the further connection pins pass through the wall of the envelope are parallel to the same plane.

5. A semiconductor device as claimed in



any of the preceding Claims, wherein the connection pins are in the form of wires which are flattened at least at the area where the semiconductor body and conductors are secured thereto, the major surfaces of the flattened parts of the connection pins being located substantially in one plane.

6. A semiconductor device as claimed in any of the Claims 1 to 4, wherein the connection pins consist of metal strips the major surfaces of which, at least in as far as the connection pins have a common plane of intersection, are substantially parallel to said plane of intersection.

7. A semiconductor device as claimed in any of the preceding Claims, wherein the semiconductor device is a transistor in which the semiconductor body is connected to the supporting connection pin through the collector, the base and the emitter electrodes of the semiconductor body being connected through the conductors to the further connection pins.

8. A semiconductor device as claimed in any of the Claims 1 to 7, wherein the connection pins pass through the wall of the envelope substantially in the same direction.

9. A transistor as claimed in Claim 7 or Claim 8 where appendant to Claim 7, wherein the semiconductor body is embedded in a resinous material, the connection pins projecting from said resinous material and the envelope of the transistor consisting exclusively of the said resinous material.

10. A transistor as claimed in Claim 9, wherein the connection pins inside the envelope of resinous material extend beside one another from a surface of the envelope of resinous material, the one further connection pin being located between the other further connection pin and the supporting connection pin, the supporting connection pin extending around the second part of the one further connection pin, the end portion of the supporting connection pin which supports the semiconductor body being located between the first and second parts of the one further connection pin.

11. A semiconductor device as claimed in Claim 8, wherein inside the envelope the one further connection pin is divided into two branches, one branch comprising the first, screening part and the other branch comprising the second part of the one further connection pin, the supporting connection pin extending around said other branch, the end portion of the supporting connection pin which supports the semiconductor body being located between the two branches of the one further connection pin, the part of the one further connection pin stemming from the branches being located, at least for part of its length, between a part of the supporting connection pin and a part of the

other further connection pin and passing through the wall of the envelope.

12. A semiconductor device as claimed in Claim 3 and Claim 8, wherein the first, screening part of the one further connection pin adjoins on one side a portion of said pin which passes through the wall of the envelope and adjoins on the opposite side a portion of said pin which lies entirely in the common plane of intersection and which extends around the end portion of the supporting connection pin, thus also constituting the second part of the one further connection pin.

13. A semiconductor device as claimed in any of Claims 1 to 7, wherein the direction in which the one further connection pin passes through the wall of the envelope is approximately at right angles, as hereinbefore defined, to the directions in which the supporting connection pin and the other further connection pin pass through the wall of the envelope.

14. A semiconductor device as claimed in Claim 13, wherein the one further connection pin is divided inside the envelope into two branches, one branch comprising the first, screening part and the other branch comprising the second part of the one further connection pin, the end portion of the supporting connection pin extending to a position between the two branches and the other further connection pin extending to a position adjacent the first, screening part of the one further connection pin.

15. A transistor as claimed in Claim 7, wherein the two further connection pins extend in substantially opposite directions from the wall of the envelope, the three connection pins lying substantially throughout their length inside the envelope in a common plane of intersection, a screening conductor being connected to the one further connection pin and extending around the end portion of the collector pin supporting the semiconductor body to a position between the collector pin and the other further connection pin, the free end of the screening conductor constituting the first, screening part of the one further connection pin.

16. A semiconductor device as claimed in any of the Claims 1 to 8 or in any of Claims 11 to 15, wherein the envelope consists of a resinous material, the semiconductor body with part of the connection pins being embedded in said resinous material.

17. A semiconductor device as claimed in any of Claims 1 to 8 or in any of Claims 11 to 15, wherein the wall of the envelope consists of electrically insulating material, the space in the envelope being filled with a gas.

18. A circuit arrangement comprising a semiconductor device as claimed in any of the preceding Claims, wherein the one



further connection pin is common to the input circuit and the output circuit, the input signals being applied to one of the two connection pins constituted by the other 5 further connection pin and the supporting connection pin, and the output signals being derived from the other of the said two connection pins.

19. A semiconductor device substantially 10 as herein described with reference to Figures 1 and 2, Figures 3 and 4, Figures 5 and 6, Figures 5 and 7, Figures 8 and 9, or Figure

10 of the accompanying drawings.

20. A circuit arrangement comprising a semiconductor device substantially as here- 15 in described with reference to Figure 1, Figure 11, Figure 12, Figure 13 or Figure 14 of the accompanying drawings.

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