resides in contact with the underlying layer 305 and resides over the substrate 303 and over the gate 301. The SnO_2 layer covers the gate both at the gate sidewalls and the top surface of the gate. The SnO_2 layer can be deposited by ALD or PECVD. Next, a layer of a second material 309 is deposited conformally over the substrate onto the SnO_2 layer 307 resulting in a structure shown in Figure 3D. In some embodiments the second material is SiO_2. The second material contacts the SnO_2 layer and resides over the substrate 303 and the gate 301, covering the gate both at its sidewalls and its top surface. In the next step, the structure is planarized (e.g., using chemical mechanical polishing). This step removes the layer of the second material (e.g., SiO_2) from the top surface of the gate, and exposes SnO_2 layer at the sidewalls of the gate. The structure shown in Figure 3E illustrates the substrate after planarization. It shows that the exposed SnO_2 layer 307 resides between exposed layer of the first material 305 and the exposed layer of the second material 309 at the sidewalls of the gate. This structure is one possible structure that can be used in operation 2201 of the process flow diagram shown in Figure 2. If the SnO_2 layer is deposited substantially conformally, the thickness of the SnO_2 layer deposited on the horizontal surfaces will be similar to the width of the SnO_2 layer exposed at the sidewalls of the gate. For example, if SnO_2 is deposited to a thickness of between about 20 – 100 Å, the exposed SnO_2 layer at the sidewall of the gate would have the width of between about 20 – 100 Å.

Next, hydrogen plasma etching is performed, as described herein. The substrate shown in Figure 3E is contacted with a plasma formed in a process gas comprising H_2 in an etch process chamber, and the exposed SnO_2 layer 307 is selectively etched (relative to other exposed materials) to form a recessed feature between the layer of the second material 309 and the layer of the first material 305. The resulting structure is shown in Figure 3F, which illustrates the recessed feature 311 between layers 309 and 305. Finally, in the subsequent step a layer of a third material (e.g., SiO_2) 313 is deposited, e.g., by HDP CVD such that it covers the recessed feature 311 without fully filling it, thereby creating an air gap.

A more specific example of a method for forming an air gap includes: (a) forming a gate on a substrate, where the gate includes high-k oxide; (b) conformally depositing a SiN layer by ALD in contact with the gate (both on the sidewalls of the gate and on the top surface of the gate); (c) conformally forming a layer of SnO_2 over

the layer of the SiN layer, e.g., by ALD or PECVD; (d) conformally forming a SiO_2 layer over the layer of SnO_2; (e) planarizing the structure (e.g., by chemical mechanical polishing), wherein planarization removes the SiO_2 from the horizontal surfaces and exposes SnO_2 and the first material at the sidewalls of the gate thereby providing a substrate having an exposed SiN layer, an exposed SiO_2 layer, and an exposed layer of SnO_2 positioned between these layers; (f) etching the exposed SnO_2 using hydrogen plasma as described herein with high etch selectivity relative to SiN and SiO_2, and thereby forming a recessed feature between SiN and SiO_2 layers; and (g) depositing a SiO_2 over the recessed feature without fully filling the recessed feature, and thereby forming the air gap between the layers of the first and second materials. The width of the SnO_2 layer that is deposited and is removed by the hydrogen plasma etch in some embodiments, is between about 20 – 100 Å.

A detailed processing scheme for forming air gaps in FinFET device fabrication is described in the commonly owned US Patent No. 9,515,156, by Besser et al., titled "Air Gap Spacer Integration For Improved Fin Device Performance" issued December 6, 2016, which is herein incorporated by reference in its entirety for the purpose of describing an air gap formation method that can be used in conjunction with the SnO_2 spacers provided herein. Methods for forming air gaps in the context of FinFET device fabrication according to some embodiments are described herein with reference to Figures 4A-4T, which show perspective views of a semiconductor substrate during various stages of FinFET device fabrication.

In some embodiments FinFET devices with air gap spacers and methods for integrating air gaps using sacrificial SnO_2 spacers into FinFET devices are provided. Air gap spacers are formed using a sacrificial SnO_2 spacer during integration. The sacrificial spacer is subsequently removed after self-aligned source/drain contact formation. The air gap spacer reduces FinFET parasitic capacitance. Low parasitic capacitance can be achieved without loss of process window or relaxing of lithography overlay requirements.

Referring now to FIGS. 4A-4B, the substrate is shown after shallow trench isolation (STI) recess etch and dummy gate formation, respectively. In FIG. 4A, the substrate 100 includes an inter-layer dielectrc (ILD) layer 110 and a plurality of fins 114. The ILD layer 110 may be made of low k dielectrics, doped oxides, flowable

417. In various embodiments, a bias power of the electrostatic chuck may be set at about 50Vb or may be set at a different bias power depending on the process performed in accordance with disclosed embodiments. For example, the bias power may be between about 20 Vb and about 100 Vb, or between about 30 Vb and about 150 Vb.

Elements for plasma generation include a coil 433 is positioned above window 411. In some embodiments, a coil is not used in disclosed embodiments. The coil 433 is fabricated from an electrically conductive material and includes at least one complete turn. The example of a coil 433 shown in Figure 5 includes three turns. The cross-sections of coil 433 are shown with symbols, and coils having an "X" extend rotationally into the page, while coils having a "●" extend rotationally out of the page. Elements for plasma generation also include an RF power supply 441 configured to supply RF power to the coil 433. In general, the RF power supply 441 is connected to matching circuitry 439 through a connection 445. The matching circuitry 439 is connected to the coil 433 through a connection 443. In this manner, the RF power supply 441 is connected to the coil 433. An optional Faraday shield 449a is positioned between the coil 433 and the window 411. The Faraday shield 449a may be maintained in a spaced apart relationship relative to the coil 433. In some embodiments, the Faraday shield 449a is disposed immediately above the window 411. In some embodiments, the Faraday shield 449b is between the window 411 and the chuck 417. In some embodiments, the Faraday shield 449b is not maintained in a spaced apart relationship relative to the coil 433. For example, the Faraday shield 449b may be directly below the window 411 without a gap. The coil 433, the Faraday shield 449a, and the window 411 are each configured to be substantially parallel to one another. The Faraday shield 449a may prevent metal or other species from depositing on the window 411 of the process chamber 424.

Process gas (e.g. H_2 and He, etc.) may be flowed into the process chamber through one or more main gas flow inlets 460 positioned in the upper sub-chamber 402 and/or through one or more side gas flow inlets 470. Likewise, though not explicitly shown, similar gas flow inlets may be used to supply process gases to a capacitively coupled plasma processing chamber. A vacuum pump, e.g., a one or two stage mechanical dry pump and/or turbomolecular pump 440, may be used to draw process gases out of the process chamber 424 and to maintain a pressure within the

9. The method of claim 1, wherein the process gas further comprises Cl_2.

10. The method of claim 1, wherein (b) comprises forming a plasma without using an external bias for the substrate.

11. The method of claim 1, wherein (b) comprises generating a plasma using a power density of between about 0.0018 and 0.36 W/cm^2.

12. The method of claim 1, wherein the etching of SnO_2 is conducted at a pressure of between about 1 and 175 mTorr.

13. The method of claim 1, wherein the process gas comprises H_2 and He.

14. The method of claim 1, wherein the process gas comprises H_2, He and a hydrocarbon.

15. The method of claim 1, further comprising, prior to (a), depositing the SnO_2 layer on the semiconductor substrate by atomic layer deposition.

16. The method of claim 1, wherein (b) comprises selectively etching SnO_2 in a presence of SiO_2, wherein the etch selectivity is at least 10.

17. The method of claim 1, further comprising:

applying photoresist to the semiconductor substrate;

exposing the photoresist to light;

patterning the photoresist and transferring the pattern to the substrate;

and selectively removing the photoresist from the substrate.

18. An apparatus for etching an SnO_2 layer, the apparatus comprising:

(a) a process chamber having a substrate holder configured for holding a semiconductor substrate during etching;

31. A system for forming an air gap on a semiconductor substrate, the system comprising:

(a) one or more deposition process chambers;

(b) one or more etch process chambers; and

(c) a controller comprising program instructions for causing the steps of:

(i) on a semiconductor substrate having an exposed layer of a first material, an exposed layer of a second material, and an exposed layer of SnO_2 positioned between the layer of the first material and the layer of the second material, selectively etching the exposed SnO_2 relative to both the first and the second materials using a hydrogen plasma etch chemistry, and thereby forming a recessed feature between the first and second materials; and

(ii) depositing a third material over the recessed feature without fully filling the recessed feature, and thereby forming the air gap between the layer of the first material and the layer of the second material.

32. The system of claim 31, further comprising a stepper.

33. A method for processing a semiconductor substrate, the method comprising:

(a) forming an SnO_2 dummy gate on the semiconductor substrate;

(b) processing the semiconductor substrate in a presence of the SnO_2 dummy gate;

(c) etching the SnO_2 dummy gate with a plasma formed in a process gas comprising H_2 to form a recessed feature in place of the dummy gate;

(d) depositing a high-k dielectric material into the formed recessed feature to thereby form a gate in place of the dummy gate.