

Description

This invention relates to a method of chamfering a semiconductor wafer, and more particularly to a method of chamfering a semiconductor method, wherein a rotating grindstone is abutted against the peripheral edge of the rotating semiconductor wafer for grinding the peripheral edge of the semiconductor wafer.

DE-A-30 26 272 discloses a method according to the preamble of claims 1 and 3.

In the semiconductor wafer cut by slicing, the surface thereof is subjected to lapping and the peripheral edge thereof is chamfered to prevent from cracking and from being adhered thereto with dust and to prevent the dust from being produced. That is, as shown in Fig. 9, an inclined surface 14 of a rotating grindstone 12 with a groove is urged against a rotating semiconductor wafer 10 to chamfer the peripheral edges 16 and 17 of the semiconductor wafer.

However, according to the conventional method of chamfering the semiconductor wafer, as shown in Fig. 9, the moving direction A of an abrasive grain 15 is limited to the circumferential direction of the wafer, whereby a streak A' is formed on a chamfered surface by the abrasive grain (partial cutting edge), so that the surface roughness accuracy of the chamfered surface is not satisfactory. When the surface roughness accuracy of the chamfered surface is unsatisfactory, the dust adheres to the peripheral edge surface where chips due to partial cracks on the peripheral edge surface of the wafer are formed. Further, there is a factor of producing the dust due to crouching of fine particles between the cracks, so that an adverse influence is rendered to the post-treatment process of the wafer. In order to obviate this drawback, the count number of the grindstone is raised, the cut-in amount is decreased, the number of times of dressing is increased and several grindstones are exchanged (at two stages, three stages and so forth) to raise the surface roughness accuracy of the ground surface, however, these counter measures present a disadvantage of lowering the grinding efficiency.

The present invention has been developed to obviate the above-described disadvantages and has its object the proposal of a method of chamfering a semiconductor wafer, wherein the surface roughness accuracy of the chamfered surface is improved and the grinding efficiency is not lowered.

According to one aspect of the present invention there is provided a method of chamfering a semiconductor wafer as set out in claim 1.

According to the first aspect of the present invention, the rotary axis of the grindstone is inclined to the direction of the tangent line of the semiconductor wafer with the respect to the rotary axis of the semiconductor wafer for grinding the peripheral edge of the semiconductor wafer, whereby the movement of the grindstone is applied to the radial direction of the wafer in the inclined surface, and simultaneously, the movement of the grindstone is applied to the rotating direction of the wafer in

the outer peripheral surface, so that the ground surface of the peripheral edge of the semiconductor wafer becomes smooth and deformation of the grinding surface of the grindstone itself is reduced, to thereby extend the service life of the grindstone.

According to another aspect of the present invention there is provided a method of chamfering the semiconductor wafer as set out in claim 3.

According to the second aspect of the present invention, the peripheral edge of the semiconductor wafer is ground while the grindstone is reciprocatingly moved along the inclined surface of the grindstone, whereby the moving direction of the abrasive grains is inclined to the circumferential direction of the wafer and the grinding is performed while the grindstone is reciprocatingly moved along the rotary axis of the wafer, so that the ground surface at the peripheral edge of the semiconductor wafer becomes smooth and the deformation of the grinding surface of the grindstone itself is reduced, to thereby extend the service life of the grindstone.

Preferred embodiments are subjects of the claims 2 and 4.

The exact nature of this invention, as well as other object and advantages thereof, will be readily apparent from consideration of the following specification relating the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof and wherein:

Fig. 1 is a front view showing the method of chamfering according to the present invention,

Fig. 2 is a view in the direction indicated by the arrows from the line 2-2 in Fig. 1,

Fig. 3 is an explanatory view showing the moving direction of the abrasive grains according to the present invention,

Fig. 4 is a block diagram showing the chamfering device for performing the method of chamfering the wafer according to the present invention,

Fig. 5 is an explanatory view showing the method of chamfering the wafer according to the present invention,

Fig. 6 is an explanatory view showing the moving direction of the abrasive grains in the method of chamfering the wafer according to the present invention,

Fig. 7 is an explanatory view showing the movement of the abrasive grains in the method of chamfering the wafer according to the present invention,

Fig. 8 is an explanatory view showing the conventional method of chamfering the semiconductor wafer,

Fig. 9 is an explanatory view showing the moving direction of the abrasive grains in the conventional method of chamfering the semiconductor wafer, and Fig. 10 is an explanatory view showing the moving direction of the abrasive grains in the conventional method of chamfering the semiconductor wafer.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Detailed description will hereunder be given of the preferred embodiment of a method of chamfering a semiconductor wafer according to the present invention with reference to the accompanying drawings.

A wafer 20 shown in Fig. 1 is held by the well-known clamping mechanism or sucking mechanism, not shown, and rotatable about an axis P - P at 1 ~ 2 r.p.m. for example. On the other hand, a grindstone 22 is formed of a grindstone with a groove, and an inclined surface 22A forming the side surface of the groove of the grindstone 22 and a peripheral surface forming the bottom surface of the groove of the grindstone 22 constitute a grinding surface. This grindstone 22 is rotatable about an axis O - O at 2500 r.p.m. for example, in the same direction as the wafer 20 or in the reverse direction thereof.

As shown in Fig. 2, the rotary axis O - O of the grindstone 22 is inclined through an angle θ to the rotary axis P - P of the wafer 20. That is, the grindstone 22 is inclined through the angle θ to the direction of the tangent line of the wafer 20, and, in this state, the grindstone 22 chamfers an edge portion 20A at the peripheral edge of the wafer 20. When chamfering is performed in this state, a moving direction A of the abrasive grain 23A of the grindstone 22 takes a direction perpendicular to the rotary axis O - O of the grindstone 22 as shown in Fig. 3, whereby the moving direction A is inclined to the chamfered surface 20A of the wafer 20. Accordingly, the moving direction A of the abrasive grains 23A is divided into two including a component force A_1 in the grinding direction and a component force A_2 in the perpendicular direction, and these component forces act on the grinding of a chamfered surface 20A of the semiconductor wafer. According to the present invention, in a special work of the chamfering of the semiconductor wafer, the inclined angle θ and an angle α of the grindstone are determined and the chamfering at a predetermined angle is performed. That is, by inclining the grindstone to the chamfering of the wafer, whereby the same movement as that in the ordinary method of inclined grinding can be offered. When the grinding is performed in this state, the number of acting abrasive grains is increased, so that the surface accuracy of the ground surface can be improved owing to the averaging effect of the acting abrasive grains.

The shaft of the grindstone is inclined in the above embodiment, however, the shaft of the wafer may be inclined.

Furthermore, an outer peripheral surface 20B of the wafer 20 is ground by the bottom surface of the groove 22B of the grindstone 22 which is inclined through the angle θ , and, in this case too, the number of the acting abrasive grains is increased, so that the satisfactory ground surface can be obtained.

As described above, according to the method of chamfering the semiconductor wafer of the present invention, the grinding is performed with the axis of the grindstone being inclined to the rotary axis of the semi-

conductor wafer, so that the ground surface having the satisfactory accuracy can be obtained and the service life of the grindstone can be extended.

The wafer 20 shown in Fig. 4 is held by the well-known clamping mechanism or sucking mechanism, and rotatable at 1 ~ 2 r.p.m. for example. On the other hand, a grindstone 24 is formed of a grindstone with a groove, and an inclined surface 25 forming the side surface of the groove of the grindstone 24 constitutes a grinding surface. This grindstone 24 is rotatable by a motor 26 at 2500 r.p.m. for example, in the same direction as the wafer 20, or in the reverse direction thereof.

Further, the grindstone 24 is reciprocatingly moved along an inclined surface 25 as indicated by arrow marks shown in Fig. 5. The above-described reciprocating movement in the direction of inclination can be achieved by combining the well-known vertically moving mechanism with the well-known horizontally moving mechanism. That is, the grindstone 24 is supported by a support plate 28 whose nut portion 30 is threadably coupled to a screw shaft 32. Accordingly, when the screw shaft 32 is rotated by the driving of a motor 34, the support plate 28 is vertically moved and the grindstone 24 is vertically moved as well. Furthermore, the motor 34 is supported by a movable table 36 whose nut portion 38 is threadably coupled to a screw shaft 40. Accordingly, when the screw shaft 40 is rotated by the driving of a motor 42, the table 36 is moved in the horizontal direction and the grindstone 24 is horizontally moved as well. Designated at 44 is a main controller and 46 an oblique movement control section. The main controller 44 controls the driving of the motor 26 and controls the oblique movement control section 46 as well. The motors 34 and 42 are controlled by the oblique movement control section 46 to reciprocatingly move the grindstone in the oblique direction. When the grindstone 22 is ground during the reciprocating movement thereof along the inclined surface 25, the moving direction of the abrasive grains becomes one shown in Fig. 7 during the obliquely upward movement of the grindstone 24, and the moving direction of the abrasive grains becomes one shown in Fig. 8 during the oblique downward movement of the grindstone 24.

With these operations, the moving direction of the abrasive grains is inclined to the circumferential direction of the wafer and the number of the acting abrasive grains of the grindstone is increased, so that the surface accuracy of the ground surface can be improved owing to the averaging effect of the acting abrasive grains.

Furthermore, as shown in Fig. 6, the grindstone 24 is reciprocatingly moved as indicated by arrow marks in Fig. 6 along a surface 25a contacting the outer periphery of the wafer (the peripheral surface of the grindstone is parallel to the rotary axis of the wafer). An embodiment of this reciprocating movement may be shown by the above-described example of the mechanism.

The grindstone is reciprocatingly moved in the above embodiment, however, the wafer may be reciprocatingly moved.

As has been described hereinabove, according to the method of chamfering the semiconductor wafer of the present invention, the grinding is performed with the grindstone being reciprocatingly moved along the inclined surface of the grindstone, so that the ground surface having the satisfactory accuracy can be obtained and the service life of the grindstone can be extended.

Claims

1. A method of chamfering a semiconductor wafer, wherein a rotating grindstone (22) is abutted against a peripheral edge (20A, 20B) of the rotating semiconductor wafer for grinding the peripheral edge (20A, 20B) of the semiconductor wafer (20), characterized in that the grindstone (22) has a cylindrical surface, the rotary axis of the grindstone is inclined in a plane which is parallel to the rotation axis of the wafer (20) and the peripheral edge (20A, 20B) of the semiconductor wafer (20) is ground with a rotary axis of the grindstone (22) being inclined to a direction of a tangent line of an outer periphery of the semiconductor wafer (20).
2. The method of chamfering the semiconductor wafer as set forth in claim 1, wherein said grindstone (22) has an axial groove (22B), the side portions thereof are an inclined surface (22A) forming the grinding surfaces of said grindstone (22) and the bottom surface of the axial groove (22B) is formed by the outer peripheral surface.
3. A method of chamfering a semiconductor wafer, wherein a rotating grindstone (24) is abutted against the peripheral edge of a rotating semiconductor wafer (20) for grinding the peripheral edge of the semiconductor wafer (20), characterized in that the edge portion at the peripheral edge of the semiconductor wafer (20) is ground while said grindstone (24) is reciprocatingly moved along an inclined surface (25) of said grindstone (24) in a state where a rotary axis of the semiconductor wafer (20) and the rotary axis of said grindstone (24) are kept in parallel to each other.
4. The method of chamfering the semiconductor wafer as set forth in claim 3, characterized in that the outer peripheral surface at the peripheral edge of the semiconductor wafer (20) is ground by the peripheral surface of the grindstone (24) disposed in parallel to the rotary axis while the grindstone (24) is reciprocatingly moved along the direction of the axis.

Patentansprüche

1. Verfahren zum Anfasen eines Halbleiterwafers, bei dem ein sich drehender Schleifstein (22) in Anlage gegen einen Umfangsrand (20A, 20B) des sich drehenden Halbleiterwafers zum Schleifen des

Umfangsrandes (20A, 20B) des Halbleiterwafers (20) gebracht wird, dadurch gekennzeichnet, daß der Schleifstein (22) eine zylindrische Fläche hat, die Drehachse des Schleifsteins in einer Ebene geneigt ist, welche parallel zu der Drehachse des Wafers (20) ist, und der Umfangsrand (20A, 20B) des Halbleiterwafers (20) derart geschliffen wird, daß eine Drehachse des Schleifsteins (22) in Richtung einer Tangentiallinie an einem Außenumfang des Halbleiterwafers (20) geneigt ist.

2. Verfahren zum Anfasen des Halbleiterwafers nach Anspruch 1, bei dem der Schleifstein (22) eine axiale Ausnehmung (22B) hat, dessen Seitenabschnitte eine geneigte Fläche (22A) bilden, welche die Schleifflächen des Schleifsteins (22) bildet, und die Bodenfläche der axialen Ausnehmung (22B) von der äußeren Umfangsfläche gebildet wird.
3. Verfahren zum Anfasen eines Halbleiterwafers, bei dem ein sich drehender Schleifstein (24) zur Anlage gegen den Umfangsrand eines sich drehenden Halbleiterwafers (20) zum Schleifen des Umfangsrandes des Halbleiterwafers (20) gebracht wird, dadurch gekennzeichnet, daß der Randabschnitt des Umfangsrandes des Halbleiterwafers (20) geschliffen wird, während dem der Schleifstein (27) entlang einer geneigten Fläche (25) des Schleifsteins (24) in einem Zustand hin- und hergehend bewegt wird, in welchem eine Drehachse des Halbleiterwafers (20) und die Drehachse des Schleifsteins (24) parallel zueinander angeordnet sind.
4. Verfahren zum Anfasen des Halbleiterwafers nach Anspruch 3, dadurch gekennzeichnet, daß die Außenumfangsfläche des Umfangsrandes des Halbleiterwafers (20) dadurch geschliffen wird, daß die Umfangsfläche des Schleifsteins (24) parallel zu der Drehachse angeordnet ist, während dem der Schleifstein (24) entlang der Achsrichtung hin- und hergehend bewegt wird.

Revendications

1. Procédé de chanfreinage d'une tranche de semi-conducteur, dans lequel une meule (22) rotative est appliquée contre un bord périphérique (20A, 20B) de la tranche de semi-conducteur en rotation, pour meuler le bord périphérique (20A, 20B) de la tranche de semi-conducteur (20), caractérisé en ce que la meule (22) a une surface cylindrique, l'axe de rotation de la meule est incliné dans un plan qui est parallèle à l'axe de rotation de la tranche (1) et le bord périphérique (20A, 20B) de la tranche de semi-conducteur (20) est meulé avec un axe de rotation de la meule (22) incliné par rapport à une direction d'une ligne tangente à la partie périphérique extérieure de la tranche de semi-conducteur (20).

As has been described hereinabove, according to the method of chamfering the semiconductor wafer of the present invention, the grinding is performed with the grindstone being reciprocatingly moved along the inclined surface of the grindstone, so that the ground surface having the satisfactory accuracy can be obtained and the service life of the grindstone can be extended.

Claims

1. A method of chamfering a semiconductor wafer, wherein a rotating grindstone (22) is abutted against a peripheral edge (20A, 20B) of the rotating semiconductor wafer for grinding the peripheral edge (20A, 20B) of the semiconductor wafer (20), characterized in that the grindstone (22) has a cylindrical surface, the rotary axis of the grindstone is inclined in a plane which is parallel to the rotation axis of the wafer (20) and the peripheral edge (20A, 20B) of the semiconductor wafer (20) is ground with a rotary axis of the grindstone (22) being inclined to a direction of a tangent line of an outer periphery of the semiconductor wafer (20).
2. The method of chamfering the semiconductor wafer as set forth in claim 1, wherein said grindstone (22) has an axial groove (22B), the side portions thereof are an inclined surface (22A) forming the grinding surfaces of said grindstone (22) and the bottom surface of the axial groove (22B) is formed by the outer peripheral surface.
3. A method of chamfering a semiconductor wafer, wherein a rotating grindstone (24) is abutted against the peripheral edge of a rotating semiconductor wafer (20) for grinding the peripheral edge of the semiconductor wafer (20), characterized in that the edge portion at the peripheral edge of the semiconductor wafer (20) is ground while said grindstone (24) is reciprocatingly moved along an inclined surface (25) of said grindstone (24) in a state where a rotary axis of the semiconductor wafer (20) and the rotary axis of said grindstone (24) are kept in parallel to each other.
4. The method of chamfering the semiconductor wafer as set forth in claim 3, characterized in that the outer peripheral surface at the peripheral edge of the semiconductor wafer (20) is ground by the peripheral surface of the grindstone (24) disposed in parallel to the rotary axis while the grindstone (24) is reciprocatingly moved along the direction of the axis.

Patentansprüche

1. Verfahren zum Anfasen eines Halbleiterwafers, bei dem ein sich drehender Schleifstein (22) in Anlage gegen einen Umfangsrand (20A, 20B) des sich drehenden Halbleiterwafers zum Schleifen des

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2. Verfahren zum Anfasen des Halbleiterwafers nach Anspruch 1, bei dem der Schleifstein (22) eine axiale Ausnehmung (22B) hat, dessen Seitenabschnitte eine geneigte Fläche (22A) bilden, welche die Schleifflächen des Schleifsteins (22) bildet, und die Bodenfläche der axialen Ausnehmung (22B) von der äußeren Umfangsfläche gebildet wird.
3. Verfahren zum Anfasen eines Halbleiterwafers, bei dem ein sich drehender Schleifstein (24) zur Anlage gegen den Umfangsrand eines sich drehenden Halbleiterwafers (20) zum Schleifen des Umfangsrandes des Halbleiterwafers (20) gebracht wird, dadurch gekennzeichnet, daß der Randabschnitt des Umfangsrandes des Halbleiterwafers (20) geschliffen wird, während dem der Schleifstein (27) entlang einer geneigten Fläche (25) des Schleifsteins (24) in einem Zustand hin- und hergehend bewegt wird, in welchem eine Drehachse des Halbleiterwafers (20) und die Drehachse des Schleifsteins (24) parallel zueinander angeordnet sind.
4. Verfahren zum Anfasen des Halbleiterwafers nach Anspruch 3, dadurch gekennzeichnet, daß die Außenumfangsfläche des Umfangsrandes des Halbleiterwafers (20) dadurch geschliffen wird, daß die Umfangsfläche des Schleifsteins (24) parallel zu der Drehachse angeordnet ist, während dem der Schleifstein (24) entlang der Achsrichtung hin- und hergehend bewegt wird.

Revendications

1. Procédé de chanfreinage d'une tranche de semi-conducteur, dans lequel une meule (22) rotative est appliquée contre un bord périphérique (20A, 20B) de la tranche de semi-conducteur en rotation, pour meuler le bord périphérique (20A, 20B) de la tranche de semi-conducteur (20), caractérisé en ce que la meule (22) a une surface cylindrique, l'axe de rotation de la meule est incliné dans un plan qui est parallèle à l'axe de rotation de la tranche (1) et le bord périphérique (20A, 20B) de la tranche de semi-conducteur (20) est meulé avec un axe de rotation de la meule (22) incliné par rapport à une direction d'une ligne tangente à la partie périphérique extérieure de la tranche de semi-conducteur (20).





2. Procédé de chanfreinage d'une tranche de semi-conducteur selon la revendication 1, dans lequel ladite meule (22) possède une gorge axiale (22B) dont les parties latérales sont constituées par une surface inclinée (22A) formant les surfaces de meulage de ladite meule (22) et la surface de fond de la gorge axiale (22B) est formée par la surface périphérique extérieure. 5
3. Procédé de chanfreinage d'une tranche de semi-conducteur dans lequel une meule (24) rotative est appliquée contre le bord périphérique d'une tranche de semi-conducteur (20) en rotation pour meuler le bord périphérique de la tranche de semi-conducteur (20), caractérisé en ce que la partie de bord située sur le bord périphérique de la tranche de semi-conducteur (20) est meulée en même temps que ladite meule (24) est entraînée en mouvement alternatif le long d'une surface inclinée (25) de ladite meule (24) dans un état où un axe de rotation de la tranche de semi-conducteur (20) et l'axe de rotation de ladite meule (24) sont maintenus parallèles entre eux. 10 15 20
4. Procédé de chanfreinage d'une tranche de semi-conducteur selon la revendication 3, caractérisé en ce que la surface périphérique extérieure située sur le bord périphérique de la tranche de semi-conducteur (20) est meulée par la surface périphérique de la meule (24) disposée parallèlement à l'axe de rotation pendant que la meule (24) est déplacée en mouvement alternatif le long de la direction de l'axe. 25 30

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