

Description

Background of the invention:

This invention relates to an analog-to-digital conversion apparatus according to the preamble of claim 1.

PROCEEDINGS OF THE 1987 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, May 1987, pages 467-472 comprises an analysis for oversampling A-to-D converter structures. The results suggest that a first order predictive encoder, with first order noise shaping, is best suited to high resolution future VLSI implementation. A second order delta modulation coder of the kind according to the preamble of claim 1 of the present application is not considered to be applicable to a precision converter, but to a high speed converter instead.

EP-A-60583 discloses a system for the quantization of signals comprising besides a first quantizer, a second quantizer for providing a second quantized output signal which is used in order to reduce part of the quantization noise. The second quantizer can have more quantizing levels than the first quantizer and these levels can be coded in a binary manner.

This invention provides in particular apparatus for high-resolution analog-to-digital conversion of electrical signals. While applicable to seismic and other dynamic waveform signals, the invention relates also to analog-to-digital encoders used in other applications, and to techniques of high-resolution analog-to-digital conversion in general.

Digital encoding of seismic, sonar, audio vibrations and other types of broad-band physical signals requires a large dynamic range, greater than 120 dB, extremely low differential non-linearity (often less than a fraction of a part-per-million), and well-defined phase and group delay. Seismic waveforms, for example, comprise a large dynamic range, greater than 140 dB, and frequency content, more than 5 decades. These signals typically do not, however, require commensurate absolute accuracy of the zero-frequency full scale.

Progress has been made in prior-art analog-to-digital encoding devices employing delta sigma modification to achieve high linearity. Improvements over early devices have produced higher loop gain within the desired signal passband by incorporating integrators or low-pass filters within the delta-modulator feedback loop, thus creating a delta-sigma modulator. For a given bit rate, the additional loop gain increases the information content in the delta-modulated serial bit-stream output at frequencies within the signal passband. Double, triple, and higher order implementations of the delta-sigma modulator are used. The following U.S.

Patents disclose examples of such systems:

3,825,831 Ishiguro
4,313,204 DeFreitas
4,509,037 Harris
4,518,948 VanRoessel
4,542,354 Robinton et al.
4,573,037 Robinton et al.
4,588,981 Senn

The Ishiguro patent discloses differential pulse code modulation apparatus including a delta modulator for converting an analog input signal to a delta modulated signal, a digital filter for removing quantization noise components, and a direct feedback pulse code modulation encoder.

The DeFreitas patent discloses apparatus for generating a digitally encoded signal from an analog signal and a reference signal, including a circuit for reducing quantization noise.

The Harris patent discloses an analog-to-digital encoder including a delta modulation encoder. An analog signal and an internal analog signal generated by an internal decoder are summed to provide an internal analog error signal. The encoder also includes a spectrum filter having at least three integrator circuits and a clipping circuit connected in parallel to two of the three integrator circuits.

The VanRoessel patent discloses an analog-to-digital converter including a series arrangement of an integrating circuit, a comparison circuit, a flip-flop and a gate.

The Robinton ('354) patent discloses a delta-sigma pulse modulator for converting an input signal to an output pulse train having an average amplitude proportional to the input signal. The modulator includes an integrator/comparator circuit.

The Robinton ('037) patent discloses an analog-to-digital converter including an integrator, a comparator, and digital gates for receiving and processing an analog input signal.

The Senn patent discloses a double integration, delta-sigma analog-to-digital converter including first and second adders, first and second integrators, a quantizer circuit, operational amplifiers and switched capacitor circuits.

The above patents accordingly describe apparatus for converting analog input signals to digital output signals. However, prior-art analog-to-digital converters (ADCs) comprising a delta-sigma modulator have a variety of operational deficiencies such as noise and limited dynamic range.

A double-integrator delta-sigma modulator, although an improvement relative to a single-integrator version or a simple delta modulator, requires a loop bit rate on the order of 1000 times the highest signal frequency to achieve 120-140 dB dynamic range. In a converter employing delta-sigma modulation, the loop bit rate should ideally be as low as possible relative to the highest processed signal

frequency for several reasons.

In particular, semiconductor analog switches such as Field Effect Transistors (FETs) that are used within the delta-sigma modulator loop introduce errors, essentially noise, because of charge injection each time the switch is operated. The error due to charge injection is proportional to the switching frequency. The number of switchings per unit time, and therefore the loop bit rate, relative to the highest signal frequency should therefore be minimized. Charge injection errors are a principal limitation in delta- and delta-sigma modulators having high dynamic range.

Moreover, a lower loop bit rate demands less numerical computation per unit time in digital filters or other processors receiving the output of the delta-sigma modulator. The time duration of the impulse response of a digital filter associated with a delta-sigma modulator is proportional to a function of the ratio of loop bit rate to highest signal frequency. The time duration of a subsequent digital filter is also proportional to the required degree of suppression by the filter of undesired signals. In particular, the single-bit output of a delta modulator class of device has a large granularity, essentially quantization noise, at the loop bit rate frequency. A digital filter may be used to reduce this noise within the desired signal passband, although to achieve 120-140 dB of dynamic range requires a substantial 120-140 dB of suppression, and an accordingly long filter duration. Excessive group delay accompanying a filter with long duration may, for example, preclude application of the ADC within a closed-loop servo control system, or other real-time application.

A triple, or higher order, delta-sigma modulator has a relatively high information content in the output serial bit stream for a given loop bit rate, but requires some means to suppress meta-stable or unstable oscillation of the delta-sigma feedback loop. Such a high-order loop, in general, violates the Nyquist criterion for stability, and has required, in prior-art devices, a non-linear device that reduces the feedback loop gain momentarily when oscillations increase. This introduces noise within the signal passband, since the delta-sigma loop order is effectively reduced to order 1 or 2, although the loop bit rate remains constant. Furthermore, such a meta-stable loop must be operated with maximum signal levels significantly below the nominal full scale range of the loop so that non-linear loop stabilization is not required frequently. Such operation, however, sacrifices dynamic range for a given implementation.

Additionally, these characteristics of delta-sigma modulation indicate that for a given loop bit rate, the technique requiring the lowest ratio of loop bit rate to maximum signal frequency provides the

highest conversion rate. Because actual circuit performance and thus potential fields of application are limited by analog switch charge injection, digital computation rate and digital filter duration, maximum conversion rate and resolution, which is required in applications such as sonar and ultrasound imaging, digital studio audio, vibration analysis, and precision instrumentation, can be achieved only by the technique requiring the lowest relative loop bit rate.

There accordingly exists a need for high-resolution analog-to-digital conversion apparatus characterized by large amplitude and frequency range and low differential non-linearity.

It is thus an object of the invention to provide improved analog-to-digital converter (ADC) apparatus for converting analog input signals to digital output signals.

It is another object of the invention to provide ADC apparatus which is capable of processing signals having a large dynamic range and frequency content.

It is a further object of the invention to provide ADC apparatus having extremely low differential non-linearity, precisely-defined phase delay and minimal group delay.

It is yet another object of the invention to provide ADC apparatus which is suitable for use in processing seismic, audio and other analog signals.

Other general and specific objects of the invention will in part be obvious and will in part appear hereinafter.

Summary of the Invention

The invention provides analog-to-digital conversion apparatus for receiving an analog input signal and producing a digital output signal, as defined by claim 1. The invention includes an input summing element for receiving an analog input signal and an analog offset signal, and for producing a residual signal in response to an arithmetic combination of the analog input signal and the analog offset signal. The invention also provides a first integrating element, in electrical circuit with the input summing element, for receiving and integrating the produced residual signal to produce a first integrator output signal.

The invention further provides a second integrating element, in electrical circuit with the first integrating element, for receiving and integrating the first integrator output signal to produce a second integrator output signal. An analog-to-digital converter element is connected in electrical circuit with the second integrating element, for receiving the second integrator output signal and for producing a digital representation of the second integrator output signal.

In another aspect of the invention, the input summing element and the first integrating element are combined in a single circuit block, are electrically balanced and directly receive a differential analog input signal.

A further aspect of the invention provides a comparator element having a one-bit sampling analog-to-digital converter. The one-bit sampling analog-to-digital converter includes a comparator for comparing the first integrator output signal and the second integrator output signal, and a digital sampling element, in circuit with the comparator, for receiving the output of the comparator and for producing in response thereto a one-bit digital offset signal.

In another aspect of the invention, the analog-to-digital converter element can have a multiple-bit digital output, and the comparator element for comparing the first and second integrator output signals can be either digital or analog. Moreover, the first or second integrating elements can be digital or analog.

A further aspect of the invention provides an analog-to-digital converter element connected in electrical circuit with both the first and second integrator elements, for receiving a combined integrator output signal representative of an arithmetic combination of the first integrator output signal and the second integrator output signal, and for producing a digital representation of the combined integrator output signal. The arithmetic combination can be a combination, in any proportion, of the first and second integrator output signals, including in limiting cases sampling only the first integrator output or the second integrator output.

The invention also includes a comparator element adapted for producing a multiple-bit digital offset signal, and a digital-to-analog offset element adapted for generating the analog offset signal in response to the multiple-bit digital offset signal.

In another aspect of the invention, the summing section contains elements for summing the analog offset signal and the analog input signal, and the output section contains differencing elements for subtracting a digital representation of the analog offset signal from the digital representation of the analog input signal.

The invention accordingly comprises apparatus embodying features of construction, combinations of elements and arrangements of parts as exemplified in the following detailed disclosure, and the scope of the invention is indicated in the claims.

Brief Description of the Drawings

For a fuller understanding of the nature and objects of the invention, reference should be made to the following detailed description and the ac-

companying drawings, in which:

FIGURE 1 is a block diagram of an analog to digital converter (ADC) according to the invention, wherein a multiple bit ADC element samples the output of a second integrator stage;

FIGURE 2 represents internal voltage vs. time waveforms at various junctions within the apparatus of FIGURE 1;

FIGURE 3 shows a spectrum of the quantization noise of the multi-bit ADC before and after differencing by the digital second differencer of FIGURE 1;

FIGURE 4 is a block diagram of a preferred embodiment of a one-bit sampling ADC element utilized in the embodiment shown in FIGURE 1;

FIGURE 5 shows a preferred embodiment of a 1-bit digital to analog converter (DAC), analog summer and first integrator;

FIGURE 6 is a block diagram of another embodiment of an ADC according to the invention, wherein the sampling multiple-bit analog to digital element samples the output of the first integrator; and

FIGURE 7 is a block diagram of another embodiment of a one-bit ADC element utilized in the embodiments of FIGURES 1 or 6, having a comparator element with positive and negative inputs.

Description of Illustrated Embodiments

FIGURE 1 is a block diagram of an analog to digital converter (ADC) according to the invention. The analog signal 40 enters the analog summer 41 where it is summed with the output 48 of the 1-bit digital to analog converter (DAC) 52. The error signal 57 is integrated by the first integrator 42 and by the second integrator 43. The outputs 44 and 45 of the first and second integrators are summed in analog summer 56, creating a signal 46 that is transmitted to the 1-bit sampling ADC 54, which in turn generates the 1-bit signal 47 that is received by the digital summer 59 and by the 1-bit DAC 52. The loop thus closed forms a double-integrator delta-sigma modulator 64.

The sampling ADC 53 samples the twice-integrated error signal 45 at the loop bit rate and converts it with N bits of resolution to digital representation. N may be any positive integer, but in typical realizations of the invention, N has ranged from 8 to 16 to achieve the necessary resolution. The digital output 49 of ADC 53 is received by the digital differencer 55 where it is second differenced in order to represent digitally the error signal 57 before integration. The second-differenced signal 58 is digitally added to the 1-bit digital signal 47 to create the digital representation 50 of the analog input signal 40. The digital representation 50 of the

analog input 40 is constructed according to the expression:

$$50_n = 49_n - 49_{n-1} - (49_{n-1} - 49_{n-2}) + 47_{n-1}$$

where 50_n , 49_n , and 47_n , respectively, represent the value of signals 50, 49 and 47 at sample n , and 50_{n-1} , 49_{n-1} and 47_{n-1} represent the value of signals 50, 49 and 47 at sample $n-1$.

An important feature of the invention is the multi-bit ADC element 53, that distinguishes the invention from prior-art delta- and delta-sigma modulators. While a standard delta modulator must operate at a high loop bit rate to make the error signal 45 as small as possible, the invention requires only that the error signal 45 remain within the measurable range of the ADC 53. The invention allows a larger loop error signal to accumulate, but, because the error signal is measured rather than forced to zero, the requirements on the loop gain and loop bit rate of the modulator are relaxed.

The digital second differencer 55 and summer 59 merge the digital bit stream signal 47--whose average value represents the input signal 40--with the digitized error signal to construct a digital representation of the analog input. The digital bit stream signal is a digital representation of the offset signal 48 that is subtracted from the analog input signal.

The invention provides, without certain limitations of prior-art techniques, conversion of broadband waveforms with high dynamic range. The invention employs double-integrator delta-sigma modulator 64 to achieve 120-140 dB of dynamic range with a loop bit rate of approximately 100 times the highest frequency of interest. This is a substantially lower ratio than that of a conventional double-integrator delta-sigma modulator, and requires less computation using a shorter-duration filter than a delta-sigma modulator of higher order. There is no loss of resolution or increase of the converter noise floor arising from non-linear methods required to suppress instability in the higher-order systems typical of the prior art.

For a given loop bit rate, the invention requires less computation in subsequent digital filters to achieve a specified suppression of out-of-band granular noise than that required by a single-bit delta- or delta-sigma modulator of any order. The invention utilizes the sampling analog-to-digital converter 54 to measure the integrated error signal within a delta-sigma modulator feedback loop with N binary bits of dynamic range and resolution, where N is a positive integer.

In an ordinary delta- or delta-sigma modulator, the single-bit serial output stream is dependent only upon the polarity of the error signal; the amplitude of the error signal is discarded. We have

found, however, that considerable information that permits construction of a digital representation of the analog input signal is contained in a measurement of the amplitude of the error signal. In accordance with the invention, therefore, the integrated loop error signal 45 is digitized by sampling A/D converter 53 to H bits, differenced by digital differencer 55, and added to the 1-bit output of the delta-sigma modulator 64 to provide a high-resolution digital output 50. If the delta-sigma modulator output 47 has a dynamic range equivalent to M bits, the digital output signal 50 may have a dynamic range and resolution equivalent to as much as $M + N$ bits within the desired signal passband. This dynamic range is recoverable through subsequent digital filtration to remove the delta-sigma modulator granular noise outside the signal passband.

The embodiment illustrated in FIGURE 1 also provides apparatus for extension of the dynamic range and resolution of a standard A/D converter, having N bits of dynamic range. As discussed above, the delta-sigma modulator 64 generates an analog offset signal 48, having M bits of dynamic range, that is subtracted from the analog input signal 40 to create an analog difference signal 57. The analog difference signal 57 is integrated twice and digitized by the A/D converter 54 to N bits of resolution. A digital representation 50 of the analog input signal 40, having $N + M$ bits of dynamic range, is constructed by adding the digital representation 47 of the offset signal 48 supplied by the delta-sigma modulator 64 to a numerically differenced, electrically integrated, digitized difference signal 58.

An important feature of the invention is that the difference signal 57 is integrated in two integrators 42 and 43 before digitization by the A/D converter 54. The integration provides high gain at frequencies within the signal passband, which is a fraction of the loop bit rate frequency, without potential saturation at high frequencies. The increased low-frequency gain reduces quantization noise for signals at the frequencies of interest.

Thus, the invention, which can be viewed either as an extension of the dynamic range and efficiency of a delta-sigma modulator by measurement of the loop error signal, or as an extension of the dynamic range of an A/D converter by subtraction of an offset signal that is generated by a delta-sigma modulator, yields a greater combined dynamic range and differential linearity than either device independently. The invention provides, for a given dynamic range, a minimum loop bit rate, and thus the lowest potential for charge injection errors, in an unconditionally stable delta-sigma loop.

Those skilled in the art will understand that while FIGURE 1 shows the multiple-bit ADC 53

configured for sampling the output signal 45 of second integrator 43 only, ADC 53 can be configured to sample any arithmetic combination of the first and second integrator output signals 44 and 45, including, in the limiting case, sampling only one of the two integrator output signals 44 and 45.

FIGURE 2 illustrates voltage-to-time waveforms at the output 44 of the first integrator; at the output 45 of the second integrator, sampled by the multi-bit A/D converter 53; at the output of analog summer 56, which is also the input of the 1-bit A/D 54; at the output 47 of the 1-bit A/D 54; and at the output 50 of the digital summer 59. The digital output signal 50 is magnified 100 times in FIGURE 2 relative to the signals 44, 49, 46, 47. It is apparent from FIGURE 2 that the granular noise in the digital output signal 50 is of order 1000 times smaller than the 1-bit output 47 of the delta-sigma modulator. In addition, the spectrum of the noise at 50 is reduced at low frequencies, as shown in FIGURE 3. Subsequent digital low-pass filtration of the digital output 50 can provide increased dynamic range and reduced quantization noise at frequencies low relative to the loop bit rate. Below roughly 0.01 of the loop bit rate, actual dynamic range may be expected to exceed 130-140 dB.

FIGURE 3 shows the action of the second differencer 55 (shown in FIGURE 1) on the signal 49, transmitted to differencer 55 by multi-bit ADC element 53. This quantization noise spectrum of signal 49 is frequency independent, as reflected by the horizontal amplitude to frequency plot. The quantization noise spectrum of the differenced signal 58, however, is reduced at frequencies low relative to the loop bit rate. $F_{Nyquist}$, as known in the art, is $1/2$ the loop bit rate frequency.

FIGURE 4 shows a preferred embodiment of the 1-bit sampling A/D converter 54. The first and second integrator output signals 44 and 45 are summed by adder 56, producing signal 46. Signal 46 is transmitted to the "+" input of comparator 90 of sampling ADC 54. Comparator 90 compares the value of signal 46 with that of reference signal 91 to produce comparator result 72. The sampling clock signal 61 clocks the comparator result 72 present at the D input of flip-flop 74 to the flip-flop's Q output, where the one-bit value of the comparator output 72 is stored until the next active transition of the sampling clock. The same sampling clock controls sampling by the multi-bit ADC 53.

A further aspect of the invention, illustrated in FIGURE 5, includes an electrically-balanced fully-differential 1-bit digital-to-analog converter 52, analog summer 41, and analog integrator 42 which compensate for charge injection errors caused by unbalanced switches. The illustrated analog summer 41 includes a switched capacitor network. The

sampling clock 61, which also controls sampling by the ADCs 53 and 54, alternately charges through switches 21 a capacitor 20 from a voltage reference 51, and discharges the capacitor 20 through switches 22 or 23 into resistors 26 of the analog summer and first integrator 41, 42. The differential analog input is summed directly through resistors 27 of the analog summer and first integrator 41, 42. The charge stored on capacitor 20 is thus transferred to integrating capacitors 28, to complete a clocked digital-to-analog conversion of the 1-bit input 47, which controls the polarity of discharge of capacitor 20 into the analog summer and first integrator.

Logic implemented by inverters 31, 32 and gates 29, 30 provide that the discharge paths through switches 22 and 23 are not active while switch 21 is closed, i.e., during charging of the capacitor 20.

Those skilled in the art will understand that resistors 26 and 27 can be replaced with a switched capacitor network. Moreover, other embodiments of the invention may include operation of the 1-bit DAC 52 as a switched current source by deleting switches 21 and capacitor 20, and converting voltage reference 51 to a current source. In other embodiments of the invention the 1-bit DAC 52 can be replaced by a converter having more quantization levels.

This feature of the invention permits achievement of low broad-band noise, a low temperature coefficient of drift, and relative insensitivity to variation in component characteristics and to their change with time. The circuit illustrated in FIGURE 5 is an electrically-balanced, fully differential circuit that features high common mode rejection. The circuit also provides compensation to first order of charge injection by the analog switches, because the switches are always active, and only the polarity is modulated.

Those skilled in the art will understand that alternative embodiments of the invention may implement the analog summer 56, integrators 42 and 43, and 1-bit DAC 52 as a single-ended circuit. A single-ended circuit embodiment of the invention would use fewer components and be more easily implemented as a monolithic or hybrid component, possibly at the expense of increased thermal coefficient of drift and first-order sensitivity to component variations.

While optimum reduction of quantization noise of the digitized signal 49 is achieved for a given loop bit rate by sampling the output signal 45 of the second integrator 43, in another embodiment of the invention, the output 44 of the first integrator 42 is sampled. This embodiment of the invention is illustrated in FIGURE 6. The embodiment of FIGURE 6 is otherwise identical to that described

above in connection with FIGURE 1. The embodiment shown in FIGURE 6 has two principal advantages over that shown in FIGURE 1. The first advantage is that a fast, accurate sample-and-hold amplifier is not required for sampling the output 44 of first integrator 42. In the embodiment illustrated in FIGURE 1, sampling the output 45 of the second integrator requires a fast and accurate sample-and-hold amplifier because signal 45 slews rapidly. Those skilled in the art will recognize that in general, the slew rate of second integrator output 45 is much higher than that of the input signal 40.

Moreover, in the embodiment shown in FIGURE 6, a less complex first-difference expression is calculated to derive the digital output signal 50. In the notation used above in connection with FIGURE 1, this expression is:

$$50_n = 49_n - 49_{n-1} + 47_{n-1}$$

In the embodiment shown in FIGURE 6, the first differencing operation reduces quantization noise at frequencies low relative to the loop bit rate as illustrated in FIGURE 3 for the embodiment sampling second integrator output 45, but the reduction is less pronounced.

FIGURE 7 shows an alternate embodiment of the 1-bit sampling ADC converter 54. The outputs 44 and 45 of the first and second integrators are received by the positive and negative inputs of the comparator. The embodiment shown in FIGURE 7 is otherwise substantially identical to that shown in FIGURE 4.

It will thus be seen that the invention efficiently attains the objects set forth above, among those made apparent from the preceding description. In particular, the invention provides high-resolution analog-to-digital conversion apparatus having low differential non-linearity, capable of processing signals having a large dynamic range and frequency content, such as seismic and audio signals.

It will be understood that changes may be made in the above construction and in the foregoing sequences of operation without departing from the scope of the invention. Those skilled in the art will understand, for example, that the multiple-bit ADC 53 can be configured for sampling any arithmetic combination of the first and second integrator output signals 44 and 45. Moreover, while a one-bit sampling ADC 54 is illustrated, a multiple-bit ADC can be employed to generate a multiple-bit digital signal 47. It is accordingly intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative rather than in a limiting sense.

Claims

1. Analog-to-digital conversion apparatus comprising

A. input summing means (41) for receiving an analog input signal (40) and an analog offset signal (48) and producing a residual signal (57) in response to an arithmetic combination of said analog input signal and said analog offset signal,

B. first integrating means (42), in electrical circuit with said input summing means (41), for receiving and integrating said produced residual signal (57) to produce a first integrator output signal (44),

C. second integrating means (43), in electrical circuit with said first integrating means (42), for receiving and integrating said first integrator output signal (44) to produce a second integrator output signal (45),

D. comparator means (54/56), in electrical circuit with said first integrating means (42) and said second integrating means (43), for comparing said first integrator output signal (44) and said second integrator output signal (45), and producing in response thereto a digital offset signal (47),

E. digital-to-analog offset means (52), in electrical circuit with said comparator means (54) and said input summing means (41), for receiving said digital offset signal (47) produced by said comparator means (54), producing in response thereto said analog offset signal (48), and transmitting said analog offset signal to said input summing means (41), and

F. output means for producing a digital representation (50) of said analog input signal (40)

characterized in that the apparatus further comprises

G. a multi-bit analog-to-digital converter means (53), in electrical circuit with at least one of said first or second integrating means (42, 43), for receiving said first or second integrator output signal (44, 45) or a combined signal thereof, sampling this output signal (44, 45) or a combined signal and producing a multi-bit digital representation (49) thereof,

H. a digital differencer (55) for differencing the digital output signal (49) of the multi-bit analog-to-digital converter (53) in order to produce a digital representation (58) of the residual signal (57), and in that

I. a digital summer (59) in electrical circuit with said digital differencer (55) and said comparator means (56/54), for respectively

above in connection with FIGURE 1. The embodiment shown in FIGURE 6 has two principal advantages over that shown in FIGURE 1. The first advantage is that a fast, accurate sample-and-hold amplifier is not required for sampling the output 44 of first integrator 42. In the embodiment illustrated in FIGURE 1, sampling the output 45 of the second integrator requires a fast and accurate sample-and-hold amplifier because signal 45 slews rapidly. Those skilled in the art will recognize that in general, the slew rate of second integrator output 45 is much higher than that of the input signal 40.

Moreover, in the embodiment shown in FIGURE 6, a less complex first-difference expression is calculated to derive the digital output signal 50. In the notation used above in connection with FIGURE 1, this expression is:

$$50_n = 49_n - 49_{n-1} + 47_{n-1}$$

In the embodiment shown in FIGURE 6, the first differencing operation reduces quantization noise at frequencies low relative to the loop bit rate as illustrated in FIGURE 3 for the embodiment sampling second integrator output 45, but the reduction is less pronounced.

FIGURE 7 shows an alternate embodiment of the 1-bit sampling ADC converter 54. The outputs 44 and 45 of the first and second integrators are received by the positive and negative inputs of the comparator. The embodiment shown in FIGURE 7 is otherwise substantially identical to that shown in FIGURE 4.

It will thus be seen that the invention efficiently attains the objects set forth above, among those made apparent from the preceding description. In particular, the invention provides high-resolution analog-to-digital conversion apparatus having low differential non-linearity, capable of processing signals having a large dynamic range and frequency content, such as seismic and audio signals.

It will be understood that changes may be made in the above construction and in the foregoing sequences of operation without departing from the scope of the invention. Those skilled in the art will understand, for example, that the multiple-bit ADC 53 can be configured for sampling any arithmetic combination of the first and second integrator output signals 44 and 45. Moreover, while a one-bit sampling ADC 54 is illustrated, a multiple-bit ADC can be employed to generate a multiple-bit digital signal 47. It is accordingly intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative rather than in a limiting sense.

Claims

1. Analog-to-digital conversion apparatus comprising

A. input summing means (41) for receiving an analog input signal (40) and an analog offset signal (48) and producing a residual signal (57) in response to an arithmetic combination of said analog input signal and said analog offset signal,

B. first integrating means (42), in electrical circuit with said input summing means (41), for receiving and integrating said produced residual signal (57) to produce a first integrator output signal (44),

C. second integrating means (43), in electrical circuit with said first integrating means (42), for receiving and integrating said first integrator output signal (44) to produce a second integrator output signal (45),

D. comparator means (54/56), in electrical circuit with said first integrating means (42) and said second integrating means (43), for comparing said first integrator output signal (44) and said second integrator output signal (45), and producing in response thereto a digital offset signal (47),

E. digital-to-analog offset means (52), in electrical circuit with said comparator means (54) and said input summing means (41), for receiving said digital offset signal (47) produced by said comparator means (54), producing in response thereto said analog offset signal (48), and transmitting said analog offset signal to said input summing means (41), and

F. output means for producing a digital representation (50) of said analog input signal (40)

characterized in that the apparatus further comprises

G. a multi-bit analog-to-digital converter means (53), in electrical circuit with at least one of said first or second integrating means (42, 43), for receiving said first or second integrator output signal (44, 45) or a combined signal thereof, sampling this output signal (44, 45) or a combined signal and producing a multi-bit digital representation (49) thereof,

H. a digital differencer (55) for differencing the digital output signal (49) of the multi-bit analog-to-digital converter (53) in order to produce a digital representation (58) of the residual signal (57), and in that

I. a digital summer (59) in electrical circuit with said digital differencer (55) and said comparator means (56/54), for respectively



receiving therefrom said multi-bit digital representation (58) of the residual signal and said digital offset signal (47), and for producing in response thereto a digital representation (50) of said analog input signal (40) and that is an arithmetic combination of different sampled values of the output signal (49) from the multi-bit analog to digital converter means (53) and of the digital offset signal (47).

2. Analog-to-digital conversion apparatus according to claim 1, wherein said input summing means (41) and said first integrating means (42) are electrically balanced.

3. Analog-to-digital conversion apparatus according to claim 2, wherein said input summing means (41) and said first integrating means (42) receive a differential input signal.

4. Analog-to-digital conversion apparatus according to any of claims 1 to 3, wherein said comparator means (54/56) comprises a one-bit sampling analog-to-digital converter (54), said analog-to-digital converter including

(i) a comparator (90) for comparing said first integrator output signal (44) and said second integrator output signal (45), and
(ii) digital sampling means (74), in circuit with said comparator (90), for receiving the output (72) of said comparator (90) and producing in response thereto the one-bit digital offset signal (47).

5. Analog-to-digital conversion apparatus according to any of claims 1 to 4, wherein said comparator means includes a digital comparator, and wherein at least one of said first and second integrating means includes a digital integrator.

6. Analog-to-digital conversion apparatus according to any of claims 1 to 4, wherein said comparator means includes an analog comparator, and wherein at least one of said first and second integrating means includes an analog integrator.

7. Analog-to-digital conversion apparatus according to any of claims 1 to 6, wherein said comparator means (54/56) includes means for producing a multiple-bit digital offset signal (47), and wherein said digital-to-analog offset means (52) includes means for generating said analog offset signal (48) in response to said multiple-bit digital offset signal (47).

8. Analog-to-digital conversion apparatus according to any of claims 1 to 7, wherein said input summing means (41) contains means for summing said analog offset signal (48) and said analog input signal (40), and wherein said output means contains means for adding said digital representation (47) of the analog offset signal and said digital representation (58) of the analog residual signal (57).

9. Analog-to-digital conversion apparatus according to any of claims 1 to 8, wherein the digital representation (50) of said analog input signal (40) is constructed according to the expression:

$$50_n = 49_n - 49_{n-1} - (49_{n-1} - 49_{n-2}) + 47_{n-1}$$

where 50_n , 49_n , and 47_n , respectively, represent the value of signals

50 = output of said summer (59)

49 = output of said multi-bit A-D converter means (53)

47 = digital offset signal

at sample n , and 50_{n-1} , 49_{n-1} and 47_{n-1} represent the value of signals 50 , 49 and 47 at sample $n-1$.

10. Analog-to-digital conversion apparatus according to any of claims 1 to 8, wherein the digital representation (50) of said analog input signal (40) is constructed according to the expression:

$$50_n = 49_n - 49_{n-1} + 47_{n-1}$$

where 50_n , 49_n , and 47_n , respectively, represent the value of signals

50 = output of said summer (59)

49 = output of said multi-bit A-D converter means (53)

47 = digital offset signal

at sample n , and 50_{n-1} , 49_{n-1} and 47_{n-1} represent the value of signals 50 , 49 and 47 at sample $n-1$.

Patentansprüche

1. Analog-Digital-Umsetzer, enthaltend

A. eine Eingangs-Summierstufe (41), die ein analoges Eingangssignal (40) und ein analoges Kompensationssignal (48) empfängt und daraus ein Restsignal (57) abhängig von einer arithmetischen Kombination des Eingangssignals und des Kompensationssignals erzeugt,

B. eine mit der Eingangs-Summierstufe (41) elektrisch verbundene erste Integratorstufe



(42), die das Restsignal (57) empfängt und integriert und daraus ein Ausgangssignal (44) der ersten Integratorstufe erzeugt,

C. eine mit der ersten Integratorstufe (42) elektrisch verbundene zweite Integratorstufe (43), die das Ausgangssignal (44) der ersten Integratorstufe empfängt und integriert und daraus ein Ausgangssignal (45) der zweiten Integratorstufe erzeugt,

D. eine mit der ersten und zweiten Integratorstufe (42, 43) elektrisch verbundene Komparatorstufe (54/56), die das Ausgangssignale (44) der ersten Integratorstufe und das Ausgangssignal (45) der zweiten Integratorstufe miteinander vergleicht und daraus ein digitales Steuersignal (47) ableitet,

E. einen mit der Komparatorstufe (54) und der Eingangs-Summierstufe (41) elektrisch verbundenen Digital-Analog-Wandler (52) für das Kompensationssignal, der das digitale Steuersignal (47) empfängt, das von der Komparatorstufe (54) erzeugt wurde, abhängig hiervon das analoge Kompensationssignal (48) erzeugt und dieses an die Eingangs-Summierstufe (41) weitergibt, sowie

F. eine Ausgangsstufe, die eine digitale Darstellung (50) des analogen Eingangssignals (40) erzeugt, dadurch gekennzeichnet, daß die Einrichtung ferner enthält:

G. eine Analog-Digital-Wandler-Stufe (53) mit mehreren Bit Auflösung, die mit mindestens einer der Integratorstufen (42, 43) elektrisch verbunden ist, und die das Ausgangssignal (44, 45) der ersten oder der zweiten Integratorstufe oder eine Kombination davon empfängt, dieses Ausgangssignal (44, 45) oder das kombinierte Signal abtastet und eine digitale Darstellung (49) mit mehreren Bit Auflösung erzeugt,

H. einen digitalen Differenzrechner (55), der das digitale Ausgangssignal (49) der Analog-Digital-Wandler-Stufe (53) mit mehreren Bit Auflösung so differenziert, daß daraus eine digitale Darstellung (58) des Restsignals (57) entsteht, und

I. einen digitalen Summierer (59), der mit dem digitalen Differenzrechner (55) und der Komparatorstufe (54/56) elektrisch verbunden ist, so daß er von diesen die digitale Darstellung (58) des Restsignals mit mehreren Bit Auflösung und das digitale Steuersignal (47) empfängt und daraus eine digitale Darstellung (50) des analogen Eingangssignals herstellt, die eine arithmetische Kombination verschiedener Abtastwerte des Ausgangssignals (49) der Analog-Digital-Wandler-Stufe (53) mit mehreren Bit Auflö-

sung und des digitalen Steuersignals (47) ist.

2. Analog-Digital-Umsetzer nach Patentanspruch 1, bei dem die Eingangs-Summierstufe (41) und die erste Integratorstufe (42) als symmetrische Gegentaktschaltung aufgebaut sind.

3. Analog-Digital-Umsetzer nach Patentanspruch 2, bei dem die Eingangs-Summierstufe (41) und die erste Integratorstufe (42) ihre Eingangssignale als Gegentaktsignale empfangen.

4. Analog-Digital-Umsetzer nach einem der Patentansprüche 1 bis 3, in dem die Komparatorstufe (54/56) einen abtastenden Ein-Bit-Analog-Digital-Wandler (54) enthält und dieser

(i) einen Komparator (90), der das Ausgangssignal (44) der ersten Integratorstufe und das Ausgangssignal (45) der zweiten Integratorstufe miteinander vergleicht, sowie

(ii) einen mit dem Komparator (90) elektrisch verbundenen digitalen Abtaster (74) enthält, der das Ausgangssignal (72) dieses Komparators (90) empfängt und daraus das digitale Steuersignal (47) mit einem Bit Auflösung erzeugt.

5. Analog-Digital-Umsetzer nach einem der Patentansprüche 1 bis 4, in dem die Komparatorstufe einen digitalen Komparator enthält, und in dem mindestens eine der beiden Integratorstufen einen digitalen Integrator enthält.

6. Analog-Digital-Umsetzer nach einem der Patentansprüche 1 bis 4, in dem die Komparatorstufe einen analogen Komparator enthält, und in dem mindestens eine der beiden Integratorstufen einen analogen Integrator enthält.

7. Analog-Digital-Umsetzer nach einem der Patentansprüche 1 bis 6, in dem die Komparatorstufe (54/56) eine Einrichtung enthält, die ein digitales Steuersignal (47) mit mehreren Bit Auflösung erzeugt, und in dem der Digital-Analog-Wandler (52) für das Kompensationssignal eine Einrichtung enthält, die das analoge Kompensationssignal (48) abhängig von dem Steuersignal (47) mit mehreren Bit Auflösung erzeugt.

8. Analog-Digital-Umsetzer nach einem der Patentansprüche 1 bis 7, in dem die Eingangs-Summierstufe (41) eine Einrichtung enthält, die das analoge Kompensationssignal (48) und das analoge Eingangssignal (40) summiert, und in dem die Ausgangsschaltung eine Einrichtung enthält, die die digitale Darstellung (47) des



analogen Kompensationssignals und die digitale Darstellung (58) des Restsignals (57) adaptiert.

Analog-Digital-Wandler nach einem der Patentansprüche 1 bis 8, in dem die digitale Darstellung (50) des Eingangssignals (40) gebildet ist gemäß der Beziehung

$$50_n = 49_n - 49_{n-1} - (49_{n-1} - 49_{n-2}) + 47_{n-1} \quad 10$$

wobei 50_n , 49_n und 47_n jeweils den Wert folgender Signale beim Zeittakt n bedeuten:

50 = Ausgangssignal des digitalen Summierers (59) 15

49 = Ausgangssignal der Analog-Digital-Wandler-Stufe

(53) mit mehrerer Bit Auflösung

47 = Digitales Steuersignal

und 50_{n-1} , 49_{n-1} und 47_{n-1} den Wert der Signale 50 , 49 und 47 beim Zeittakt $n-1$ bedeuten. 20

10. Analog-Digital-Umsetzer nach einem der Patentansprüche 1 bis 8, in dem die digitale Darstellung (50) des Eingangssignals (40) gebildet ist gemäß der Beziehung 25

$$50_n = 49_n - 49_{n-1} + 47_{n-1} \quad 30$$

wobei 50_n , 49_n und 47_n jeweils den Wert folgender Signale beim Zeittakt n bedeuten:

50 = Ausgangssignal des digitalen Summierers (59)

49 = Ausgangssignal der Analog-Digital-Wandler-Stufe (53) mit mehreren Bit Auflösung 35

47 = Digitales Steuersignal

und 50_{n-1} , 49_{n-1} und 47_{n-1} den Wert der Signale 50 , 49 und 47 beim Zeittakt $n-1$ bedeuten. 40

Revendications

1. Dispositif de convertisseur analogique/digital comprenant : 45

- un moyen de sommation d'entrée (41) pour la réception d'un signal analogique d'entrée (40) et d'un signal analogique de compensation (48) et pour la production d'un signal résiduel (57) en réponse à une combinaison arithmétique dudit signal analogique d'entrée et dudit signal analogique de compensation; 50
- un premier moyen d'intégration (42), raccordé électriquement audit moyen de sommation d'entrée (41), pour la réception et l'intégration dudit signal résiduel produit (57) afin de produire un premier 55

signal de sortie d'intégrateur (44);

- un second moyen d'intégration (43), raccordé électriquement audit premier moyen d'intégration (42), pour la réception et l'intégration dudit premier signal de sortie d'intégrateur (44) afin de produire un second signal de sortie d'intégrateur (45);
 - un moyen de comparateur (54/56), raccordé électriquement audit premier moyen d'intégration (42) et audit second moyen d'intégration (43), pour la comparaison dudit premier signal de sortie d'intégrateur (44) et dudit second signal de sortie d'intégrateur (45) et pour la production en réponse d'un signal numérique de compensation (47);
 - un moyen de compensation digital/analogique (52), raccordé électriquement audit moyen de comparateur (54) et audit moyen de sommation d'entrée (41), pour la réception dudit signal numérique de compensation (47) produit par ledit moyen de comparateur (54), pour la production en réponse dudit signal analogique de compensation (48) et pour la transmission dudit signal analogique de compensation audit moyen de sommation d'entrée (41); et
 - un moyen de sortie pour la production d'une représentation numérique (50) dudit signal analogique d'entrée (40), caractérisé en ce que le dispositif comprend, de plus:
 - un moyen de convertisseur analogique/digital sur plusieurs bits (53), raccordé électriquement à au moins un desdits premier ou second moyens d'intégration (42, 43), pour la réception dudit premier ou dudit second signal de sortie d'intégrateur (44, 45) ou un signal combiné de ces derniers, pour l'échantillonnage de ce signal de sortie (44, 45) ou d'un signal combiné et pour la production d'une représentation numérique sur plusieurs bits (49) de celui-ci;
 - un différenciateur digital (55) pour différencier le signal numérique de sortie (49) du convertisseur analogique/digital sur plusieurs bits (53) de façon à produire une représentation numérique (58) du signal résiduel (57);
- et en ce que, comme moyen de sortie, un sommateur digital (59), raccordé électriquement audit différenciateur digital (55) et audit moyen de comparateur (56/54), pour en recevoir respectivement ladite représentation numérique sur



- plusieurs bits (58) du signal résiduel et ledit signal numérique de compensation (47) et pour la production en réponse d'une représentation numérique (50) dudit signal analogique d'entrée (40), c'est-à-dire une combinaison arithmétique de différentes valeurs échantillonnées du signal de sortie (49) fourni par le moyen de convertisseur analogique/digital sur plusieurs bits (53) et du signal numérique de compensation (47).
2. Dispositif de conversion analogique/digital selon la revendication 1, dans lequel ledit moyen de sommation d'entrée (41) et ledit premier moyen d'intégration (42) sont électriquement équilibrés.
 3. Dispositif de conversion analogique/digital selon la revendication 2, dans lequel ledit moyen de sommation d'entrée (41) et ledit premier moyen d'intégration (42) reçoivent un signal différentiel d'entrée.
 4. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 3, dans lequel ledit moyen de comparateur (54/56) comprend un convertisseur analogique/digital d'échantillonnage sur un bit (54), ledit convertisseur analogique/digital comprenant:
 - un comparateur (90) pour la comparaison dudit premier signal de sortie d'intégrateur (44) et dudit second signal de sortie d'intégrateur (45), et
 - un moyen digital d'échantillonnage (74), raccordé audit comparateur (90), pour la réception de la sortie (72) dudit comparateur (90) et pour la production en réponse du signal numérique de compensation d'un bit (47).
 5. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 4, dans lequel ledit moyen de comparateur comprend un comparateur digital et dans lequel au moins un desdits premier et second moyens d'intégration comprend un intégrateur digital.
 6. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 4, dans lequel ledit moyen de comparateur comprend un comparateur analogique et dans lequel au moins un desdits premier et second moyens d'intégration comprend un intégrateur analogique.
 7. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 6, dans lequel ledit moyen de comparateur (54/56) comprend un moyen pour la production d'un signal numérique de compensation sur plusieurs bits (47) et dans lequel ledit moyen digital/analogique de compensation (52) comprend un moyen pour la génération dudit signal analogique de compensation (48) en réponse audit signal numérique de compensation sur plusieurs bits (47).
 8. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 7, dans lequel ledit moyen de sommation d'entrée (41) contient un moyen pour additionner ledit signal analogique de compensation (48) et ledit signal analogique d'entrée (40) et dans lequel ledit moyen de sortie contient un moyen pour combiner ladite représentation numérique (47) du signal analogique de compensation avec ladite représentation numérique (58) du signal analogique résiduel (57).
 9. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 8, dans lequel la représentation numérique (50) dudit signal analogique d'entrée (40) est établie selon l'expression suivante :

$$50_n = 49_n - 49_{n-1} - (49_{n-1} - 49_{n-2}) + 47_{n-1}$$
 où 50_n , 49_n et 47_n représentent respectivement la valeur des signaux suivants :
 - 50 = la sortie dudit additionneur (59)
 - 49 = la sortie dudit moyen de convertisseur A/D sur plusieurs bits (53)
 - 47 = le signal numérique de compensation pour l'échantillon n et 50_{n-1} , 49_{n-1} et 47_{n-1} représentent la valeur des signaux 50, 49 et 47 pour l'échantillon $n-1$.
 10. Dispositif de conversion analogique/digital selon l'une quelconque des revendications 1 à 8, dans lequel la représentation numérique (50) dudit signal analogique d'entrée (40) est établie selon l'expression suivante :

$$50_n = 49_n - 49_{n-1} + 47_{n-1}$$
 où 50_n , 49_n et 47_n représentent respectivement la valeur des signaux suivants :
 - 50 = la sortie dudit additionneur (59)
 - 49 = la sortie dudit moyen de convertisseur A/D sur plusieurs bits (53)
 - 47 = le signal numérique de compensation



pour l'échantillon n et 50_{n-1} , 49_{n-1} et 47_{n-1} représentent la valeur des signaux 50, 49 et 47 pour l'échantillon $n-1$.

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