

Description

The present invention relates to memories which have a chip select function, and more particularly to memories which have the chip select function and which utilize address transition detection.

Background of the Invention

A chip select function has long been used in memories to disable a memory circuit to reduce power consumption. The memory is not responsive to external address signals when deselected by the chip select signal. Although there is power savings, there is also the potential problem of a loss of speed when switching from the deselected mode to the selected mode because the circuitry is powered-down and there is a recovery time. One of the major power losses in CMOS is the first input stage for an input signal because it generally must be compatible with TTL signal levels. A logic high TTL signal may be as low as 2.0 volts. Such a logic high, which is suppose to turn off a P channel transistor, will cause the input P channel transistor to be conductive and thus waste power. Consequently, it is desirable to disable the input stage of as many input signals as is feasible during deselect mode. In many modern memories, however, address transition is used for equilibrating bit lines as well as for other functions, for the purpose of increasing the speed of operation which is reflected in lower access times. When an address buffer which receives an external address signal receives a logic low input, the transition from the deselect to select modes will cause the buffer to provide an address transition which is detected as such if the buffer is disabled during the deselect mode. There is then an unnecessary equalization pulse generated as a consequence of the address buffer being disabled during the deselect mode. There is, however, a delay in generating the equalization pulse because there is a delay in enabling the address buffer because there is an unavoidable delay in responding to the chip select signal. This causes a longer access time for the case in which the memory circuit is coming out of the chip deselect mode than for the case of a address transition during the select mode. The alternative to having the extended access time has been to not disable the address buffers during the deselect mode and incur the additional power loss.

Summary of the Invention

An object of the present invention is to provide an improved chip select operation for a memory.

Another object of the invention is to provide an

improved memory which utilizes address transition detection and which has a chip select operation.

Yet another object of the invention is to provide an improved technique for transferring a memory from a deselect mode to a select mode.

In accordance with the present invention there is provided a memory circuit which is enabled in response to a occurrence of a chip select signal (CS), comprising:

a plurality of address input means, each for receiving an address signal and being enabled in response to a occurrence of the chip select signal;

transition detection means, coupled to the output of the plurality of address input means, for detecting a transition of an address signal; said memory circuit being characterised by:

disabling means for disabling the transition detection means for a predetermined time delay following a occurrence of the chip select signal.

In accordance with the present invention there is also provided a method as defined in claim 7.

Brief Description of the Drawings

FIG. 1 is an external diagram of a conventional memory;

FIG. 2 is combination of circuit and block diagram of a portion of a memory of the prior art;

FIG. 3 is a first timing diagram of conventional operation of memory signals;

FIG. 4 is a second timing diagram of signals as operated in the prior art;

FIG. 5 is a block diagram of a portion of a memory according to a preferred embodiment of the invention;

FIG. 6 is a timing diagram of signals as operated in the preferred embodiment of the invention; and

FIG. 7 is a circuit diagram of a portion of the block diagram of FIG. 5.

Description of the Invention

Shown in FIG. 1 is a conventional static random access memory (SRAM) 10 in block form having a plurality of row address signal inputs A0, A1, A2, and AN; column address signals AC, a chip select signal *CS; a data I/O D; and a read/write signal R/W. Chip select signal *CS determines if memory 10 is in an enabled or disabled state. When signal *CS is a logic high memory 10 is disabled and thus deselected. When signal *CS is a logic low, memory 10 is enabled and thus selected. When selected, memory 10 is responsive to the address signals to either read or write data D as determined by signal R/W. Memory 10 is shown as an example of conventional memory with a single data line. Memory 10 can be then, for example a

64Kx1 SRAM. In such case there will be 16 address signals. Some will be row address signals and the others will be column address signals. For address transition detection purposes, a transition of a column address is detected separately from that of row address transition. In many cases the address transition detection is only for a row address transition because equilibration of bit lines is not deemed necessary for a column address change. Address signals A0, A1, A2, and AN are representative of the row address signals. The detection of a row address transition is for equilibrating bit lines but may also be used for other purposes such as enabling decoders.

Shown in FIG. 2 is a circuit 11 of the prior art for use in memory 10, which is used for address transition detection and which uses the chip select signal *CS. Circuit 11 is comprised of an input pad 12 for receiving chip select signal *CS, an input pad 13 for receiving address signal AN, an address input amplifier 14 for providing buffered address signal ANB in response to signal AN, a transition detector 15 for providing an address transition pulse *ANTX in response to a transition of signal ANB, an input buffer 16 for providing a buffered chip select signal *CSB in response to chip select signal *CS, a delay circuit 17 for providing a delayed chip select signal *CSD in response to signal *CSB, and an equalization pulse (EQ) generator 18 for generating an equalization pulse EQ. Amplifier 14 comprises an input circuit 19, and a buffer 21. Input circuit 19 comprises a P channel transistor 22, a P channel transistor 23, an N channel transistor 24, an N channel transistor 25. All of the transistors described herein are insulated gate field effect transistors of the enhancement type. Transistor 22 has a source connected to a positive power supply terminal for receiving, for example, 5 volts, a gate connected to an output of buffer 16 for receiving signal *CSB, and a drain. Transistor 23 has a source connected to the drain of transistor 22, a gate connected to pad 13 for receiving signal AN, and a drain. Transistor 24 has a drain connected to the drain of transistor 23, a gate connected to pad 13 for receiving signal AN, and a source connected to ground. Transistor 25 has a drain connected to the drain of transistor 24, a gate for receiving signal *CSB, and a source connected to ground. Transistors 22-25 which form input circuit 19 also form a conventional CMOS NOR gate.

Transition detector 15 provides pulse *ANTX as a negative going pulse in response to an address transition of signal AN. The asterisk (*) preceding a signal indicates that the signal is active when it is a logic low. Pulse *ANTX is normally a logic high but switches to a logic low for about 8 nanoseconds in response to an address transition of signal AN. EQ generator 18 receives pulse *ANTX and also re-

ceives pulses *AOTX, *A1TX, and *A2TX which have the same characteristics as pulse *ANTX except that pulse *AOTX, *A1TX, and *A2TX are active in response to an address transition of address signals A0, A1, and A2, respectively. EQ generator 18 provides a NAND function so that pulse EQ will remain active until all of the input pulses AOTX-ANTX switch to a logic high. A timing diagram of normal operation for a transition of signal AN is shown in FIG. 3. At a time t0, signal AN makes a transition. The particular transition shown is from a logic low to a logic high. Input circuit 19 and buffer 21 respond to switch signal ANB from a logic low to a logic high at a time t1 about 5 nanoseconds after time t0. Transition detector 15 responds to buffer 21 by causing signal *ANTX to become active (a logic low) at a time t2 about 2 nanoseconds after time t1. Signal *ANTX remains low for about 8 nanoseconds. EQ generator 18 responds by activating pulse EQ at a time t3 about 4 nanoseconds after time t2. When pulse *ANTX switches back to a logic high at time t4, EQ generator 18 responds by causing pulse EQ to switch to a logic low at a time t5 about 4 nanoseconds following time t4. Valid data D appears at a time t6 about 10 nanoseconds following time t5. This is the desired operation. For this example in FIG. 3, the access time, the time from t0 to t6, is 29 nanoseconds. This is given as an example. The actual times are highly dependent upon the actual process used in the manufacturing of the memory. The times given are comparable to those for a high speed state of the art process.

Shown in FIG. 4 is a timing diagram for the operation of circuit 11 of FIG. 2 when memory 10 comes of the deselect mode. At a time t0, chip select signal *CS switches from a logic high to a logic low so that memory 10 is then selected. Address signal is assumed to be a continuous logic low. With signal AN at a logic low, transistor 24 is non-conductive. Prior to time t0, chip select signal *CS is a logic high so that buffer 16 provides signal *CSB also at a logic high. With signal *CSB at a logic high transistor 25 is conductive and transistor 22 is non-conductive, disabling input circuit 19 and causing signal *ANI to be a logic low. This is the conventional technique which is effective in reducing power loss during the deselect mode. About 5 nanoseconds after signal *CS switches to a logic low, buffer 16 provides signal *CSB to input circuit 19 at a logic low, enabling input circuit 19 by causing transistor 22 to be conductive and transistor 25 to be non-conductive. With signal AN at a logic low, input circuit 19 responds to signal *CSB switching to a logic low at a time t1 by causing signal *ANI to switch to a logic high. Buffer 21 responds to signal *ANI switching logic state by causing signal ANB to switch logic state at time t2.

Transition detector 15 responds to signal ANB switching state by activating pulse *ANTX at a time t3. Buffer 21, generates signals in addition to signal ANB. These additional signals are both true and complementary and have various timing relationships to signal AN. These additional signals are the ones actually coupled to transition detector 15 for the purpose of generating signal *ANTX. These additional signals are shown as being coupled to transition detector 15 via a bus 27. Signal ANB is conveniently used for noting the delay incurred in buffering signal AN. The delay caused by buffer 16 is about 5 nanoseconds. The delay between signal AN and ANB via input circuit 19 and buffer 21 is also about 5 nanoseconds. Consequently, the time between time t0 and time t2 is about 10 nanoseconds. The time delay between signal ANB switching logic state and pulse *ANTX being activated is about 2 nanoseconds so that the time between t2 and t3 is 2 nanoseconds. Because of the switch of signal *CS from a logic high to logic low, signal EQ is a logic high when pulse *ANTX becomes active. Signal *CSD is maintained at a logic low for a predetermined time delay following signal *ANB switching to a logic low. Signal *CSD at a logic high causes pulse EQ to be a logic high. Consequently, during the deselect mode pulse EQ is held at a logic high so that the memory array is equilibrated during the deselect mode. For a transition from the deselect to select modes, pulse EQ is held at a logic high long enough to let the circuitry stabilize. The predetermined delay between signal *CSB and signal *CSD is determined by delay circuit 17. The delay is set sufficiently long to avoid pulse EQ switching to a logic low before signal *ANTX, or some other address transition pulse, would cause it to switch to a logic high. Consequently, the switching of pulse *ANTX to a logic low at time t3 does not cause the activation of pulse EQ because pulse EQ is being held at a logic high by signal *CSD. Signal *CSD switches to a logic low at time t4, releasing EQ generator 18 to the control of the address transition pulses, pulses AOTX-ANTX. By the time signal *CSD has released control of EQ generator 18 at time t4, pulse *ANTX has switched to a logic low at time t3, causing pulse EQ to remain at a logic high. Pulse EQ cannot switch to a logic low until, signal *ANTX switches to a logic high at a time t5, about 8 nanoseconds after time t3. Consequently, the elapsed time from t3 to t5 is 20 nanoseconds. Pulse EQ switches to a logic low at a time t6 about 4 nanoseconds after pulse *ANTX switches to a logic high. Valid data follows at a time t7 about 10 nanoseconds after pulse EQ switches to a logic low. Consequently, the access time, the time from t0 to t7 is about 34 nanoseconds for switching from the deselect to select modes. Consequently, the

access time for a chip select transition is about 5 nanoseconds longer than the access time for an address transition. The time from the transition of signal ANB to valid data is the same, about 24 nanoseconds, for both cases. The difference is in the time from t0 to the transition of signal ANB. When an access begins by a transition of signal *CS, buffer 16 causes a 5 nanosecond delay before enabling input circuit 19. The enabling of input circuit 19 causes a transition of signal *ANI which in turn causes pulse *ANTX to be activated in the case in which address signal AN is a logic low. Consequently, even though no address transition has occurred, signal *ANTX is activated. This is known as a false address transition. This occurs for address input circuits which are disabled by a chip select signal during the deselect mode. This false address transition only occurs when the address signal is a logic low. When signal AN is a logic high, signal *ANI will be a logic low even when input circuit is disabled because transistor 24 is conductive. Consequently, the enabling of input circuit 19 does not cause a transition of signal *ANI. Of course it is not knowable in which state the addresses will be. The memory must be prepared to handle this false address transition.

This false address transition problem has manifested itself in one of two ways. The access time is extended by about 5 nanoseconds and is specified as such. The access time for a transition from the deselect to select modes is specified as 5 nanoseconds longer than for an access time caused by an address transition during the select mode. The other manifestation has been simply to not disable the input circuits during the deselect mode. This results in higher current during the deselect mode. The deselect mode is also known as standby. Not disabling the input circuits results in specifying a higher standby current.

Shown in FIG. 5 is a circuit 30 according to a preferred embodiment of the invention. Circuit 30 is for replacing circuit 11 in memory 10. Circuit 30 is comprised generally of input pads 12, 31, 32, 33 and 34, the chip select buffer 16, a plurality of address input buffers 36, a plurality of transition detectors 37, a chip select delay circuit 38, and an EQ generator 39. Plurality of input buffers 36 comprises address input amplifiers 41, 42, 43 and 44. Plurality of transition detectors 37 comprises transition detectors 46, 47, 48 and 49. Chip select delay circuit 38 comprises a delay circuit 51, a NOR gate 52, an inverter 53, an OR gate 54, a NAND gate 55, and an inverter 56. NOR gate 52 has a first input for receiving signal *CSB which is generated in the same way as shown in FIG. 2, a second input, and an output. Delay circuit 51 has an input for receiving signal *CSB and an output connected to the second input of NOR gate 52. Inverter 53

has an input connected to the output of NOR gate 52 and an output for providing a first delayed chip select signal *CSD1. OR gate 54 has a first input connected to the output of delay circuit 51, a second input for receiving signal *CSB, and an output. NAND gate 55 has a first input connected to the output of OR gate 54, a second input connected to the output of inverter 53, and an output. Inverter 56 has an input connected to the output of NAND gate 55, and an output for providing a second delayed chip select signal *CSD2. Input pads 31, 32, 33 and 34 receive address signals A0, A1, A2 and AN, respectively. Address input amplifiers 41, 42, 43 and 44 each have an input for receiving a corresponding address signal and an output for providing a buffered address signal. Amplifiers 41, 42, 43 and 44 receive address signals A0, A1, A2 and AN, respectively, and provide corresponding buffered address signals A0B, A1B, A2B and ANB, respectively, as well as other signals via buses 61, 62, 63 and 64, respectively. Address input amplifiers 41-44 each operate the same as address input amplifier 14 of FIG. 2. Each of transition detectors 46, 47, 48 and 49 receive signals relating to corresponding address signals A0, A1, A2 and AN, respectively, via buses 61, 62, 63 and 64, respectively. Transition detectors 46, 47, 48 and 49 are connected to amplifiers 41, 42, 43 and 44, respectively, via buses 61, 62, 63 and 64, respectively. Transition detectors 46-49 each have a control input for receiving signal *CSD2 by being connected to the output of inverter 56. Transition detectors 46, 47, 48 and 49 each have an output for providing an address transition pulse. Transition detectors 46, 47, 48 and 49 provide pulses *A0TX, *A1TX, *A2TX and *ANTX. Transition detectors 46-49 operate substantially the same as transition detector 15 of FIG. 2 except that when signal *CSD2 is a logic high, transition detectors 46-49 are disabled. EQ generator 39 is connected to the outputs of transition detectors 46-49 and the output of inverter 53 and provides signal EQ. EQ generator 39 is functionally the same as EQ generator 18 of FIG. 2.

During normal operation in the select mode in which signal *CSB is a logic low, circuit 30 operates the same as circuit 11 of FIG. 2. An address transition causes pulse EQ and subsequent valid data with the same chain reaction as shown in the timing diagram of FIG. 3. With signal *CSB at a logic low, signals *CSD1 and *CSD2 will also be a logic low. With signal *CSD2 at a logic low, transition detectors 46-49 are enabled so that they will respond to an address transition by activating the corresponding address transition pulse A0TX-ANTX. With signal *CSD at a logic low, EQ generator 39 will respond to an activated address transition pulse A0TX-ANTX by activating pulse EQ.

The improvement over circuit 11 of FIG. 2 is for the case in which a data access is initiated by a transition from the deselect to select modes. Prior to such transition, signal *CSB is a logic high which disables amplifiers 41-44 and causes signals *CSD1 and *CSD2 to be a logic high. With signal *CSD2 a logic high, transition detectors 46-49 are disabled. Pulse EQ is active due to signal *CSD1 being a logic high. When signal *CSB switches to a logic low to cause the switch from the deselect mode to the select mode, amplifiers 41-44 are enabled, causing signals A0B-ANB to assume the logic state of corresponding address signals A0-AN. For the address signals A0-AN which were a logic low at the time of the mode transition, the corresponding buffered address signals will undergo a logic high to logic low transition.

Shown in FIG. 6 is a timing diagram for the case in which signal AN is a logic low when signal *CS switches from a logic high to a logic low at a time t0. Signal *CS switching to a logic low causes signal *CSB to switch to a logic low at a time t1 which in turn causes the false transition of signal ANB which switches to a logic low at a time t2. An elapsed time for t0 to t2 in FIG. 6 is the same as that shown in FIG. 4, about 10 nanoseconds. Signal *ANTX, however, is not generated because signal *CSD2 is kept at a logic high sufficiently long to ensure that the false transitions have ceased. Signal *CSD2 will remain at a logic high until both inputs of OR gate 54 are a logic low or until signal *CSD1 switches to a logic low. Both signal *CSD1 and *CSD2 are held to a logic high by delay circuit 51 for a predetermined time delay following signal *CSB switching to a logic low. When signal *CSB switches to a logic low, delay circuit 51 does not output a logic low until the predetermined delay time has elapsed. With NOR gate 52 receiving a logic high for the predetermined delay time, signal *CSD1 will be held at a logic high as well. With the output of delay circuit 51 and signal *CSD1 both at a logic high, signal *CSD2 is also held at a logic high. When the predetermined delay time has elapsed, the output of delay circuit 51 switches to a logic low, causing signals *CSD1 and *CSD2 to switch to a logic low at virtually the same time. In order for access time to be the same for a chip select transition as for an address transition, the time from the chip select transition to signals *CSD1 and *CSD2 switching to a logic low should be the same as the time from the address transition to the termination of the address transition pulse. In terms of the timing diagrams this means that the time from t0 to t4 in FIG. 3 should equal the time from t0 to t3 in FIG. 6. This is achieved by so selecting *CSD1. Alternatively, the delay time for *CSD1 can be reduced so that a chip select transition access can occur faster than an address

transition access.

One delayed chip select signal could be used to both suppress the transition detectors and to generate the equalization pulse for the desired time delay following the chip select transition. This function was achieved in circuit 30 with signals *CSD1 and *CSD2 to provide a margin of safety. Signal *CSD2, which suppresses transition detectors 46-49, will not be generated unless both signal *CSB and signal *CSD1 are a logic high. This guards against the situation in which signal *CSB is a logic high for only a very short time but causes transition detectors to miss an address transition but does not cause the EQ pulse to be active sufficiently long. Circuit 30 causes pulse EQ to be generated by signal *CSD1 switching to a logic high which occurs before signal *CSD2 can suppress transition detectors 46-49. Measures are thus taken to provide sufficient time for pulse EQ to be active for sufficiently long. With two delayed chip select signals, there is also the opportunity to continue to suppress *ANTX after initiating the termination of pulse EQ by terminating *CSD1 before terminating *CSD2.

Shown in FIG. 7 is a more detailed drawing of input amplifier 44, transition detector 49, and bus 64. Transition detector 49 comprises transistors 66, 67, 68, 69, 70, 71, 72, 73, inverter 74, and NOR gate 75. Input amplifier 44 comprises an input circuit 77, a buffer circuit 78, and inverters 79, 80, 81, 82, 83 and 84. Bus 64 is simply the connections between amplifier 44 and transition detector 49. Transition detector 49 uses true and complementary fast address signal ANF and *ANF and true and complementary slow address signals ANS and *ANS in conventional fashion to generate pulse *ANTX in response to a transition of signal AN, except that NOR gate 75 would normally be an inverter and would not receive signal *CSD2. When signal *CSD2 is a logic high NOR gate 75 is forced to provide signal ANS at a logic low. A false address transition occurs when signal AN is a logic low during the transition from the deselect to select modes. This false transition imitates the affect of a logic high to logic low address transition. A logic high to logic low address transition results in an occurrence of pulse *ANTX by virtue of signal *ANF switching to a logic high before signal ANS switches to a logic low. Signal *CSD2 at a logic high forces signal ANS to a logic low, effectively suppressing the detection of a logic high to logic low address transition which is the only false address transition. There is no need to suppress the detection of a logic low to logic high address transition because there is no false address transition that imitates a logic low to logic high transition. Accordingly, inverter 74 need not be converted to a NOR gate. Consequently, a conventional transition detec-

tor need only have an inverter changed to a NOR gate to respond to the control provided by circuit 38 of FIG. 5. The input of NOR gate 75 which receives signal *CSD2 thus provides transition detector 49 the capability of being controllably suppressed.

Claims

1. A memory circuit (30) which is enabled in response to an occurrence of a chip select signal (CS), comprising:
 - a plurality of address input means (36), each for receiving a address signal and being enabled in response to a occurrence of the chip select signal;
 - transition detection means (37), coupled to the output of the plurality of address input means, for detecting a transition of an address signal; said memory circuit being characterised by:
 - disabling means (38, 51, 52, 53, 54, 55, 56) for disabling the transition detection means for a predetermined time delay following a occurrence of the chip select signal.
2. A memory circuit according to claim 1 which is enabled in response to the chip select signal (CS) switching from a first logic state to a second logic state,
 - wherein the plurality of address input means are enabled by the second logic state of the chip select signal and disabled by the first logic state of the chip select signal, each address input means (41, 42, 43, 44) providing a output signal representative of the received address signal when enabled by the chip select signal, and providing the output signal in a predetermined state when disabled by the chip select signal,
 - wherein said transition detection means comprises a plurality of transition detection means (46, 47, 48, 49) each coupled to a corresponding address input means (41, 42, 43, 44) for detecting a transition of the output signal of the corresponding address input means; and
 - wherein the disabling means (38) disables all of the plurality of transition detection means for the predetermined time delay following the chip select signal switching from the first logic state to the second logic state.
3. The memory circuit of claim 2 wherein each enabled transition detector means (46, 47, 48, 49) provides a output pulse in response to detecting an address transition of the output signal of the corresponding address input

transition access.

One delayed chip select signal could be used to both suppress the transition detectors and to generate the equalization pulse for the desired time delay following the chip select transition. This function was achieved in circuit 30 with signals *CSD1 and *CSD2 to provide a margin of safety. Signal *CSD2, which suppresses transition detectors 46-49, will not be generated unless both signal *CSB and signal *CSD1 are a logic high. This guards against the situation in which signal *CSB is a logic high for only a very short time but causes transition detectors to miss an address transition but does not cause the EQ pulse to be active sufficiently long. Circuit 30 causes pulse EQ to be generated by signal *CSD1 switching to a logic high which occurs before signal *CSD2 can suppress transition detectors 46-49. Measures are thus taken to provide sufficient time for pulse EQ to be active for sufficiently long. With two delayed chip select signals, there is also the opportunity to continue to suppress *ANTX after initiating the termination of pulse EQ by terminating *CSD1 before terminating *CSD2.

Shown in FIG. 7 is a more detailed drawing of input amplifier 44, transition detector 49, and bus 64. Transition detector 49 comprises transistors 66, 67, 68, 69, 70, 71, 72, 73, inverter 74, and NOR gate 75. Input amplifier 44 comprises an input circuit 77, a buffer circuit 78, and inverters 79, 80, 81, 82, 83 and 84. Bus 64 is simply the connections between amplifier 44 and transition detector 49. Transition detector 49 uses true and complementary fast address signal ANF and *ANF and true and complementary slow address signals ANS and *ANS in conventional fashion to generate pulse *ANTX in response to a transition of signal AN, except that NOR gate 75 would normally be an inverter and would not receive signal *CSD2. When signal *CSD2 is a logic high NOR gate 75 is forced to provide signal ANS at a logic low. A false address transition occurs when signal AN is a logic low during the transition from the deselect to select modes. This false transition imitates the affect of a logic high to logic low address transition. A logic high to logic low address transition results in an occurrence of pulse *ANTX by virtue of signal *ANF switching to a logic high before signal ANS switches to a logic low. Signal *CSD2 at a logic high forces signal ANS to a logic low, effectively suppressing the detection of a logic high to logic low address transition which is the only false address transition. There is no need to suppress the detection of a logic low to logic high address transition because there is no false address transition that imitates a logic low to logic high transition. Accordingly, inverter 74 need not be converted to a NOR gate. Consequently, a conventional transition detec-

tor need only have an inverter changed to a NOR gate to respond to the control provided by circuit 38 of FIG. 5. The input of NOR gate 75 which receives signal *CSD2 thus provides transition detector 49 the capability of being controllably suppressed.

Claims

1. A memory circuit (30) which is enabled in response to an occurrence of a chip select signal (CS), comprising:
 - a plurality of address input means (36), each for receiving a address signal and being enabled in response to a occurrence of the chip select signal;
 - transition detection means (37), coupled to the output of the plurality of address input means, for detecting a transition of an address signal; said memory circuit being characterised by:
 - disabling means (38, 51, 52, 53, 54, 55, 56) for disabling the transition detection means for a predetermined time delay following a occurrence of the chip select signal.
2. A memory circuit according to claim 1 which is enabled in response to the chip select signal (CS) switching from a first logic state to a second logic state,
 - wherein the plurality of address input means are enabled by the second logic state of the chip select signal and disabled by the first logic state of the chip select signal, each address input means (41, 42, 43, 44) providing a output signal representative of the received address signal when enabled by the chip select signal, and providing the output signal in a predetermined state when disabled by the chip select signal,
 - wherein said transition detection means comprises a plurality of transition detection means (46, 47, 48, 49) each coupled to a corresponding address input means (41, 42, 43, 44) for detecting a transition of the output signal of the corresponding address input means; and
 - wherein the disabling means (38) disables all of the plurality of transition detection means for the predetermined time delay following the chip select signal switching from the first logic state to the second logic state.
3. The memory circuit of claim 2 wherein each enabled transition detector means (46, 47, 48, 49) provides a output pulse in response to detecting an address transition of the output signal of the corresponding address input



means (41, 42, 43, 44).

4. The memory circuit of claim 3 further comprising an equalisation pulse generator means (39), coupled to the plurality of transition detection means (37), for generating a equalisation pulse (EQ) in response to receiving a output pulse.
5. The memory circuit of claim 4 wherein the disabling means provides a delayed chip select signal (CSD) when the chip select signal disables the memory circuit.
6. The memory circuit of claim 5 wherein the equalisation pulse generator provides the equalisation pulse when the delayed chip select signal is present.
7. A method of enabling a memory circuit in response to an occurrence of a chip select signal (CS), the memory circuit comprising:
 - Input means (36) for receiving an address signal;
 - transition detection means (37) coupled to the output of the input means; and
 - an equalisation pulse generator means (39) coupled to the transition detection means, said method comprising the steps of:
 - providing a output signal at the output of the input means in response to the received address signal when enabled by an occurrence of the chip select signal, and providing the output at a predetermined state when disabled by the chip select signal;
 - detecting a transition of the address signal;
 - generating an equalisation pulse (EQ) in response to the detection of a transition of the address signal, the method being characterised by the steps of:
 - preventing the transition detection means from detecting a transition of the address signal for at least a predetermined time delay following a occurrence of the chip select signal.
8. The method of claim 7 further comprising the steps of:
 - providing the equalisation pulse for at least the predetermined time delay following the occurrence of the chip select signal.
9. The method of claim 8 further comprising the steps of:
 - terminating the equalisation pulse in response to the termination of a first delay signal (CSD1); and
 - terminating the prevention of detecting a

transition of the address signal in response to the termination of a second delay signal (CSD2).

10. The method of claim 9 wherein the first delay signal is terminated prior to the termination of the second delay signal.

Patentansprüche

1. Speicherschaltkreis (30), der bei Auftreten eines Chipauswahlsignals (CS) freigegeben wird, mit:
 - einer Mehrzahl von Adreßeingangsgliedern (36), die jeweils ausgebildet sind, ein Adreßsignal zu empfangen und bei Auftreten des Chipauswahlsignals freigegeben zu werden;
 - einer mit dem Ausgang der Mehrzahl von Adreßeingangsgliedern verbundenen Übergangserfassungseinrichtung (37) zum Erfassen eines Übergangs eines Adreßsignals;
 - gekennzeichnet durch:
 - eine Sperreinrichtung (38, 51, 52, 53, 54, 55, 56) zum Sperren der Übergangserfassungseinrichtung (37) für eine vorgegebene Zeitspanne im Anschluß an ein Auftreten des Chipauswahlsignals.
2. Speicherschaltkreis nach Anspruch 1, der freigegeben wird, sobald das Chipauswahlsignal (CS) von einem ersten logischen Zustand in einen Zweiten logischen Zustand wechselt, wobei
 - die Mehrzahl von Adreßeingangsgliedern durch den zweiten logischen Zustand des Chipauswahlsignals freigegeben und durch den ersten logischen Zustand des Chipauswahlsignals gesperrt werden und jedes Adreßeingangsglied (41, 42, 43, 44) bei Freigabe durch das Chipauswahlsignal ein das empfangene Adreßsignal repräsentierendes Ausgangssignal liefert und bei Sperrung durch das Chipauswahlsignal das Ausgangssignal in einem vorbestimmten Zustand ausgibt;
 - die Übergangserfassungseinrichtung eine Mehrzahl von Übergangserfassungseinrichtungen (46, 47, 48, 49) umfaßt, von denen jede mit einem zugeordneten Adreßeingangsglied (41, 42, 43, 44) verbunden ist und ausgebildet ist, einen Übergang des Ausgangssignals des zugeordneten Adreßeingangsglieds zu erfassen; und
 - die Sperreinrichtung (38) die Mehrzahl von Übergangserfassungseinrichtungen für die vorgegebene Verzögerungszeit alle sperrt, sobald das Chipauswahlsignal vom ersten in den zweiten logischen Zustand wechselt.



3. Speicherschaltkreis nach Anspruch 2, bei dem jede freigegebene Übergangserfassungseinrichtung (46, 47, 48, 49) einen Ausgangsimpuls liefert, wenn sie einen Adreßübergang des Ausgangssignals, des zugeordneten Adreßeingangsglieds (41, 42, 43, 44) erfaßt. 5
4. Speicherschaltkreis nach Anspruch 3, ferner mit einem mit der Mehrzahl von Übergangserfassungseinrichtungen (37) verbundenen Abgleichimpulsgenerator (39) zum Erzeugen eines Abgleichimpulses (EQ) bei Empfang eines Ausgangsimpulses. 10
5. Speicherschaltkreis nach Anspruch 4, bei dem die Sperreinrichtung ein verzögertes Chipauswahlsignal (CSD) liefert, wenn das Chipauswahlsignal den Speicherschaltkreis sperrt. 15
6. Speicherschaltkreis nach Anspruch 5, bei dem der Abgleichimpulsgenerator den Abgleichimpuls liefert, wenn das verzögerte Chipauswahlsignal vorliegt. 20
7. Verfahren zum Freigeben eines Speicherschaltkreises bei Auftreten eines Chipauswahlsignals (CS), wobei der Speicherschaltkreis folgende Merkmale aufweist: 25
 - ein Eingangsglied (36) zum Empfangen eines Adreßsignals;
 - eine mit dem Ausgang des Eingangsglieds verbundene Übergangserfassungseinrichtung (37); und
 - einen mit der Übergangserfassungseinrichtung verbundenen Abgleichimpulsgenerator (39); 30
 - und wobei das Verfahren folgende Schritte umfaßt:
 - Ausgeben eines Ausgangssignals am Ausgang des Eingangsglieds bei Empfang des Adreßsignals, wenn das Eingangsglied durch ein Auftreten des Chipauswahlsignals freigegeben ist, und Ausgeben des Ausgangssignals in einem vorbestimmten Zustand, wenn das Eingangsglied durch das Chipauswahlsignal gesperrt ist; 35
 - Erfassen eines Übergangs des Adreßsignals;
 - Erzeugen eines Abgleichimpulses (EQ) bei Erfassung eines Übergangs des Adreßsignals; 40
 - gekennzeichnet durch die Verfahrensschritte, daß die Übergangserfassungseinrichtung im Anschluß an ein Auftreten des Chipauswahlsignals zumindest für eine vorgegebene Zeitspanne daran gehindert wird, einen Übergang des Adreßsignals zu erfassen. 45
8. Verfahren nach Anspruch 7, mit den weiteren 55

Schritten, daß der Abgleichimpuls im Anschluß an das Auftreten des Chipauswahlsignals zumindest für die vorgegebene Zeitspanne bereitgestellt wird.

9. Verfahren nach Anspruch 8, mit den weiteren Schritten, daß
 - der Abgleichimpuls bei Beendigung eines ersten Verzögerungssignals (CSD1) beendet wird; und
 - das Verhindern der Erfassung eines Adreßsignalübergangs bei Beendigung eines zweiten Verzögerungssignals (CSD2) beendet wird.
10. Verfahren nach Anspruch 9, wobei das erste Verzögerungssignal vor Beendigung des zweiten Verzögerungssignals beendet wird.

Revendications

1. Circuit de mémoire (30) qui est validé en réponse à l'apparition d'un signal de sélection de puce (CS), comprenant:
 - une pluralité de moyens d'entrée d'adresse (36), chacun étant destiné à recevoir un signal d'adresse et étant validé en réponse à l'apparition du signal de sélection de puce;
 - un moyen de détection de transition (37), couplé à la sortie de la pluralité des moyens d'entrée d'adresse, pour détecter une transition d'un signal d'adresse; ledit circuit de mémoire étant caractérisé par:
 - un moyen d'invalidation (38,51,52,53,54,55,56) pour invalider le moyen de détection de transition pendant un temps de retard prédéterminé suivant l'apparition du signal de sélection de puce.
2. Circuit de mémoire selon la revendication 1 qui est validé en réponse au signal de sélection de puce (CS) passant d'un premier état logique à un second état logique,
 - dans lequel la pluralité des moyens d'entrée d'adresse sont validés par le second état logique du signal de sélection de puce et invalidés par le premier état logique du signal de sélection de puce, chaque moyen d'entrée d'adresse (41,42,43,44) fournissant un signal de sortie représentant le signal d'adresse reçu quand il est validé par le signal de sélection de puce, et fournissant le signal de sortie dans un état prédéterminé quand il est invalidé par le signal de sélection de puce,
 - dans lequel ledit moyen de détection de transition comprend une pluralité de moyens détecteurs de transition (46,47,48,49) couplés chacun à un moyen d'entrée d'adresse corres-



pendant (41,42,43,44) pour détecter une transition du signal de sortie du moyen d'entrée d'adresse correspondant; et

dans lequel le moyen d'invalidation (38) invalide l'ensemble de la pluralité des moyens détecteurs de transition pendant le temps de retard prédéterminé suivant le passage du signal de sélection de puce du premier état logique au second état logique.

3. Circuit de mémoire selon la revendication 2, dans lequel chaque moyen détecteur de transition validé (46,47,48,49) fournit une impulsion de sortie en réponse à la détection d'une transition d'adresse du signal de sortie du moyen d'entrée d'adresse correspondant (41, 42,43,44).

4. Circuit de mémoire selon la revendication 3, comprenant en outre un moyen générateur d'impulsions d'égalsation (39), couplé à la pluralité des moyens détecteurs de transition (37), pour générer une impulsion d'égalsation (EQ) en réponse à la réception d'une impulsion de sortie.

5. Circuit de mémoire selon la revendication 4, dans lequel le moyen d'invalidation fournit un signal de sélection de puce retardé (CSD) quand le signal de sélection de puce invalide le circuit de mémoire.

6. Circuit de mémoire selon la revendication 5, dans lequel le générateur d'impulsions d'égalsation fournit l'impulsion d'égalsation quand le signal de sélection de puce retardé est présent.

7. Procédé pour valider un circuit de mémoire en réponse à l'apparition d'un signal de sélection de puce (CS), le circuit de mémoire comprenant:

un moyen d'entrée (36) pour recevoir un signal d'adresse;

un moyen de détection de transition (37) couplé à la sortie du moyen d'entrée; et

un moyen générateur d'impulsions d'égalsation (39) couplé au moyen de détection de transition, ledit procédé comprenant les étapes qui consistent à:

fournir un signal de sortie à la sortie du moyen d'entrée en réponse au signal d'adresse reçu quand il est validé par l'apparition du signal de sélection de puce, et fournir le signal de sortie à un état prédéterminé quand il est invalidé par le signal de sélection de puce;

détecter une transition du signal d'adresse; générer une impulsion d'égalsation (EQ)

en réponse à la détection d'une transition du signal d'adresse, le procédé étant caractérisé par l'étape qui consiste à:

empêcher que le moyen de détection de transition détecte une transition du signal d'adresse pendant au moins un temps de retard prédéterminé suivant l'apparition du signal de sélection de puce.

8. Procédé selon la revendication 7, comprenant en outre l'étape qui consiste à:

fournir l'impulsion d'égalsation pendant au moins le temps de retard prédéterminé suivant l'apparition du signal de sélection de puce.

9. Procédé selon la revendication 8, comprenant en outre les étapes qui consistent à:

terminer l'impulsion d'égalsation en réponse à la fin d'un premier signal retardé (CSD1); et à

terminer l'interdiction de détecter une transition du signal d'adresse en réponse à la fin d'un second signal retardé (CSD2).

10. Procédé selon la revendication 9, dans lequel le premier signal retardé est terminé avant la fin du second signal retardé.

