

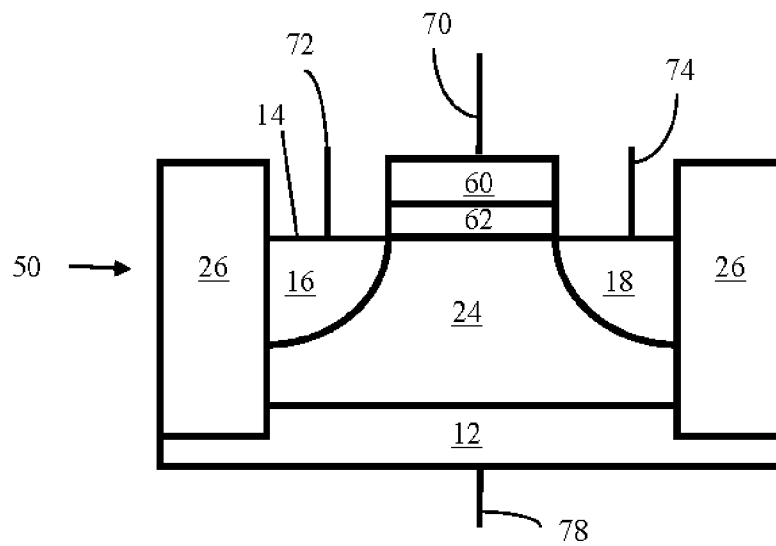


FIG. 1

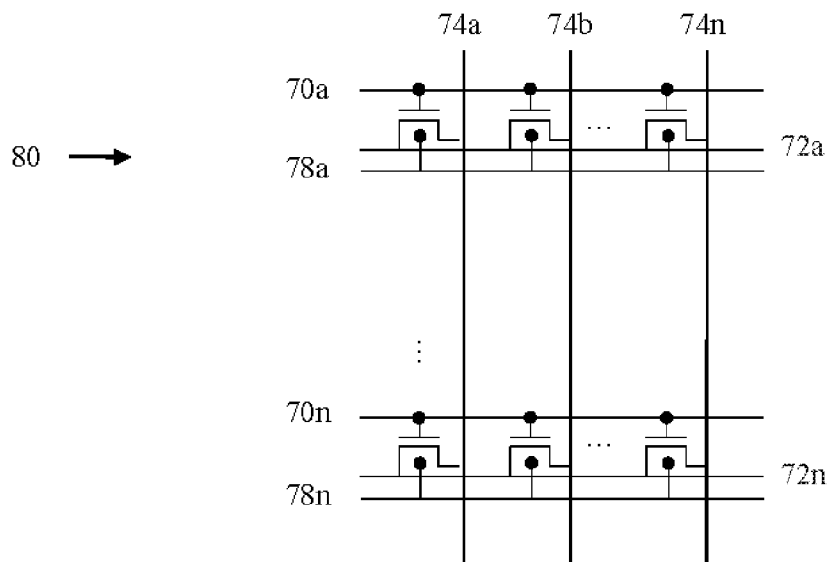


FIG. 2

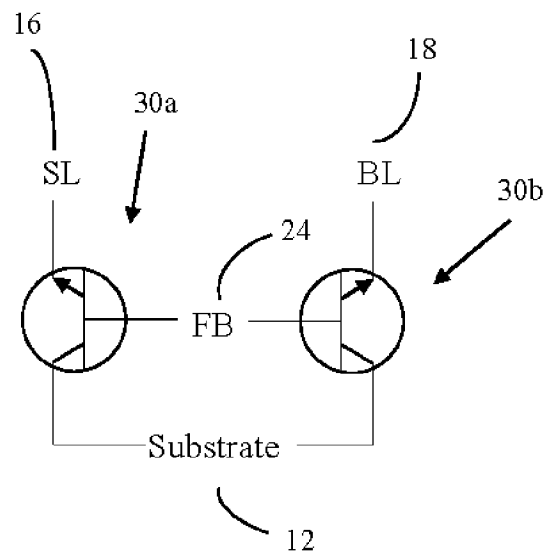


FIG. 3

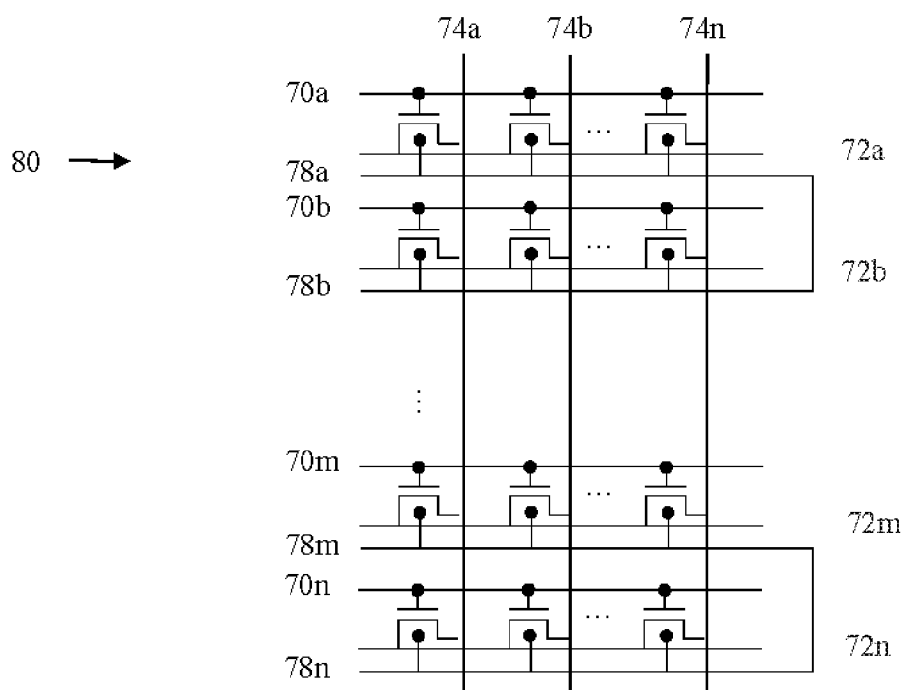


FIG. 4A

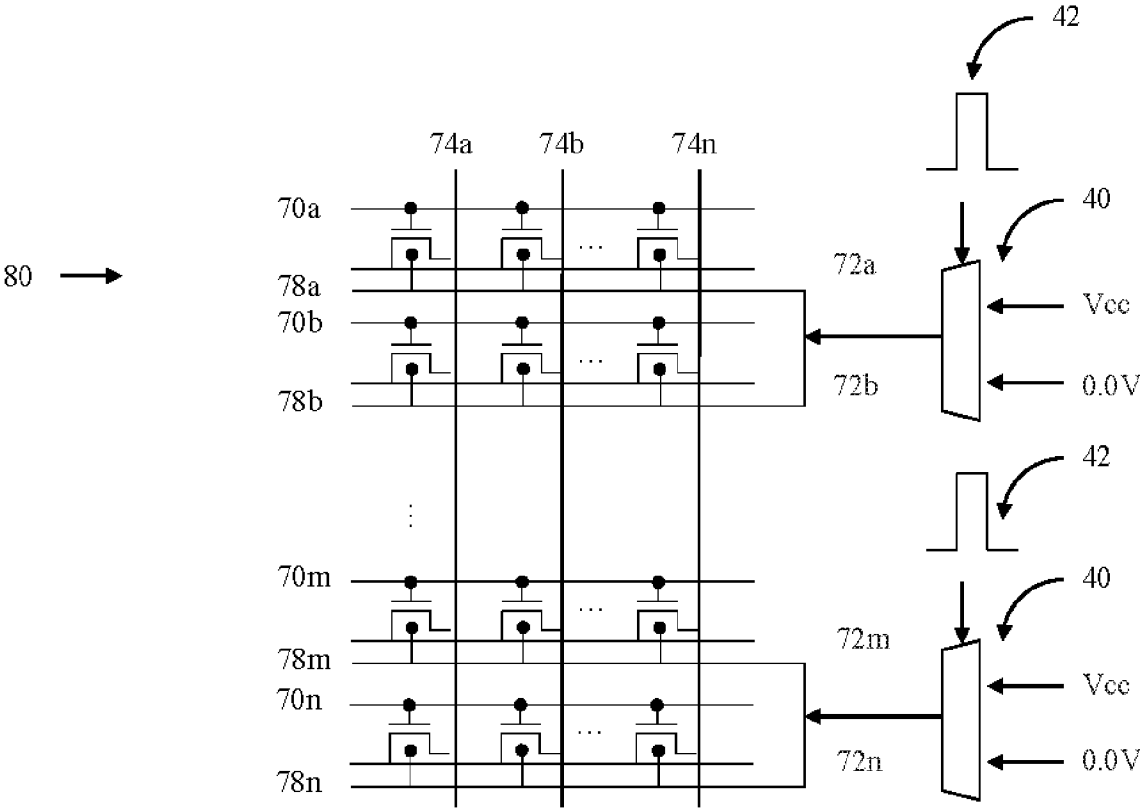


FIG. 4B

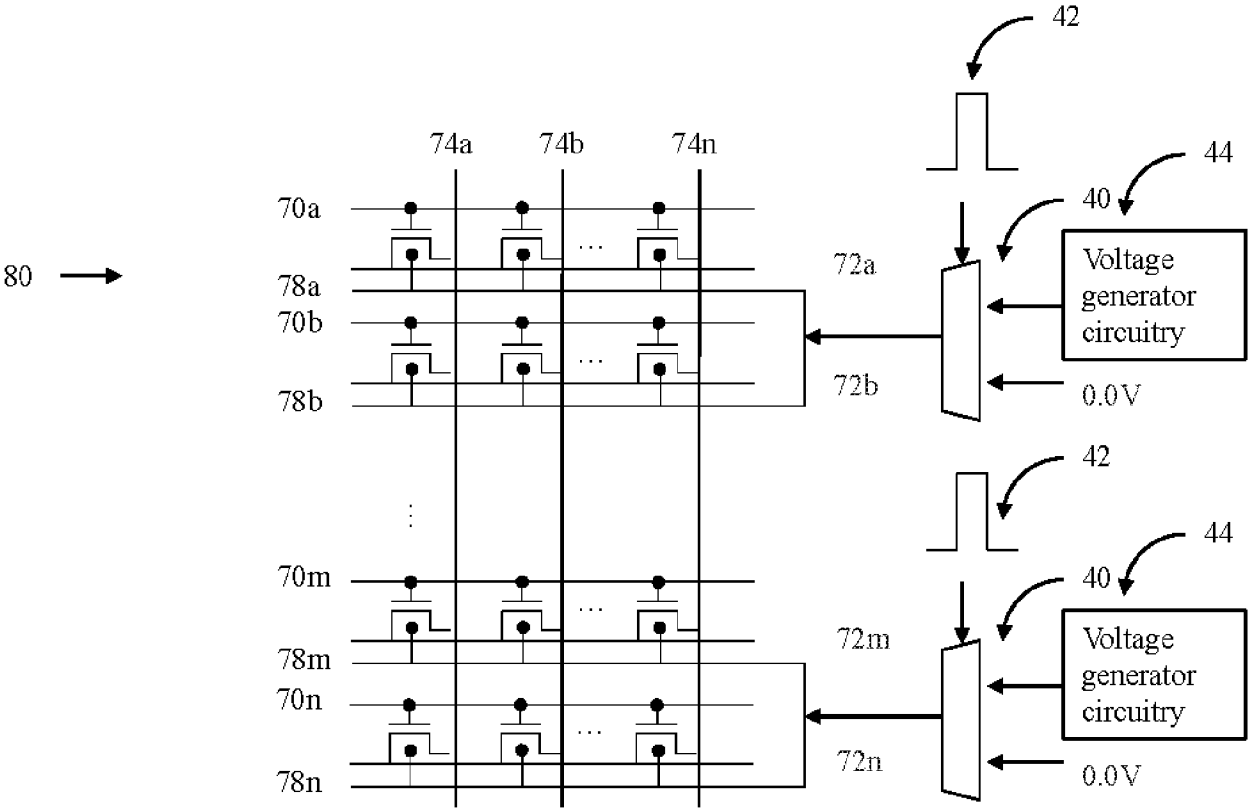


FIG. 4C

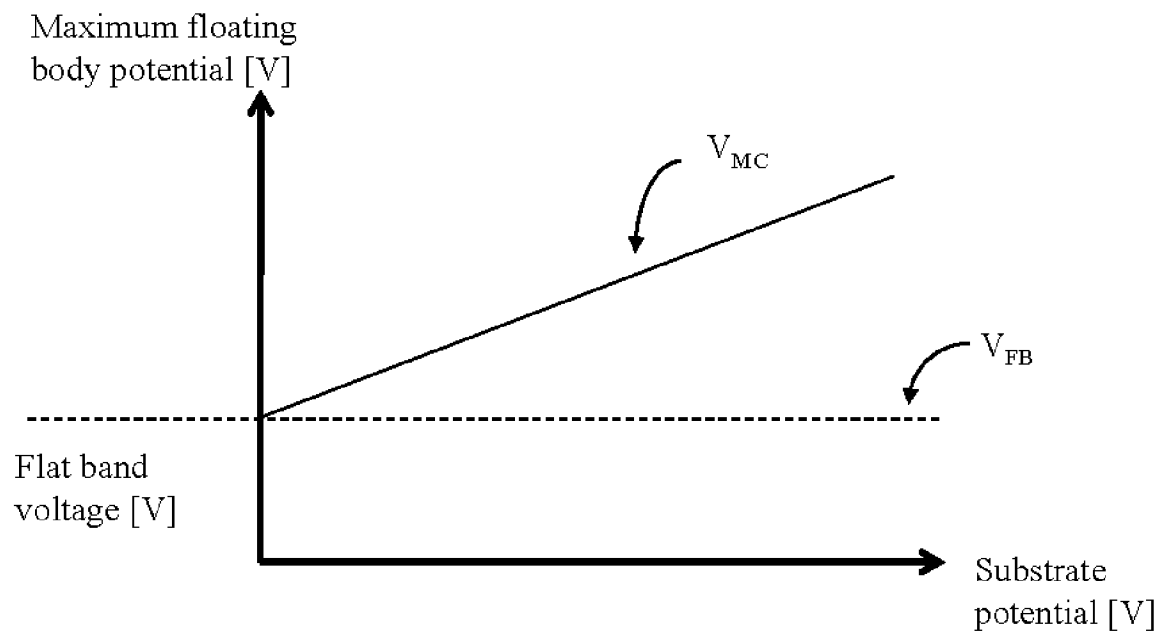


FIG. 5

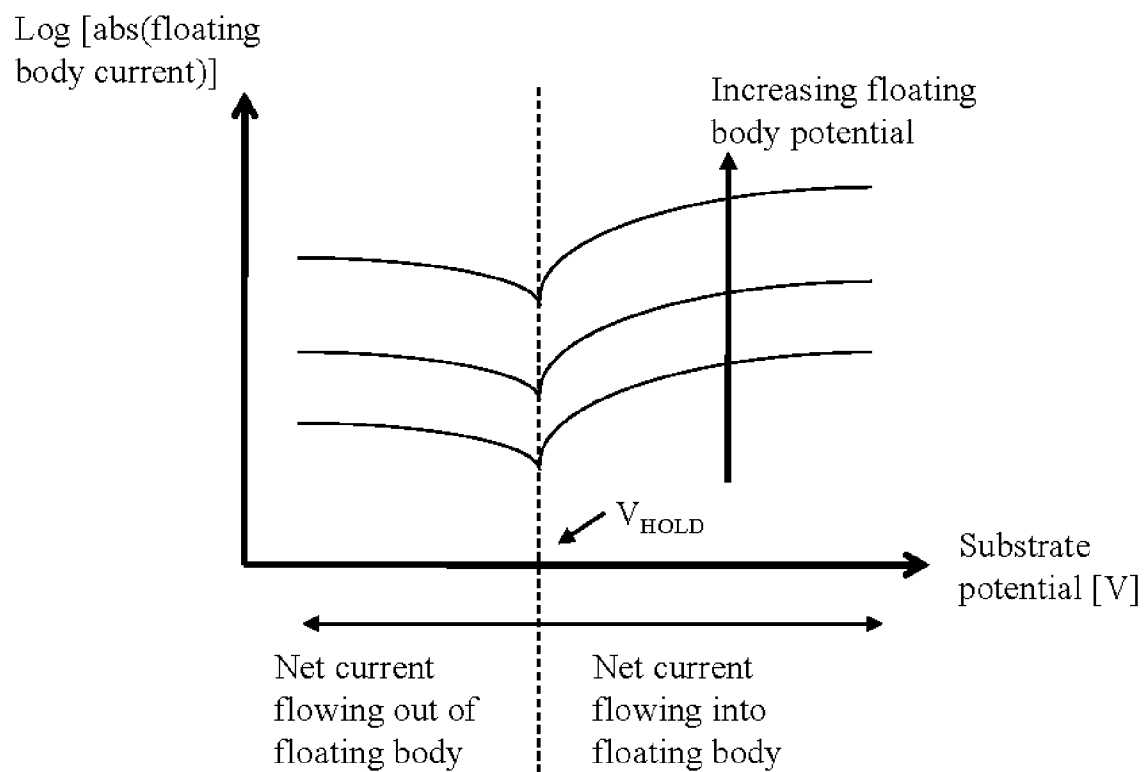


FIG. 6A

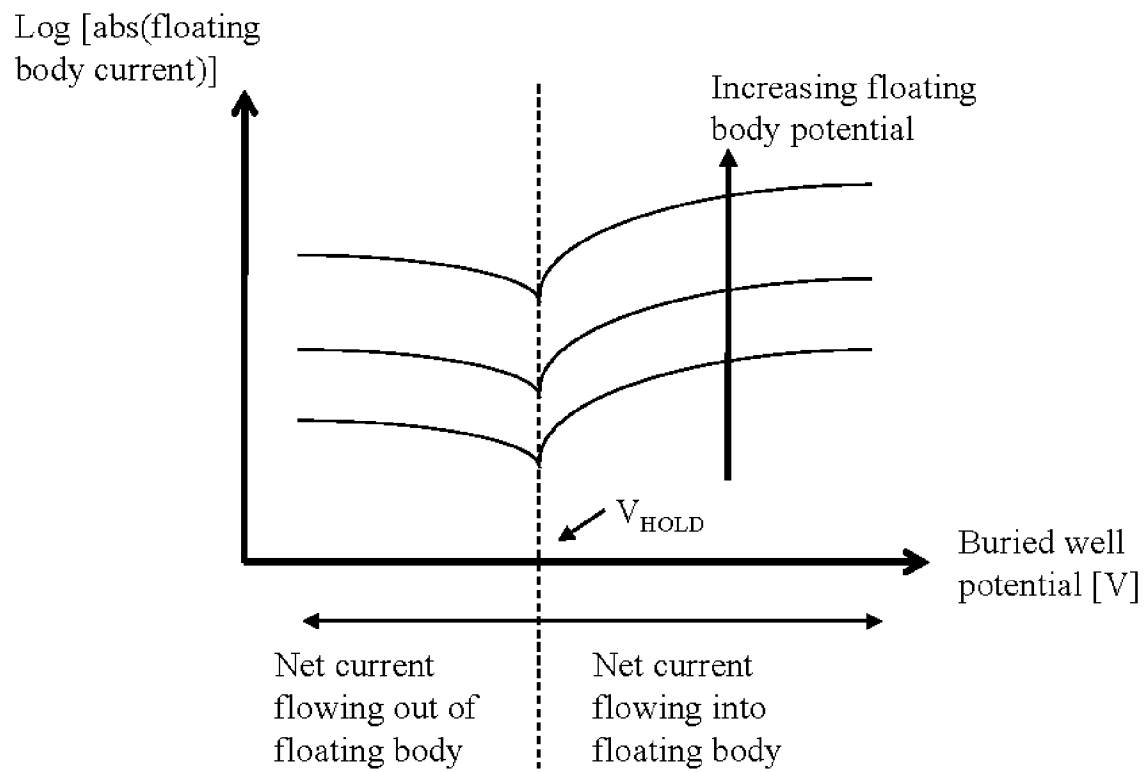


FIG. 6B

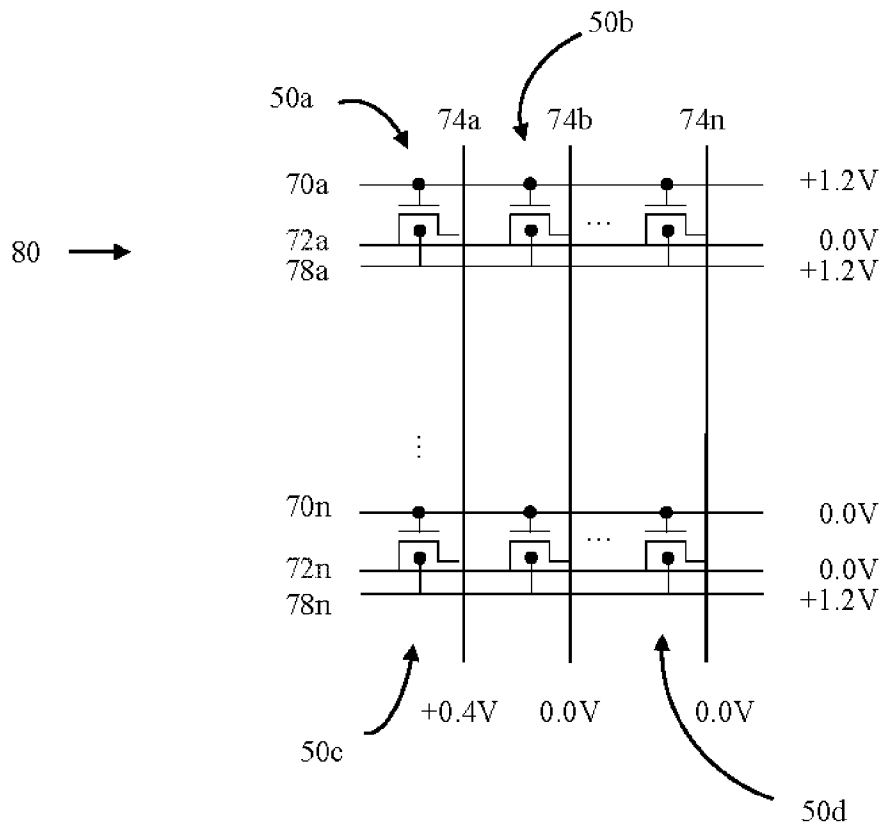


FIG. 7

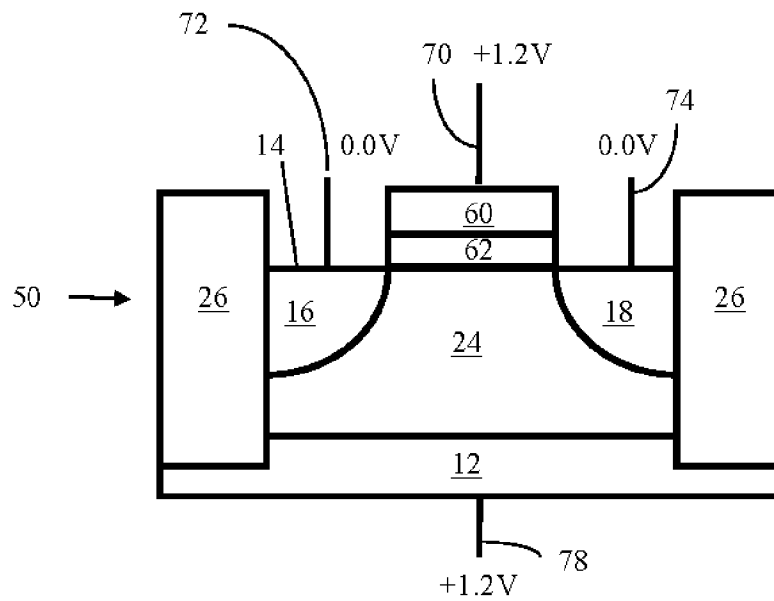


FIG. 8A

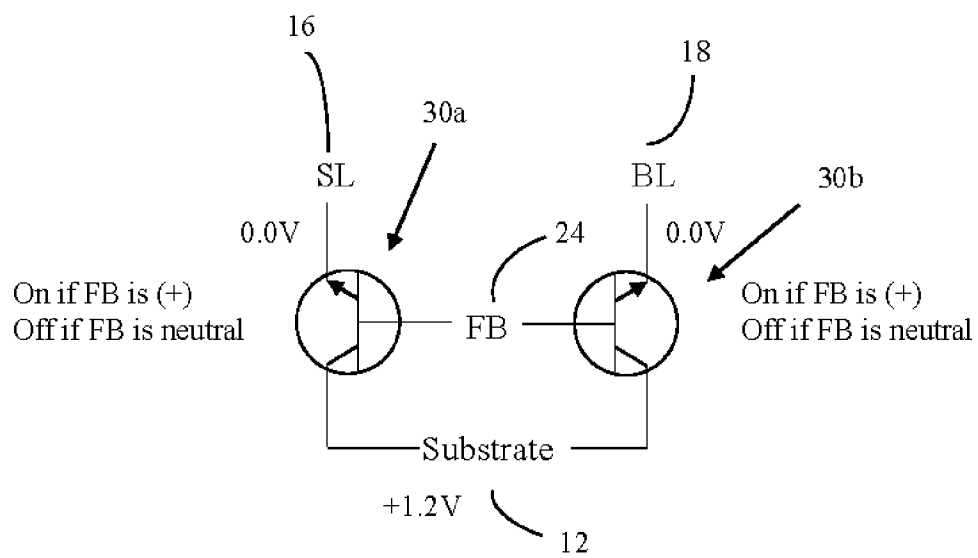


FIG. 8B

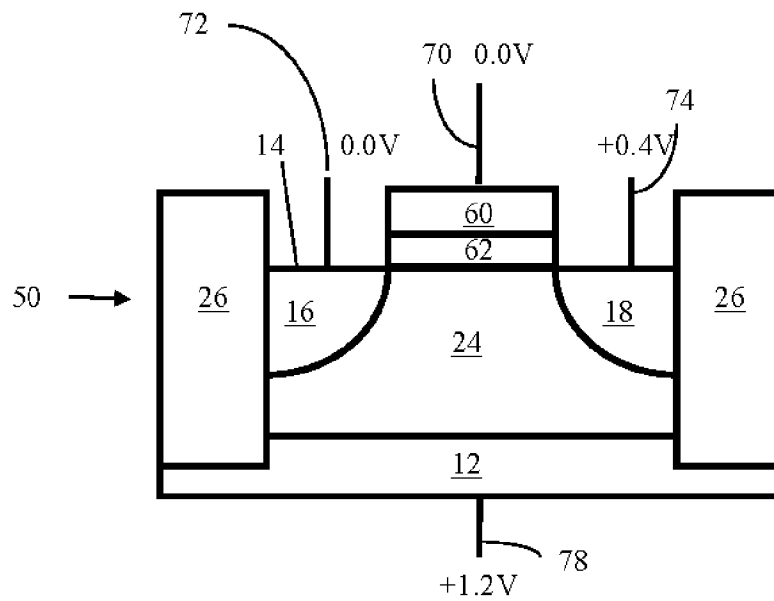


FIG. 8C

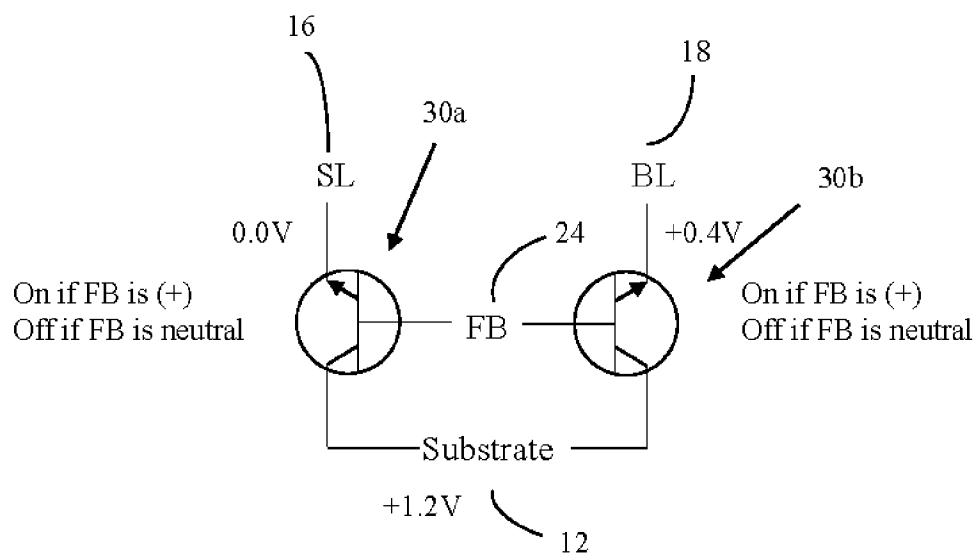
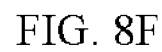
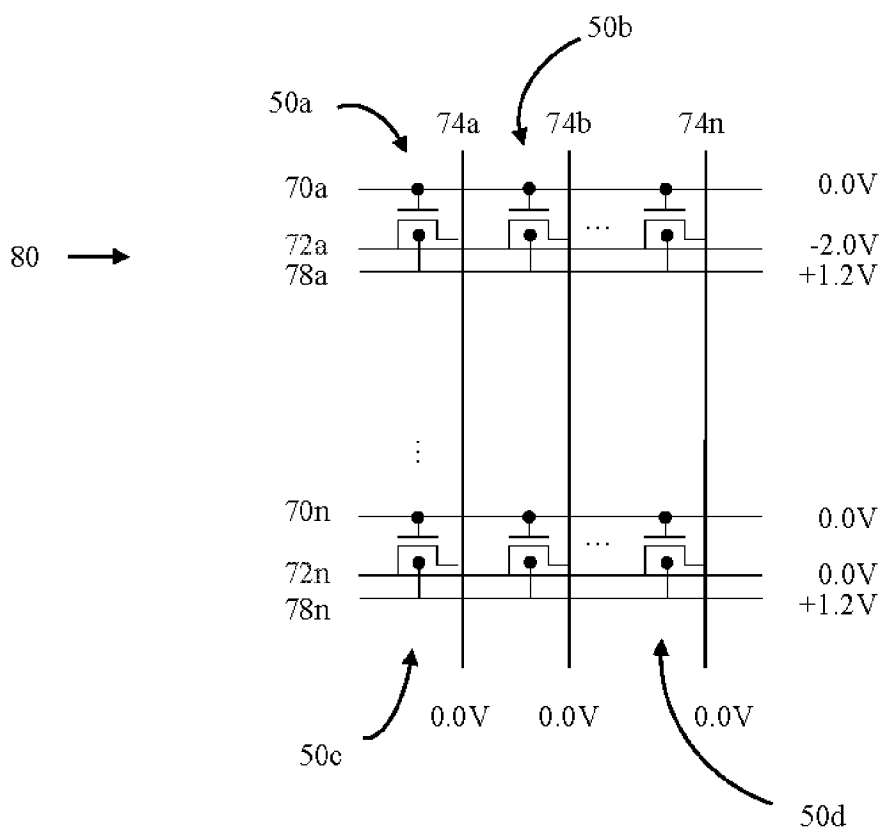


FIG. 8D





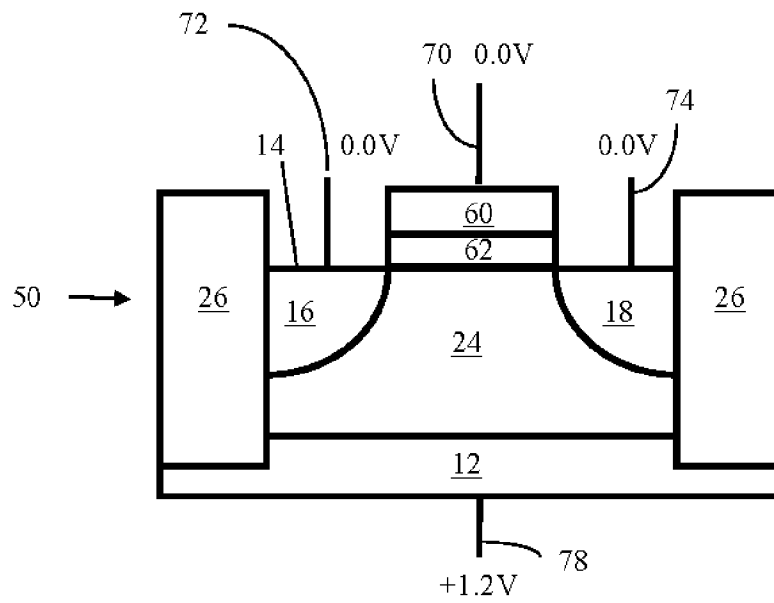


FIG. 11A

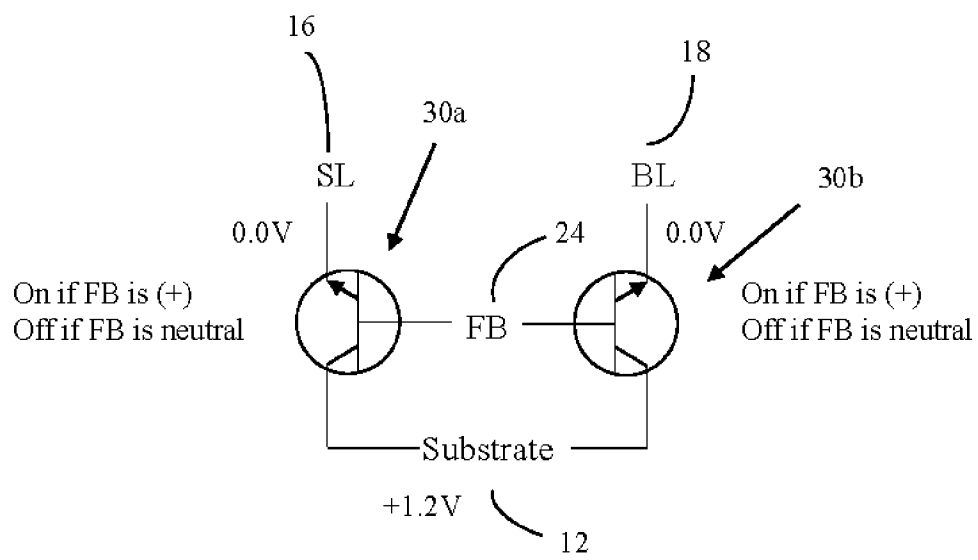


FIG. 11B

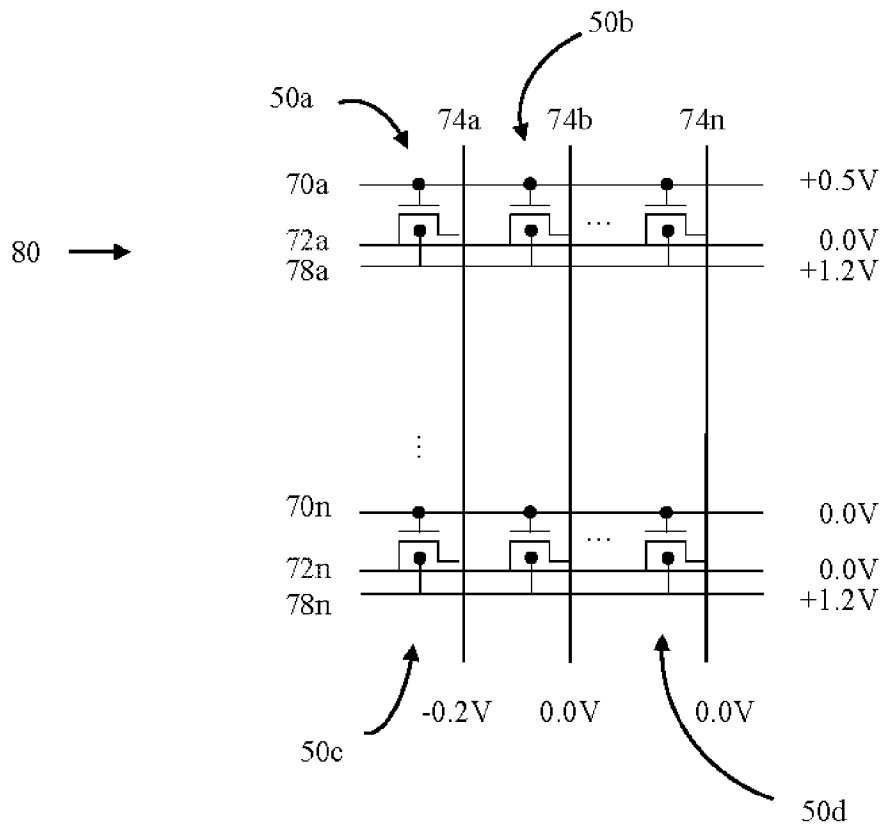


FIG. 12

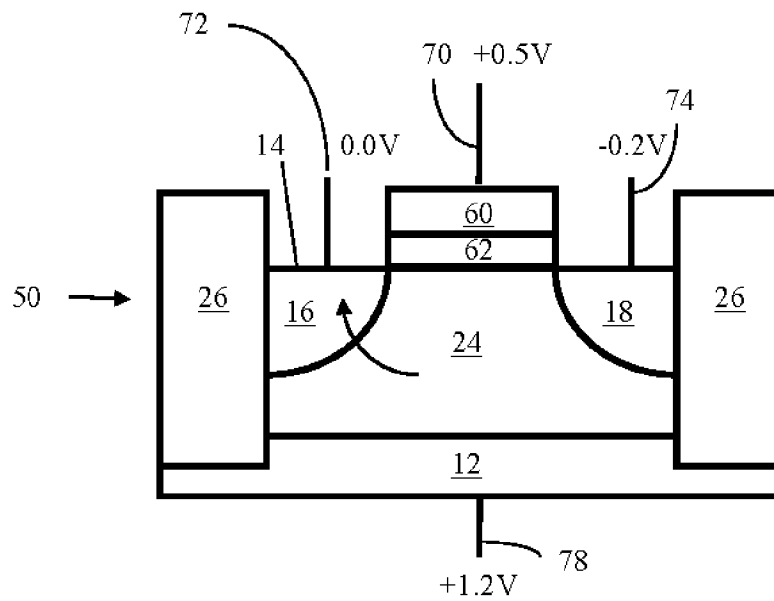


FIG. 13A

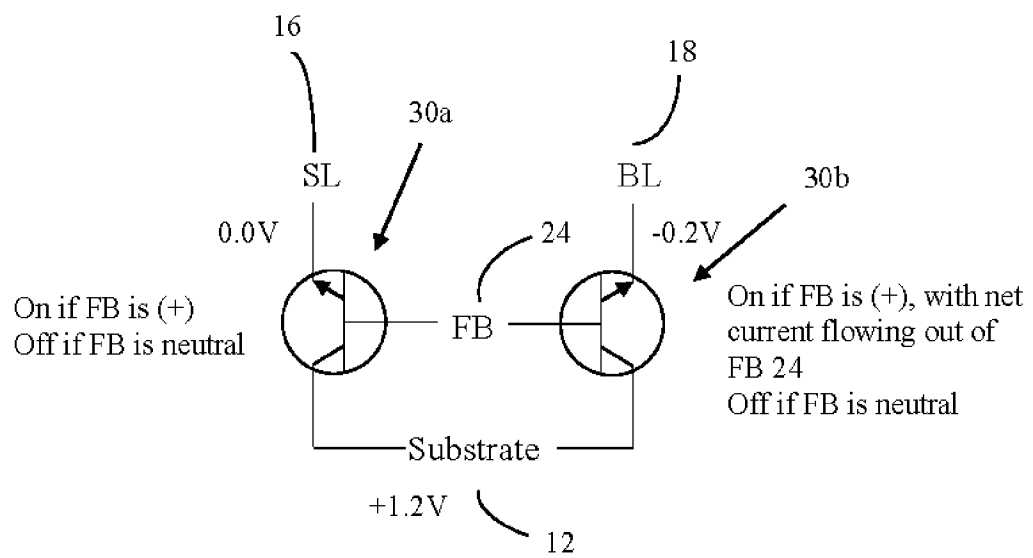


FIG. 13B

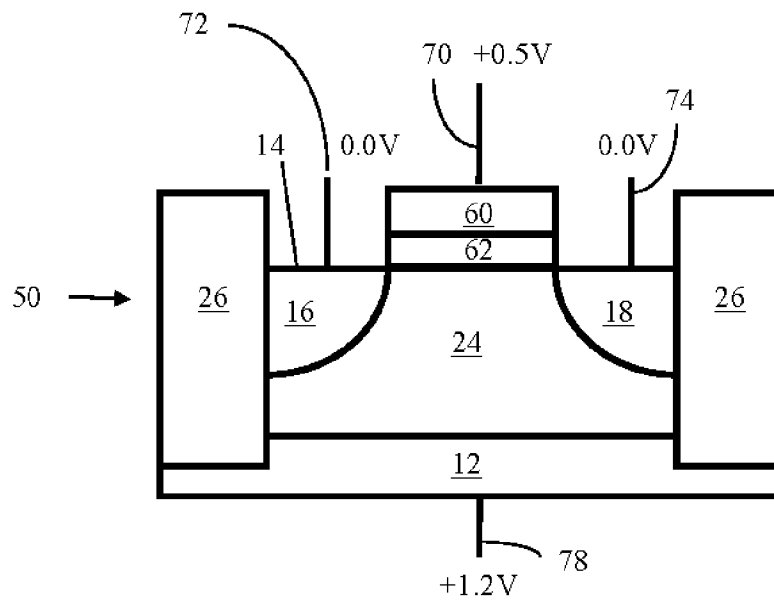


FIG. 13C

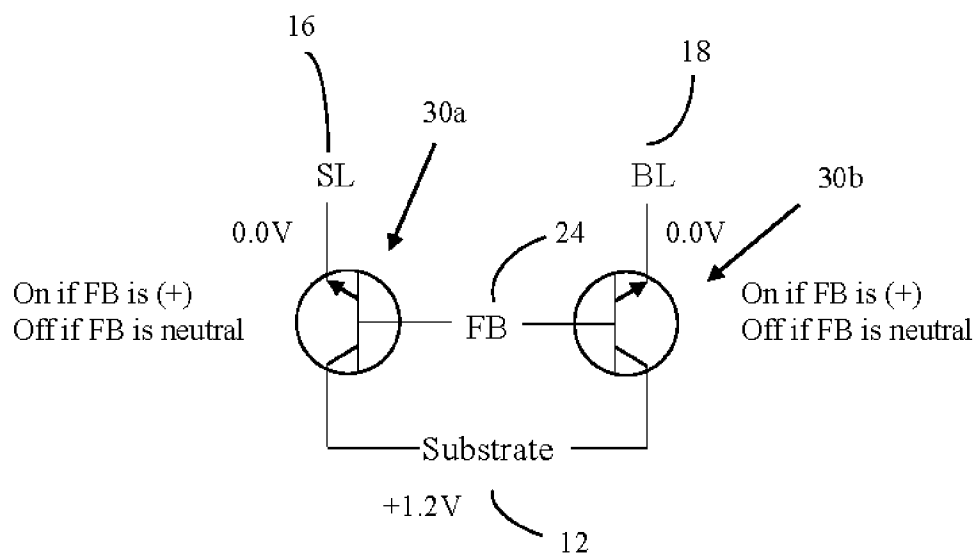


FIG. 13D

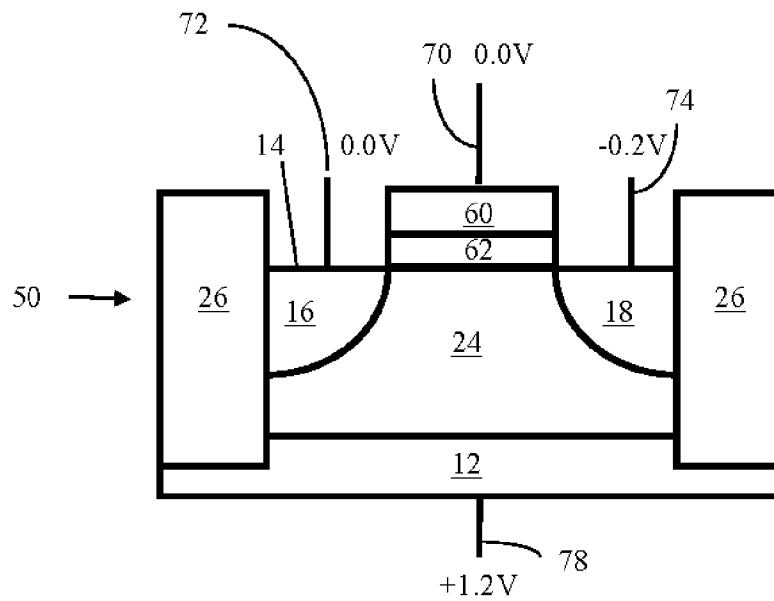


FIG. 13E

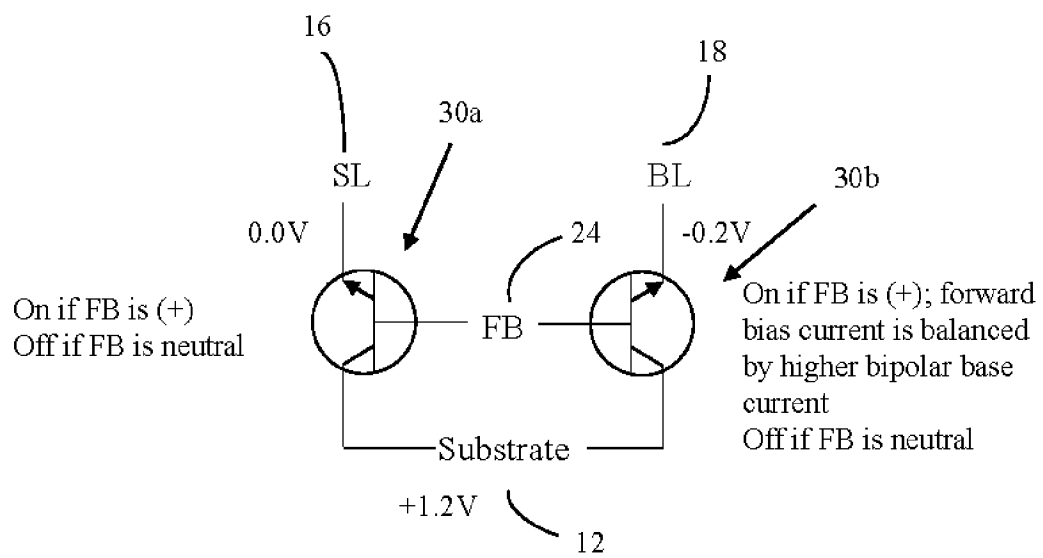


FIG. 13F

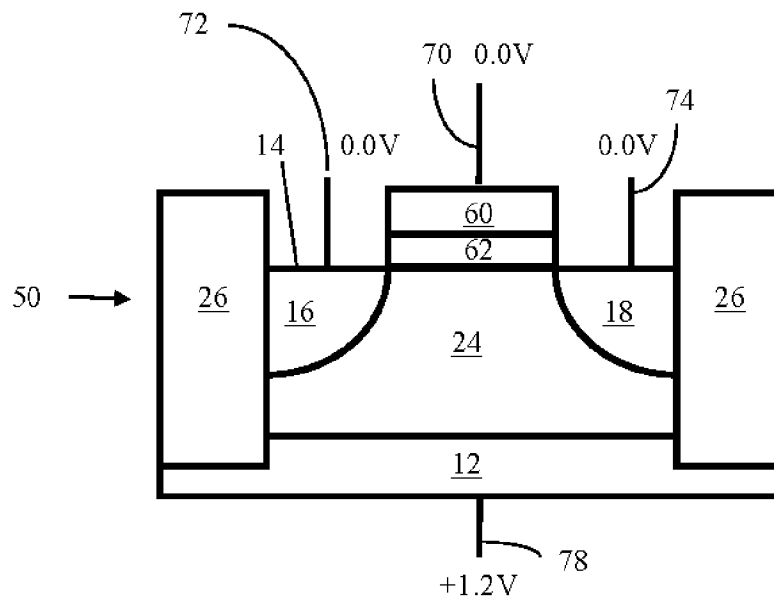


FIG. 13G

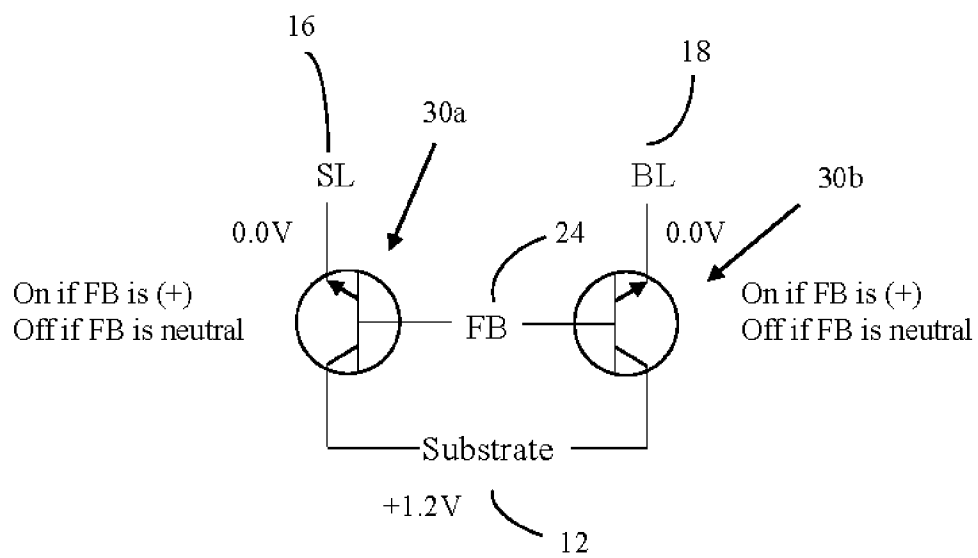


FIG. 13H

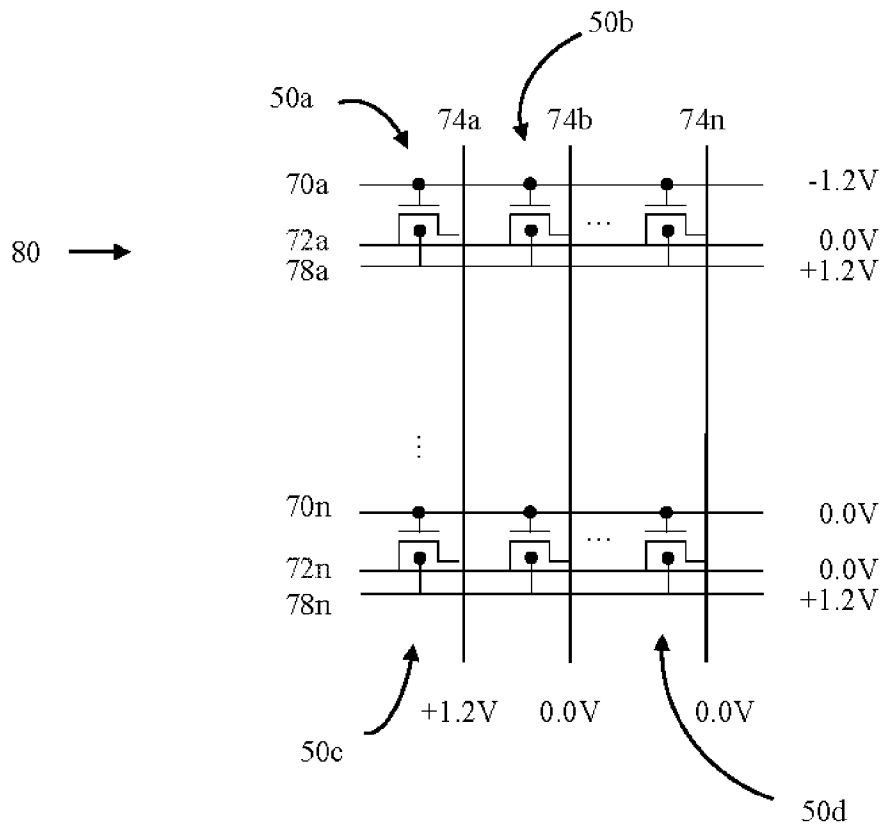


FIG. 14

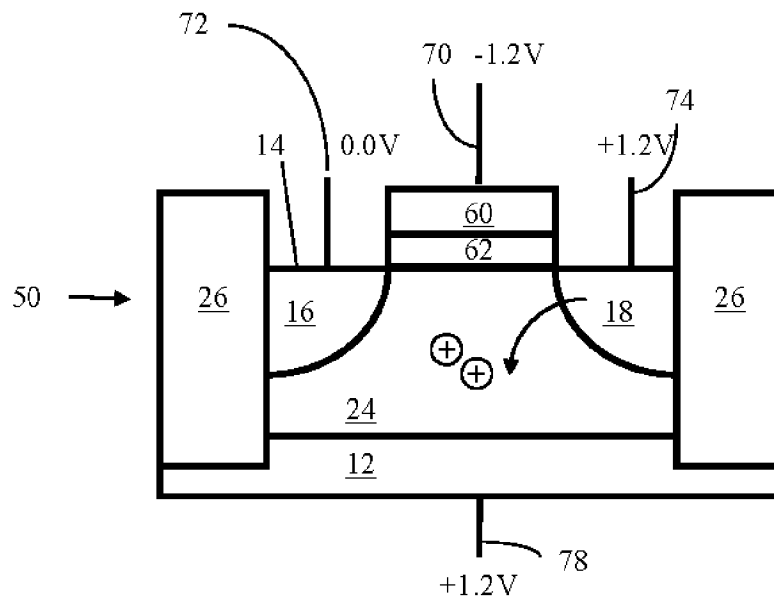


FIG. 15A

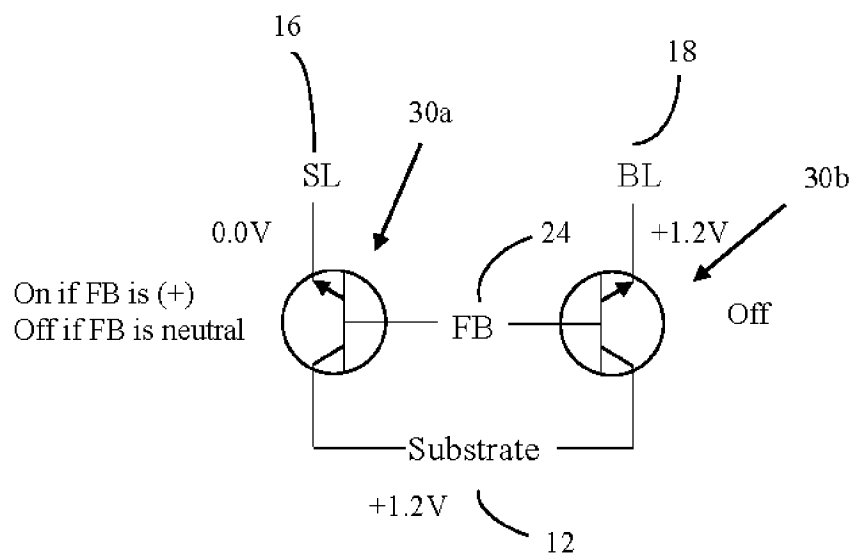


FIG. 15B

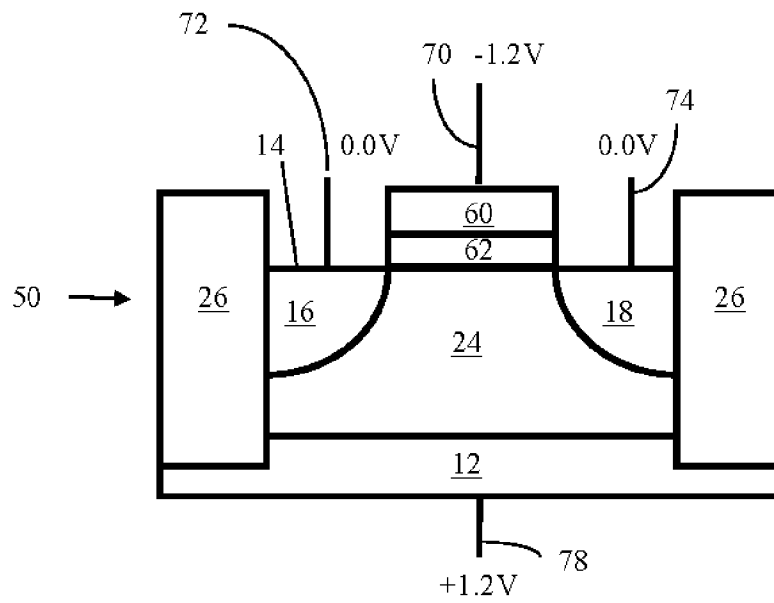


FIG. 15C

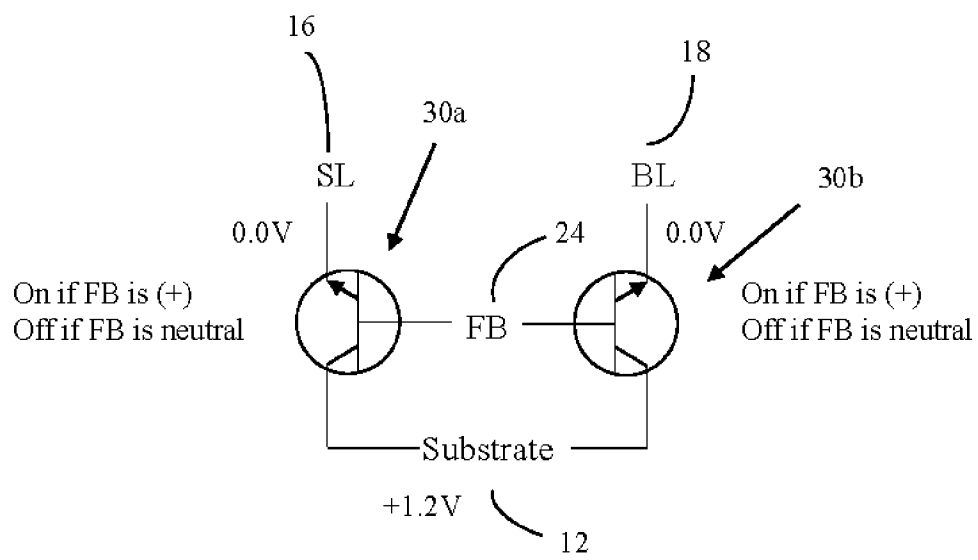


FIG. 15D

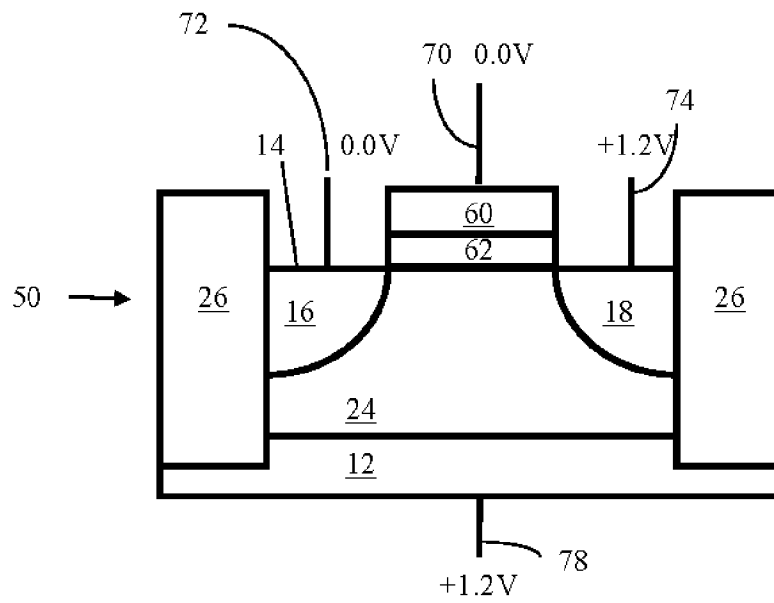


FIG. 15E

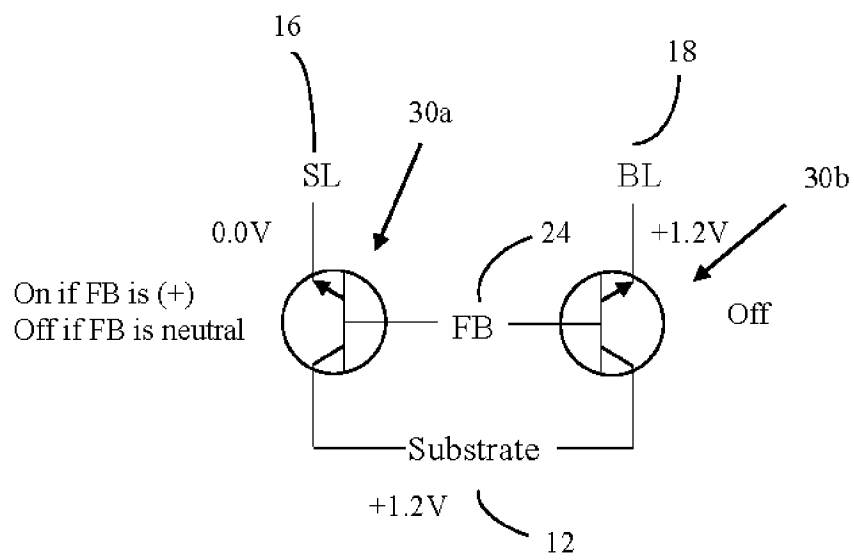


FIG. 15F

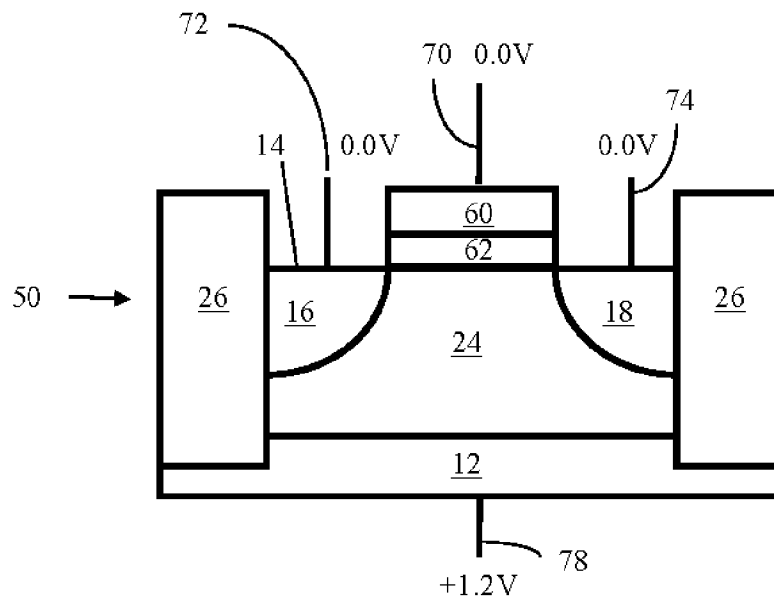


FIG. 15G

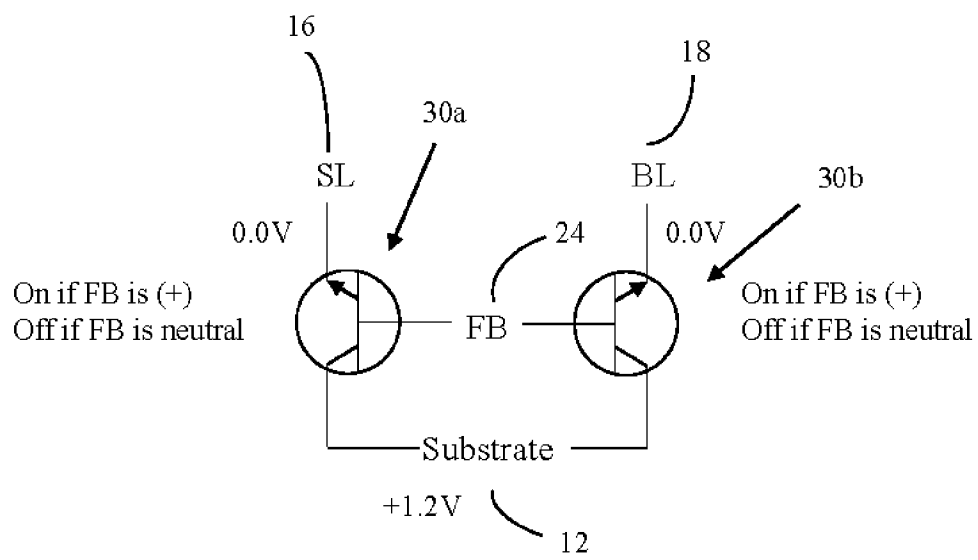


FIG. 15H

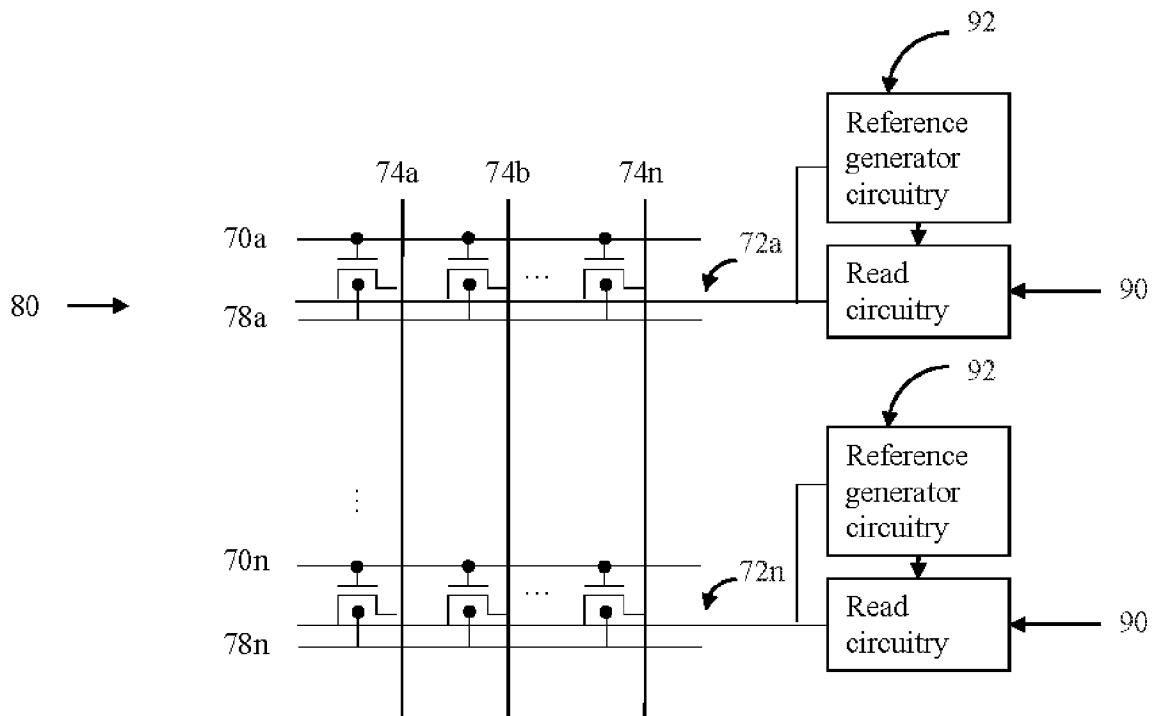


FIG. 16A

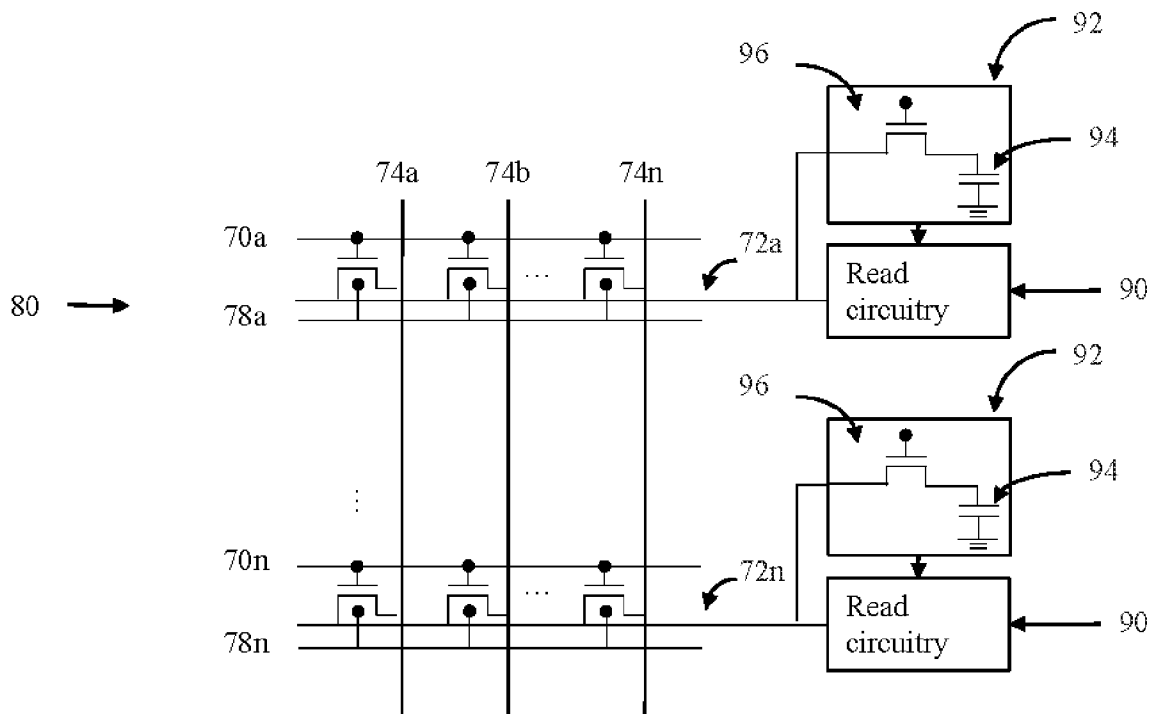


FIG. 16B

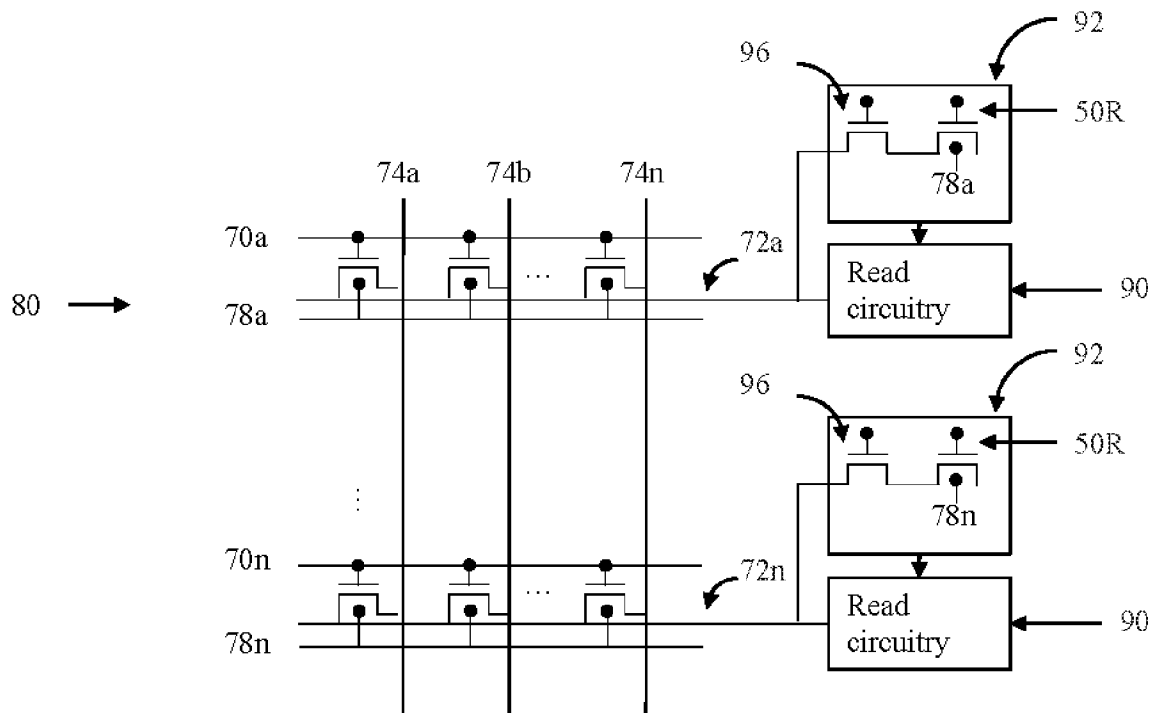


FIG. 16C

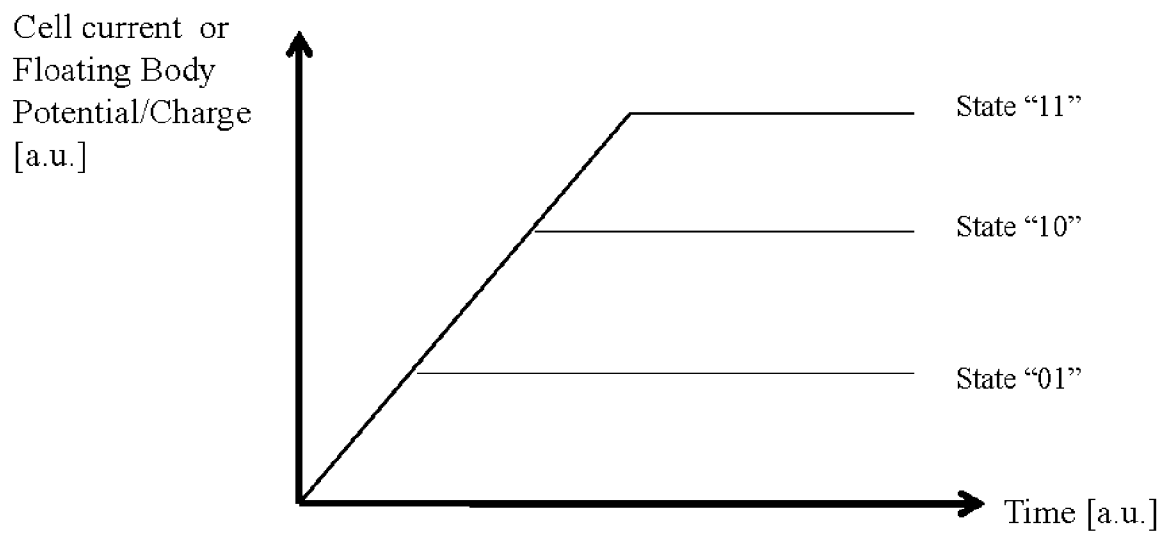


FIG. 17

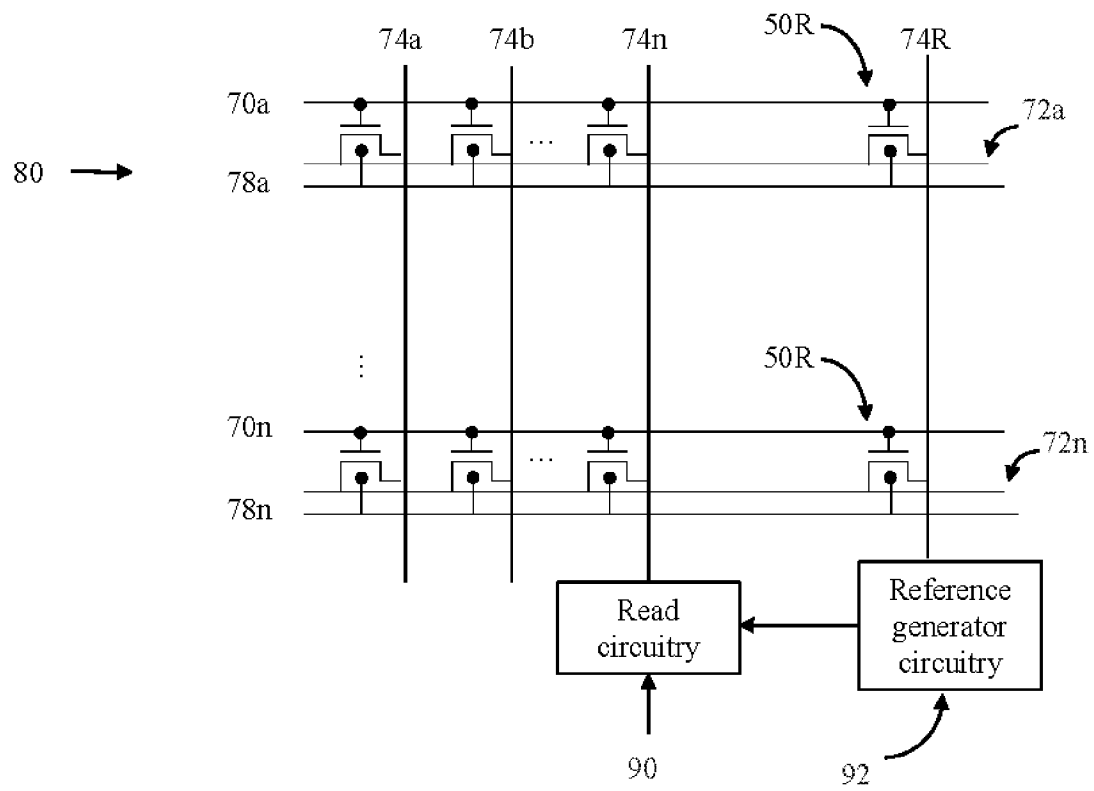


FIG. 18A

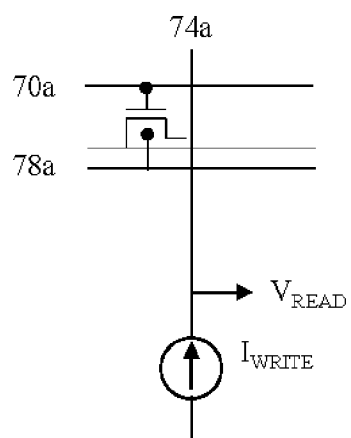


FIG. 18B

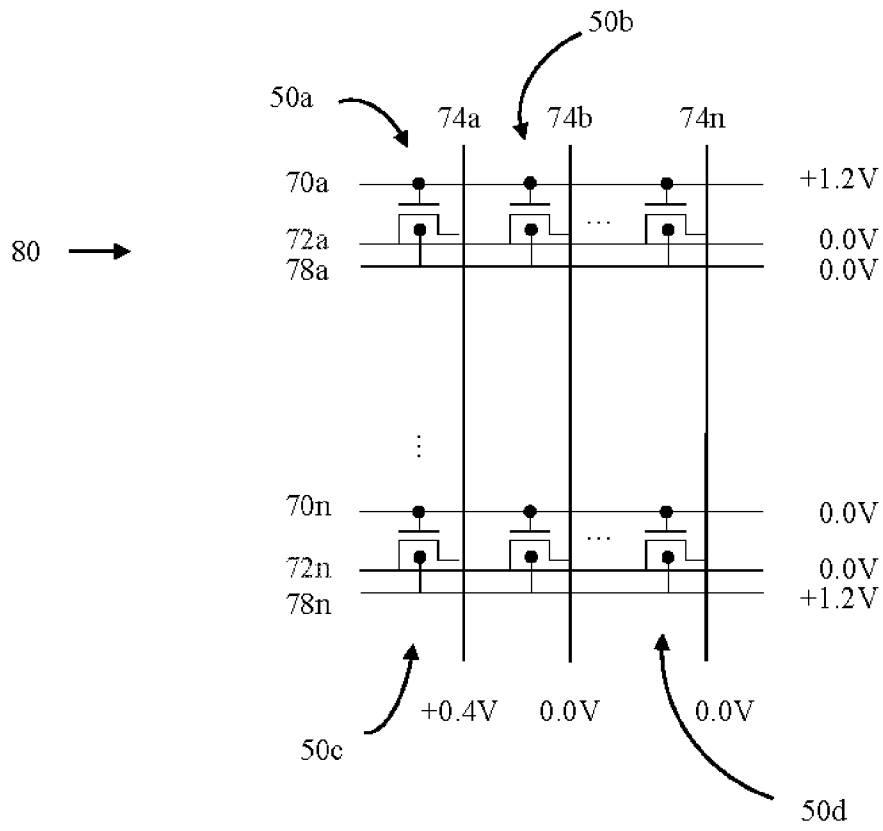


FIG. 19

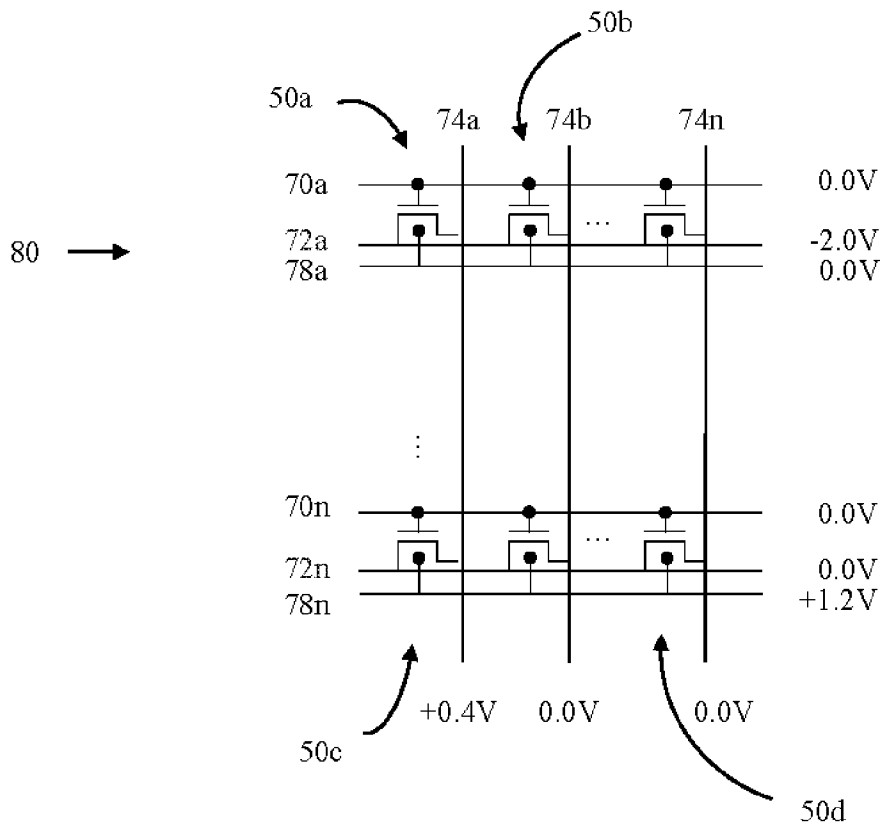


FIG. 20

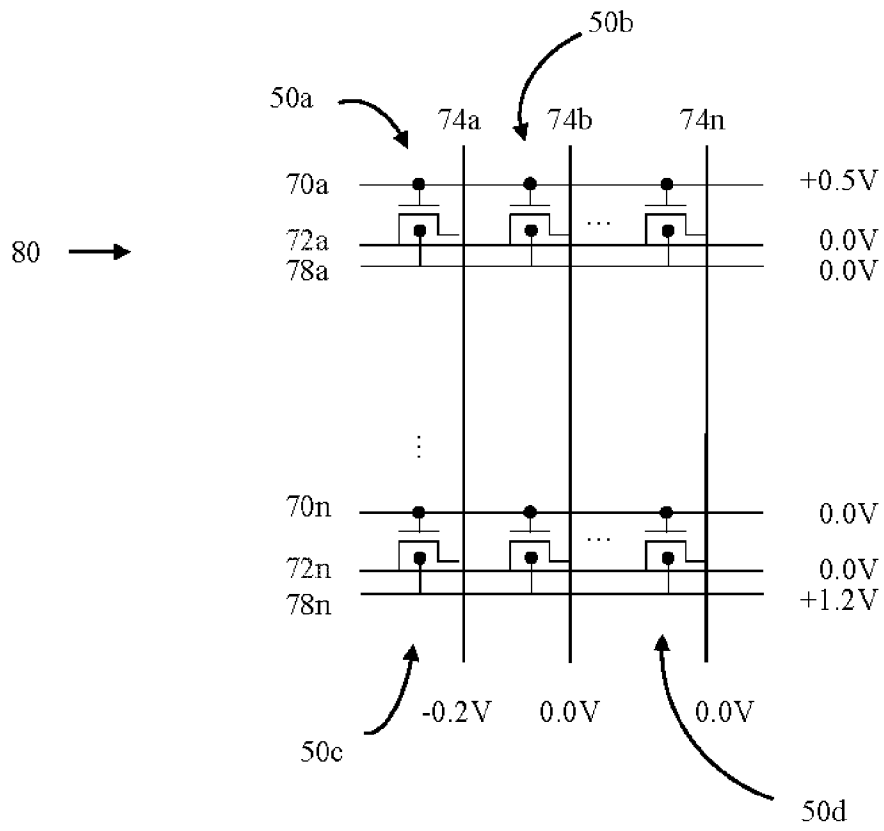


FIG. 21

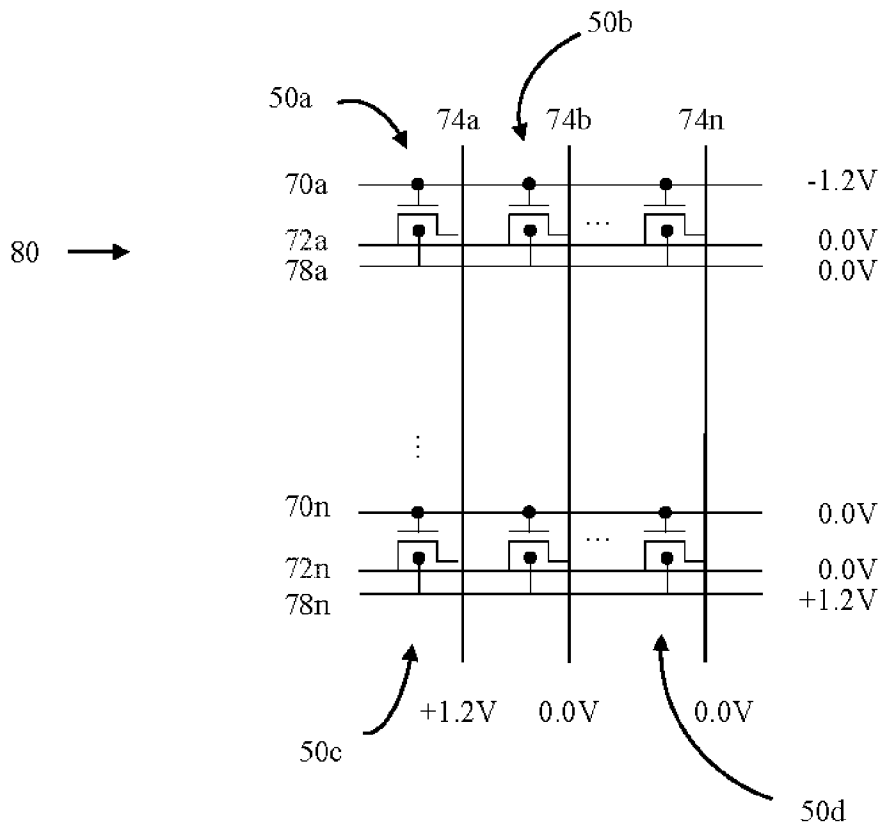


FIG. 22

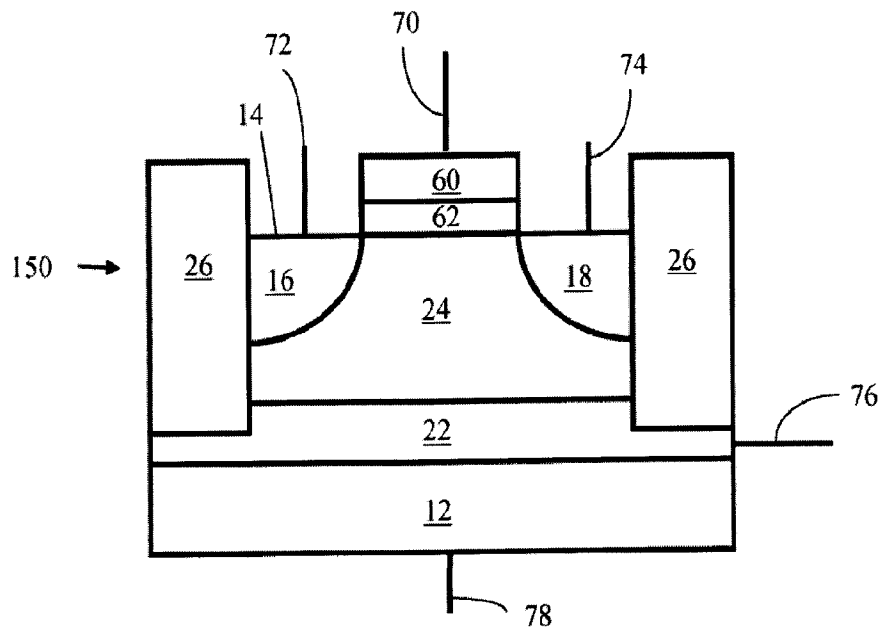


FIG. 23A

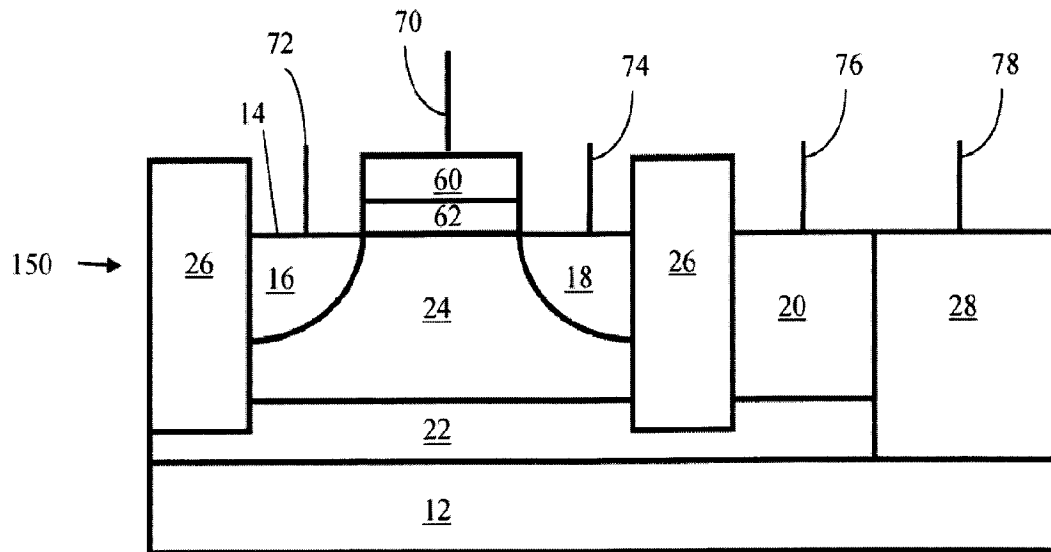


FIG. 23B

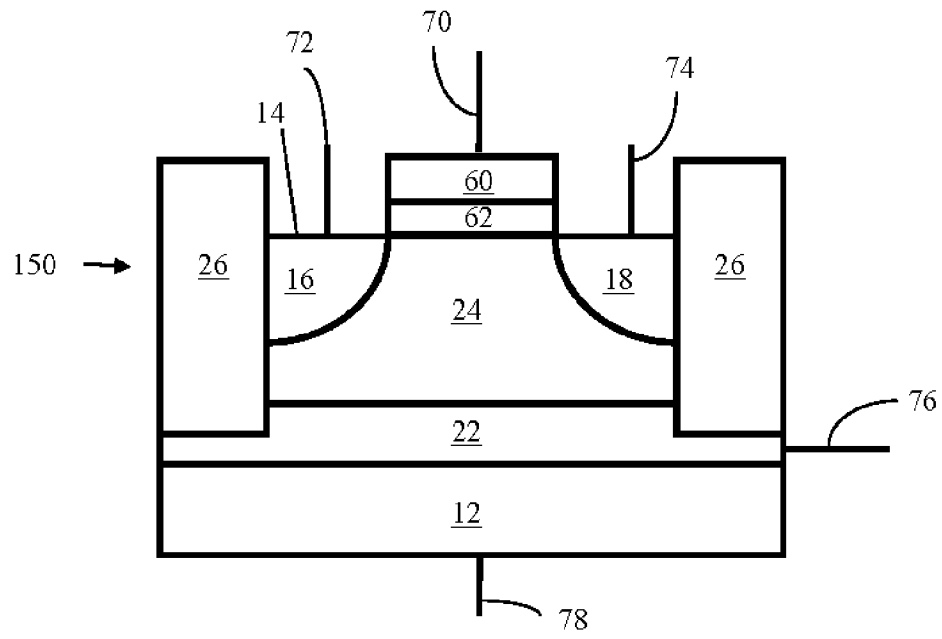


FIG. 23

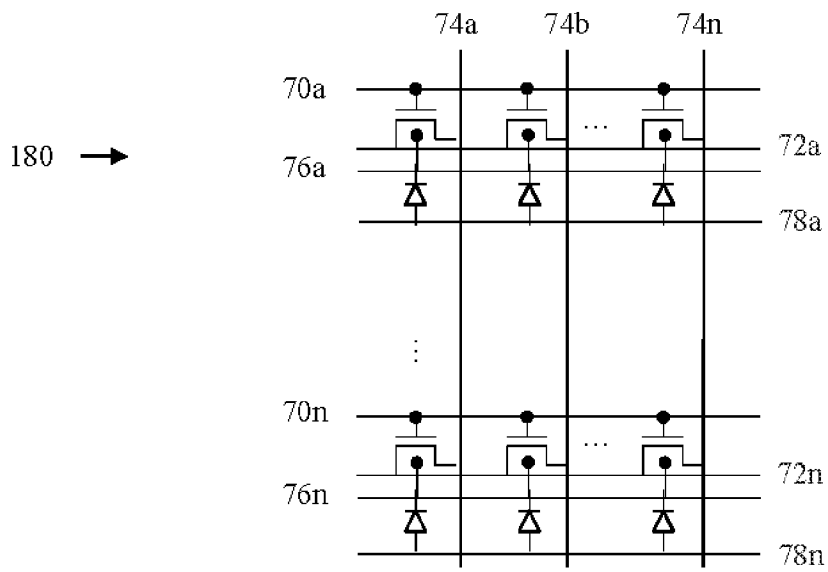


FIG. 24

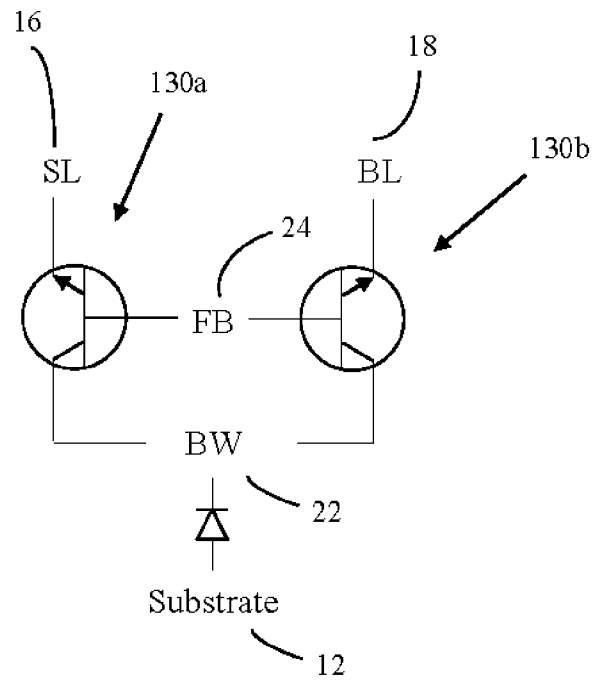


FIG. 25

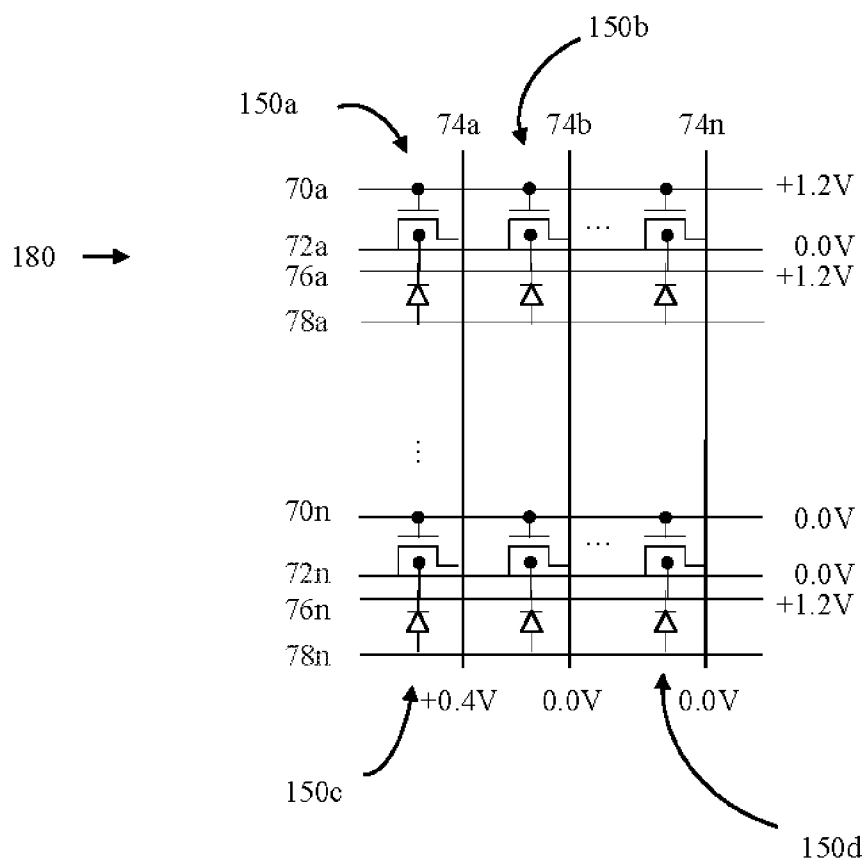


FIG. 26

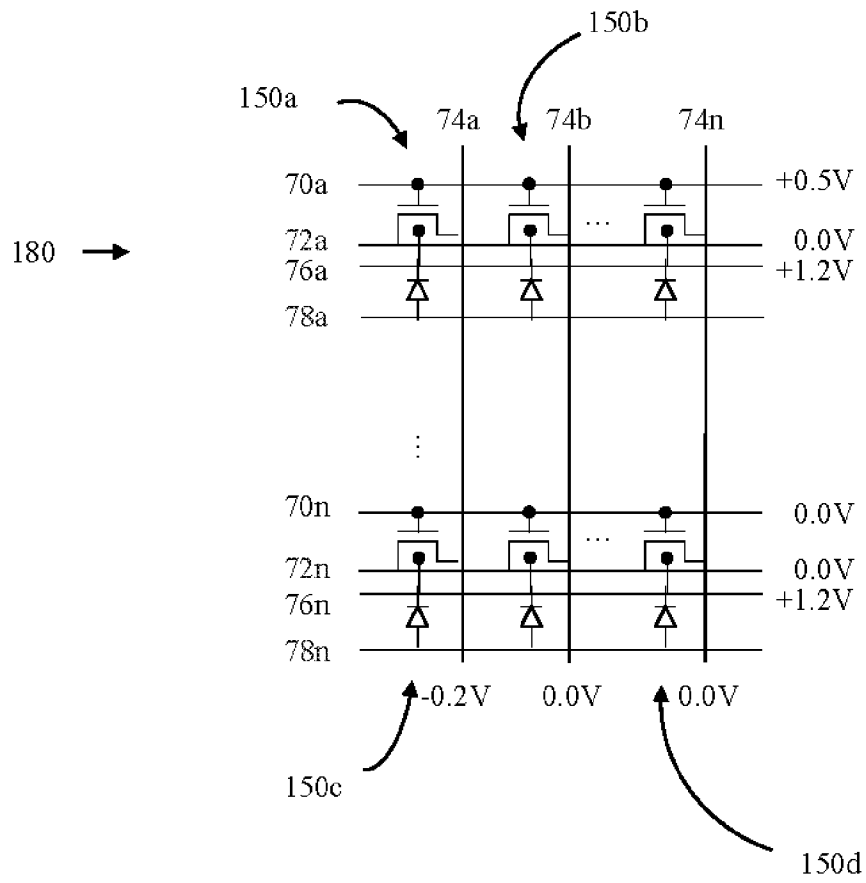


FIG. 27

The diagram shows a differential pair of MOSFETs, labeled 130a and 130b, with a common source resistor 22. The gates of both MOSFETs are connected to a feedback node FB. The source of MOSFET 130a is connected to a supply voltage 16 (SL) at 0.0V. The source of MOSFET 130b is connected to a supply voltage 18 (BL) at -0.2V. The common source resistor 22 is connected between the sources of the two MOSFETs and a substrate 12. The other end of the resistor 22 is connected to a bias voltage BW at 0.0V. The resistor 22 is labeled as 'Reverse biased'. The output of MOSFET 130a is labeled 24. The operating conditions are specified as: 'On if FB is (+)' and 'Off if FB is neutral' for both MOSFETs.

FIG. 28B

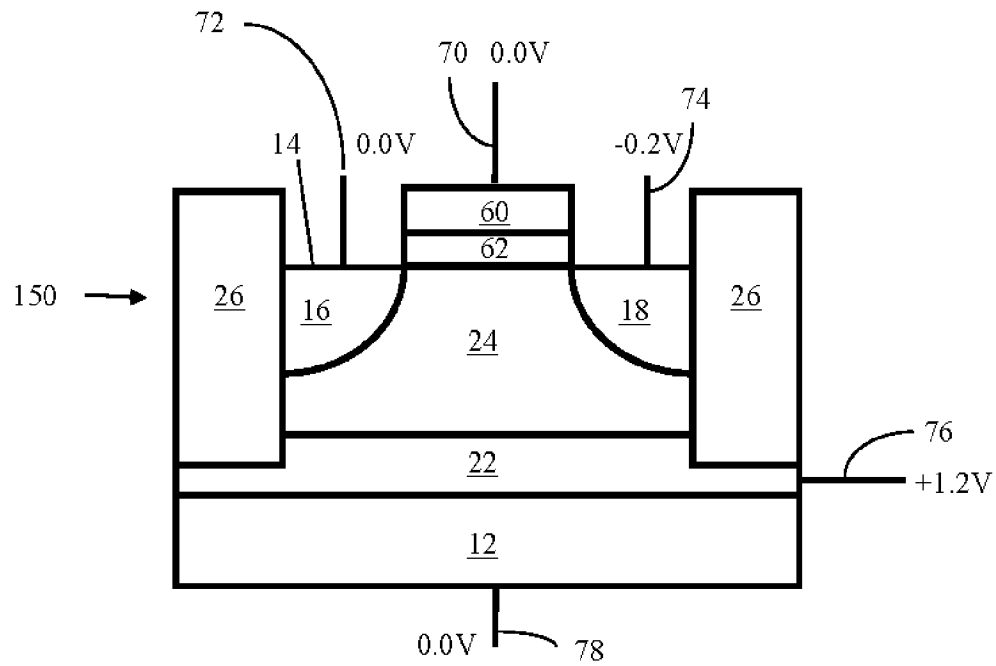


FIG. 28E

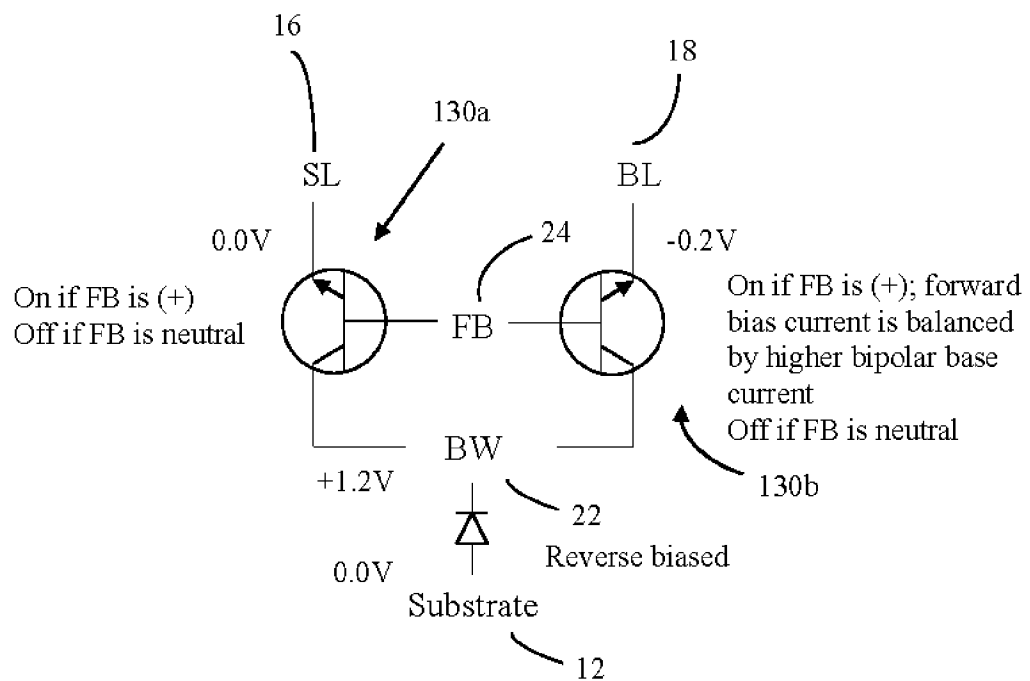


FIG. 28F

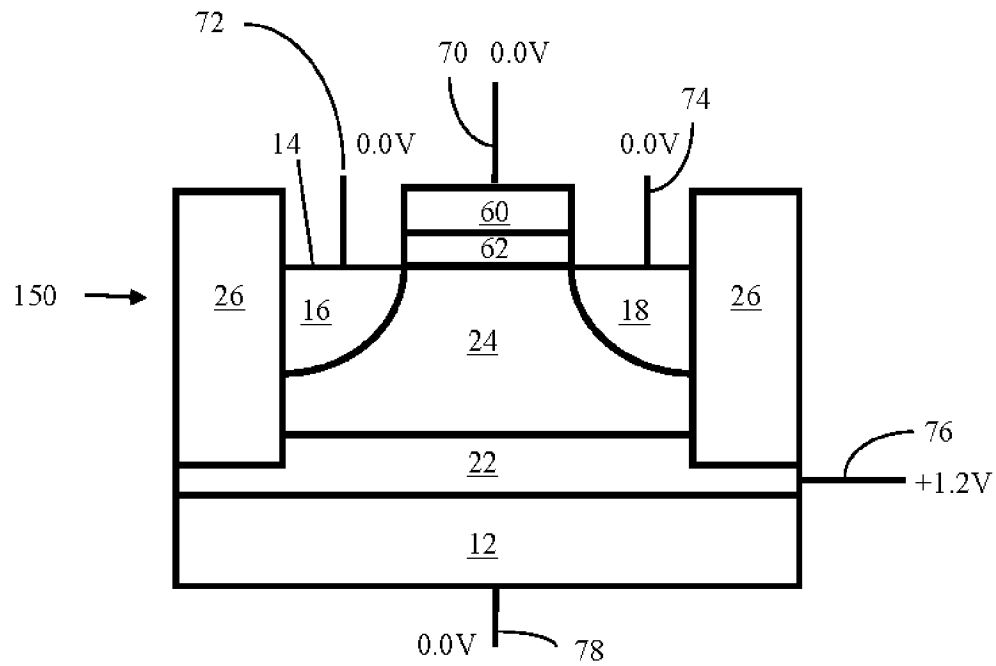


FIG. 28G

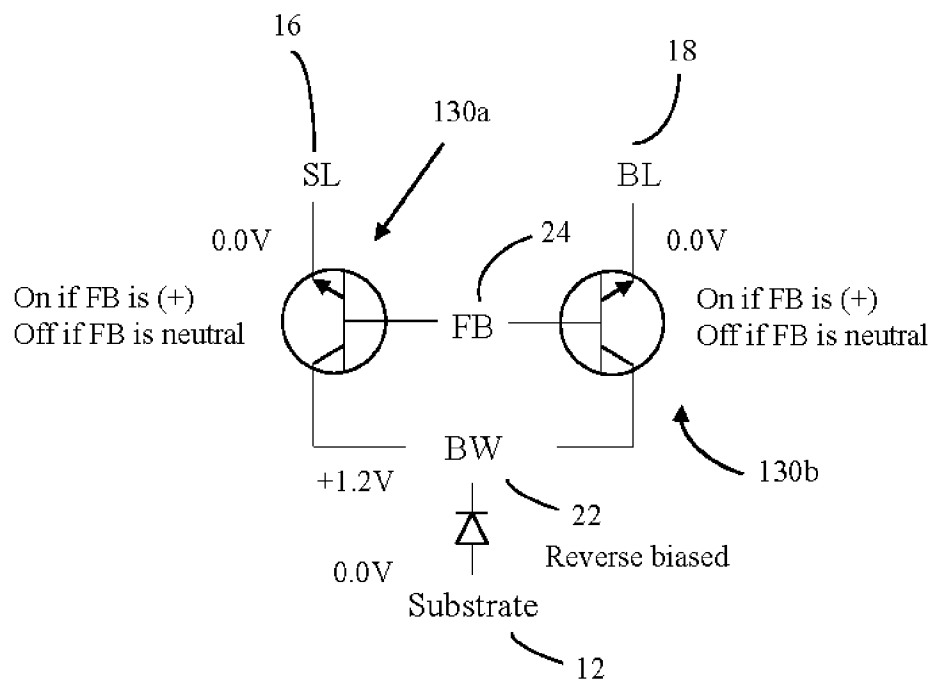


FIG. 28H

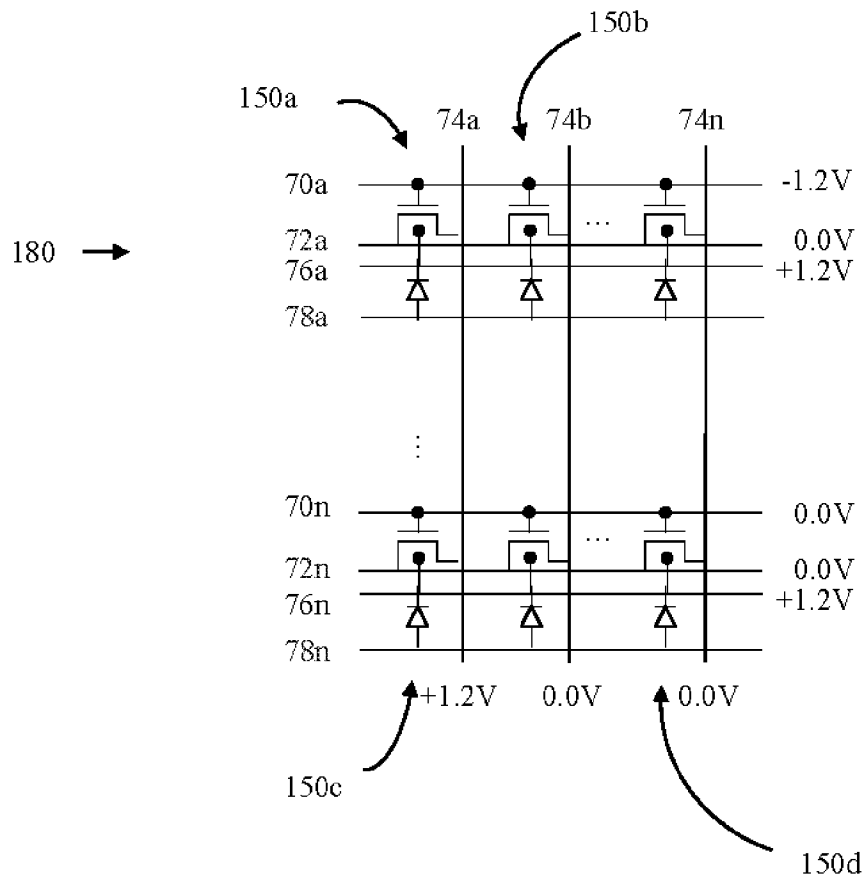


FIG. 29

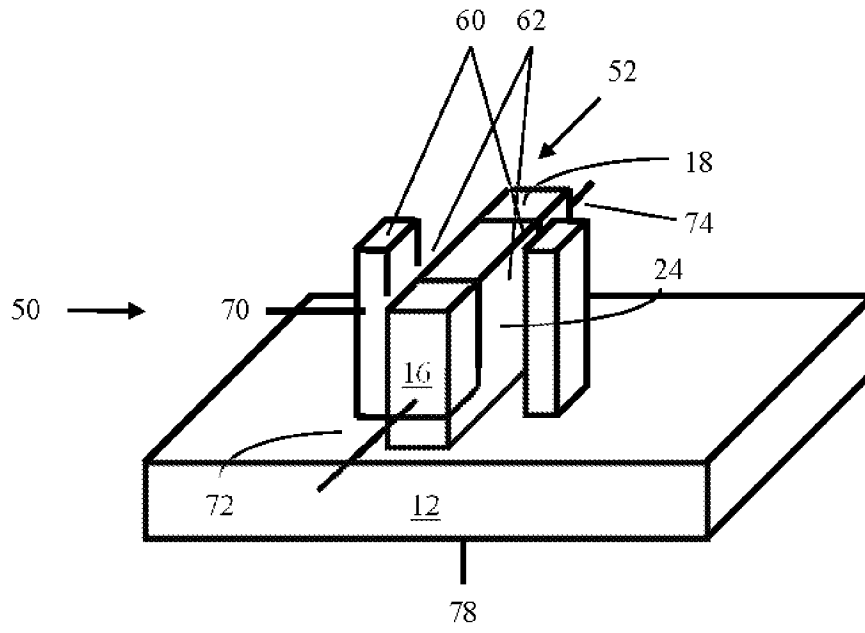


FIG. 30

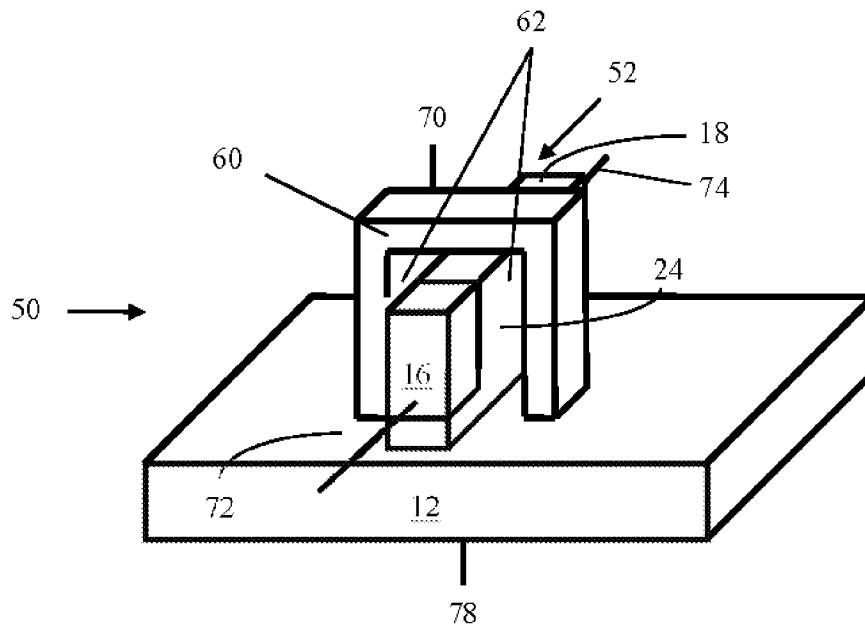


FIG. 31

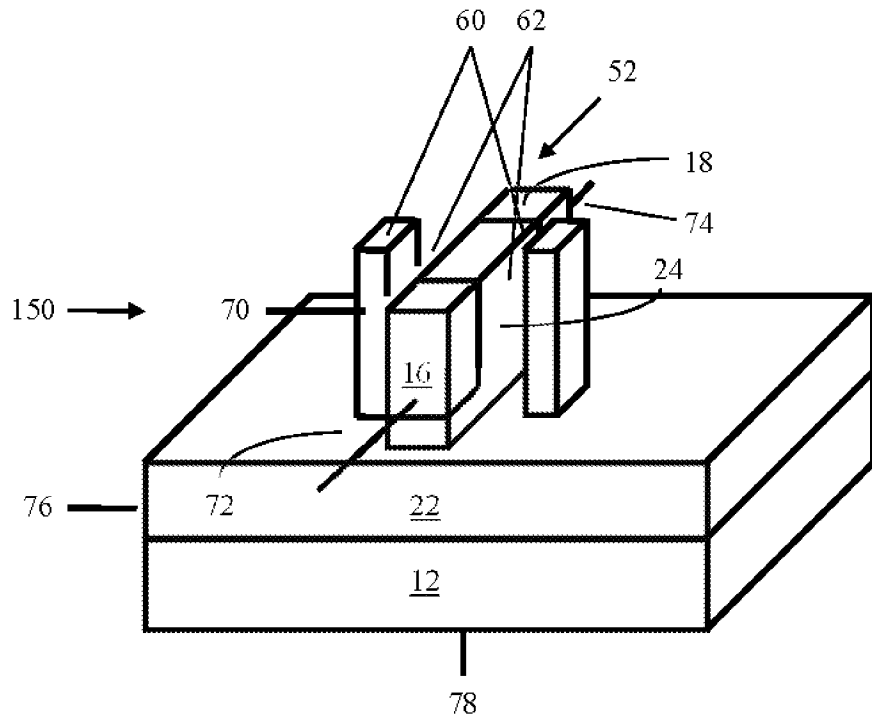


FIG. 32

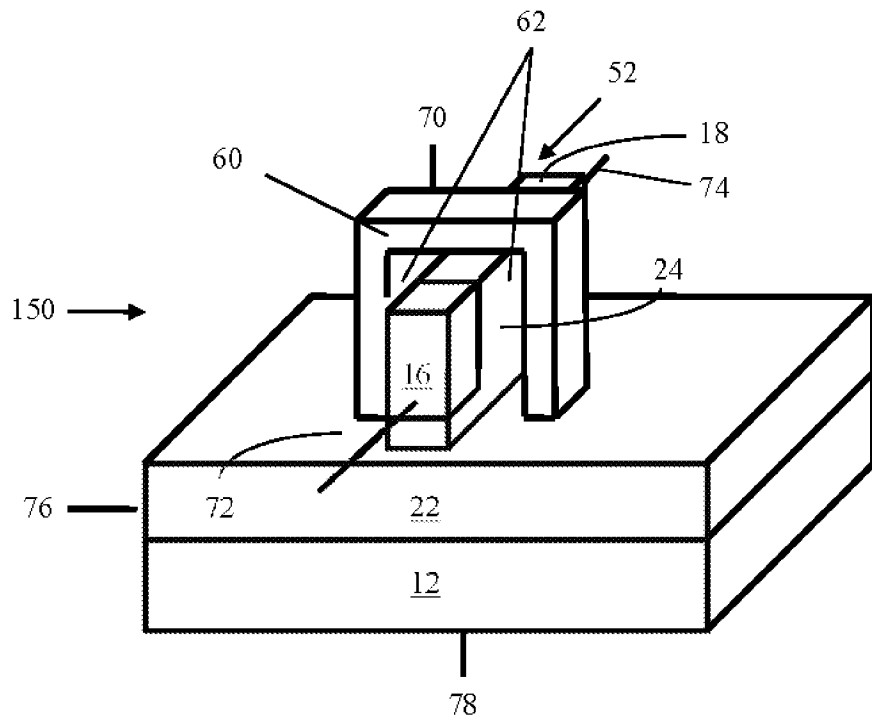


FIG. 33

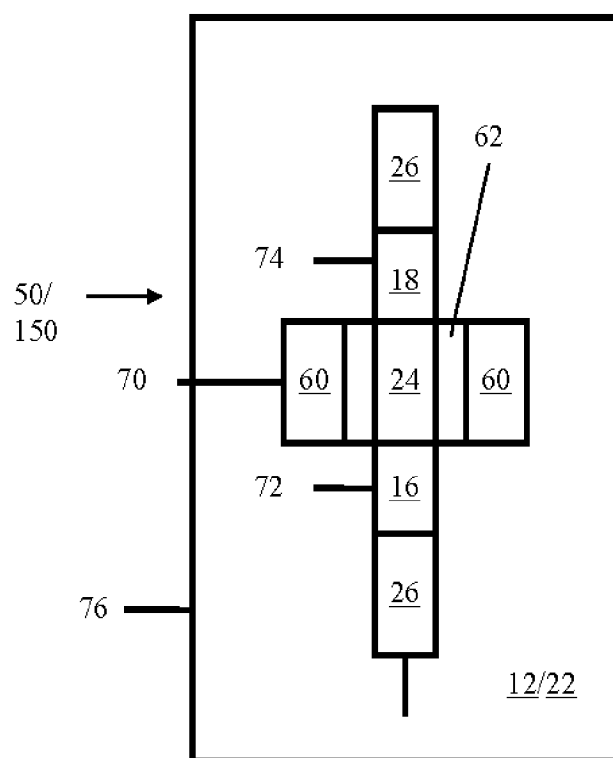


FIG. 34

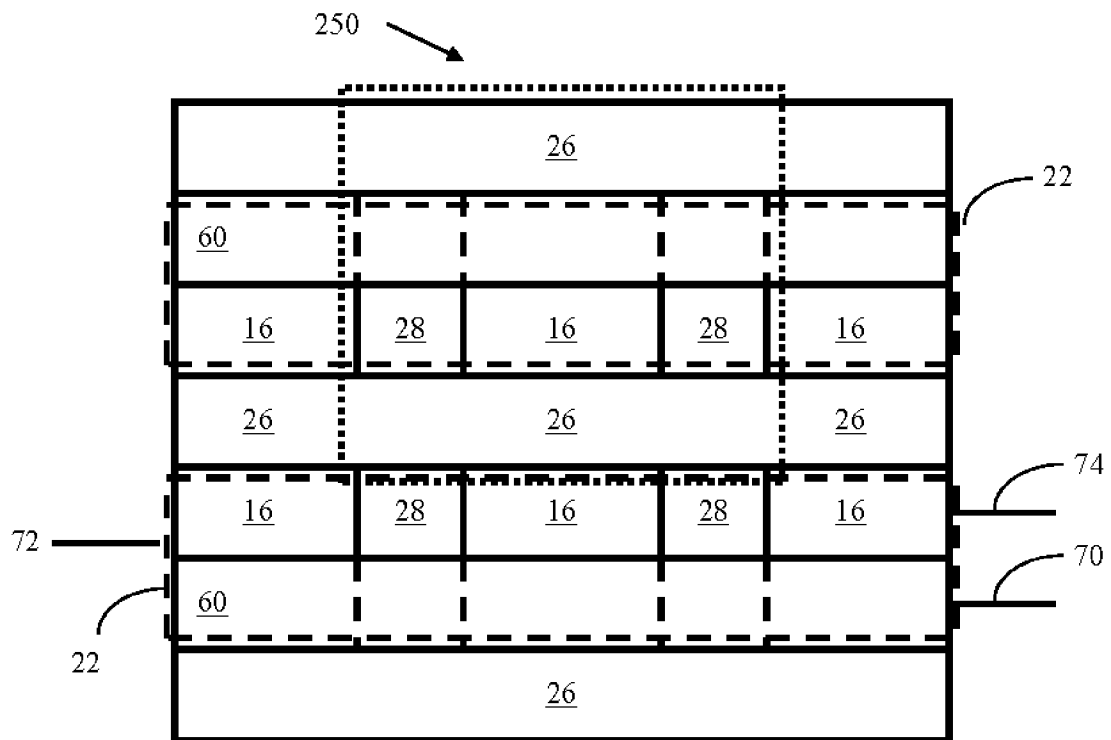


FIG. 35A

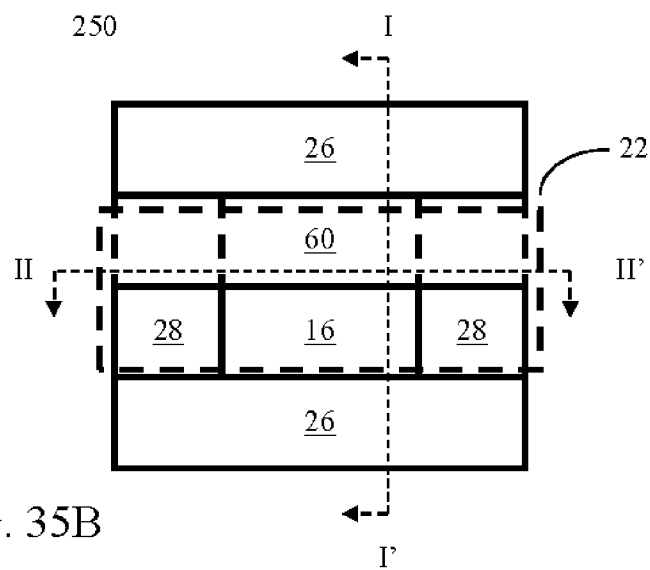


FIG. 35B

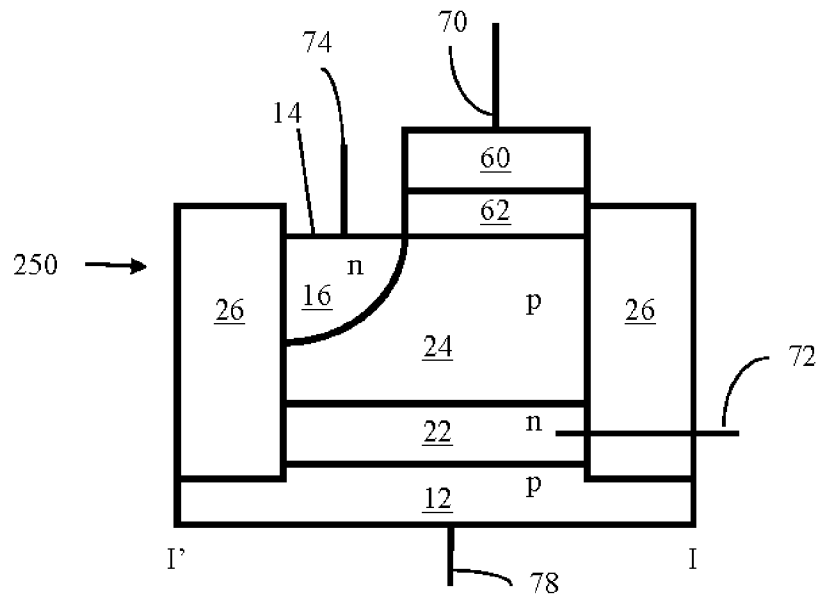


FIG. 35C

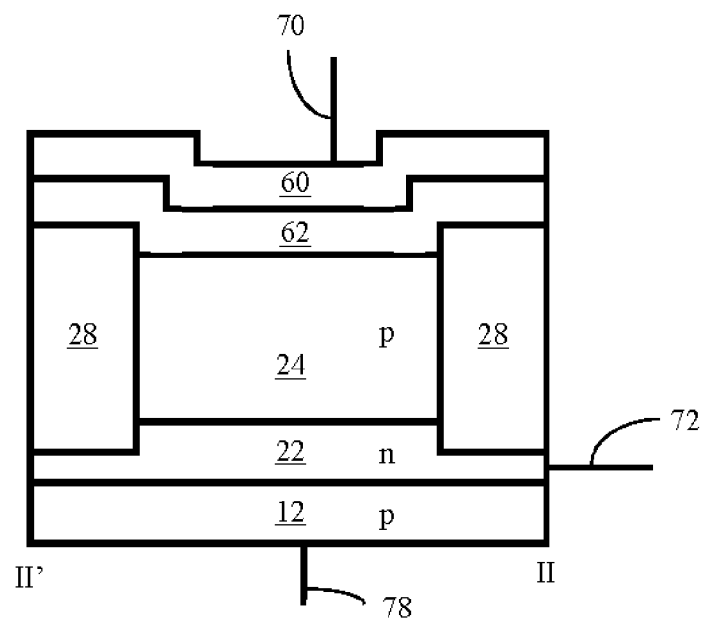


FIG. 35D

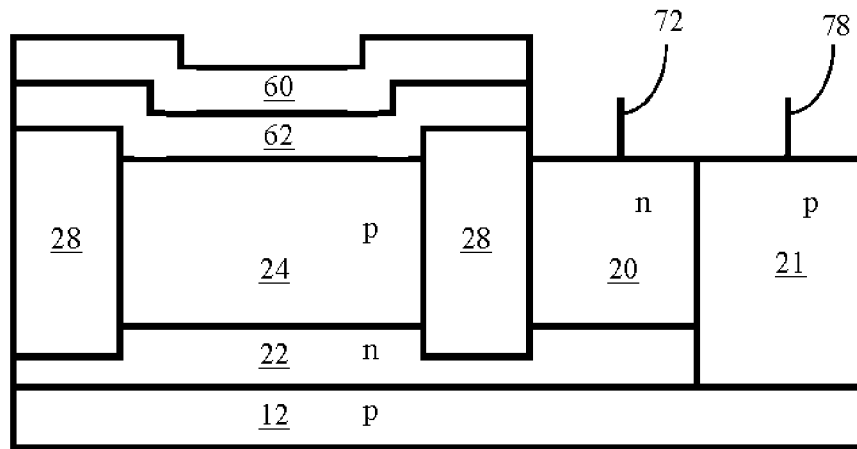


FIG. 35E

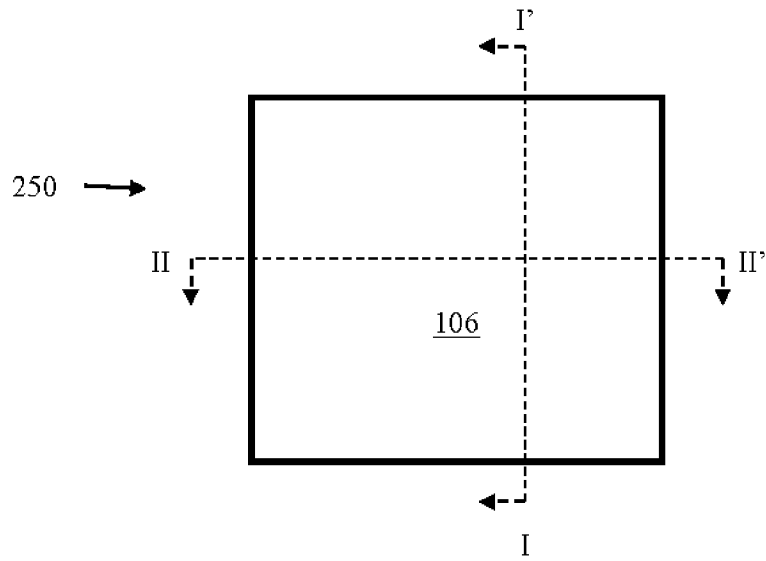


FIG. 36A

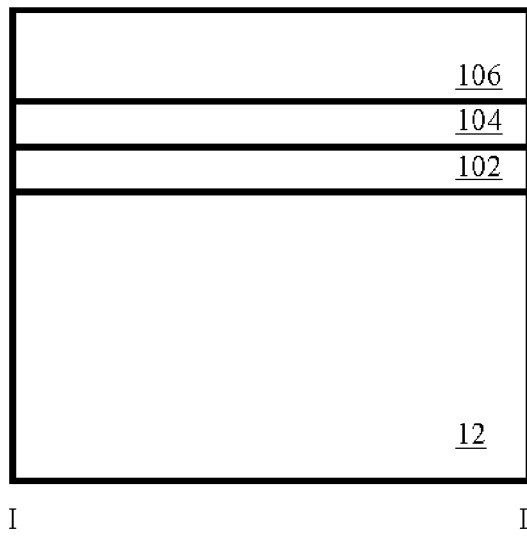


FIG. 36B

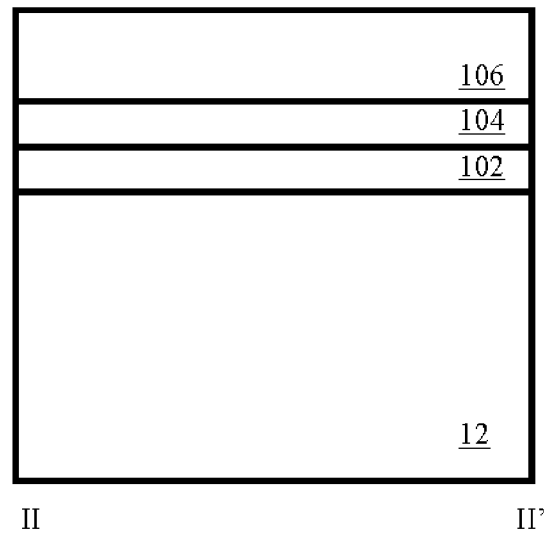


FIG. 36C

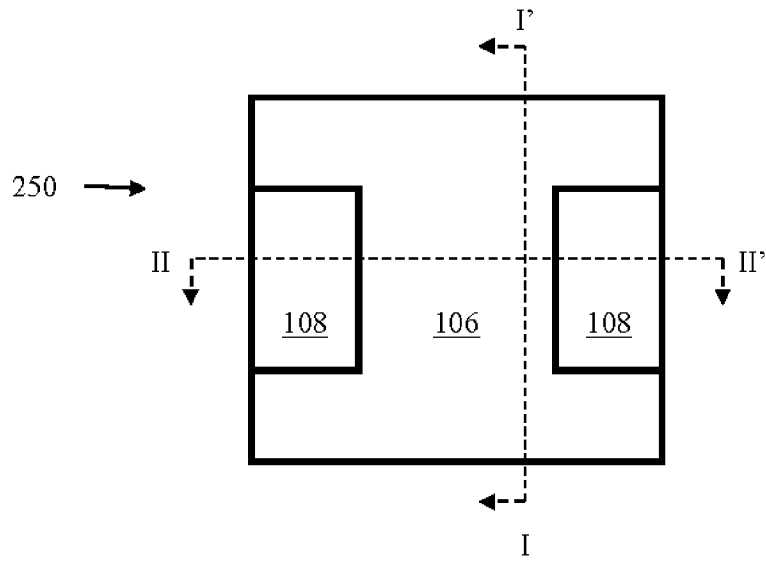


FIG. 36D

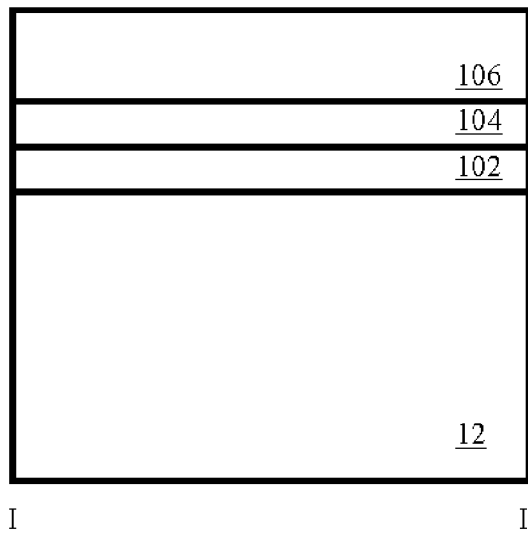


FIG. 36E

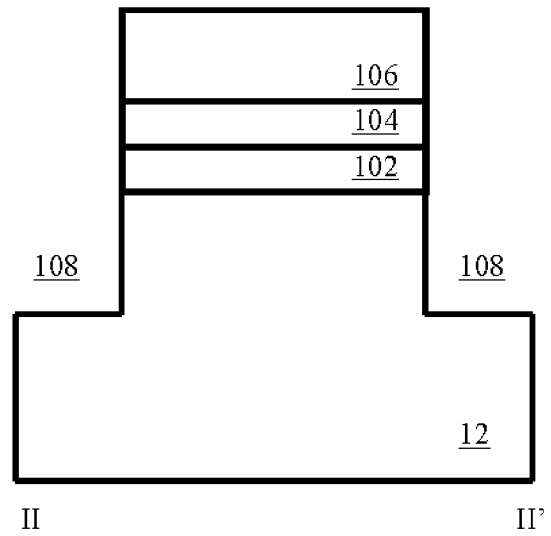


FIG. 36F

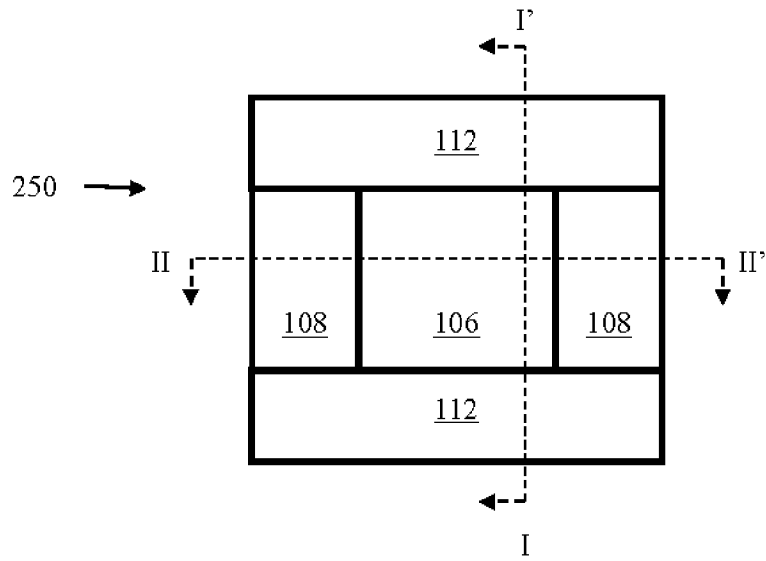


FIG. 36G

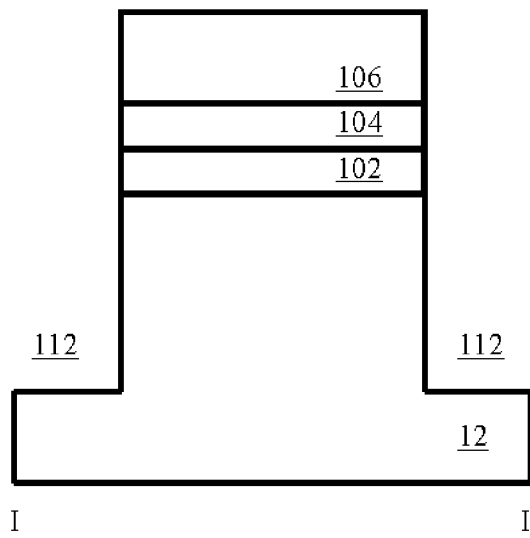


FIG. 36H

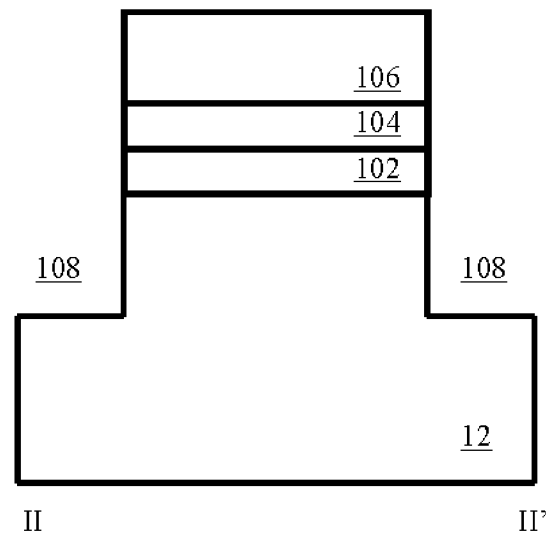


FIG. 36I

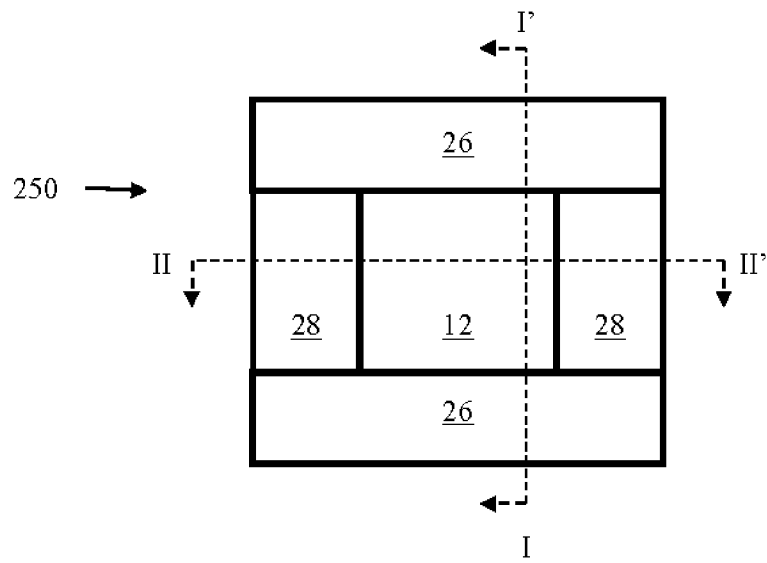


FIG. 36J

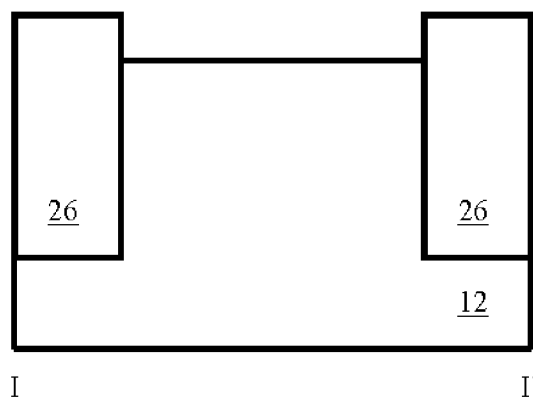


FIG. 36K

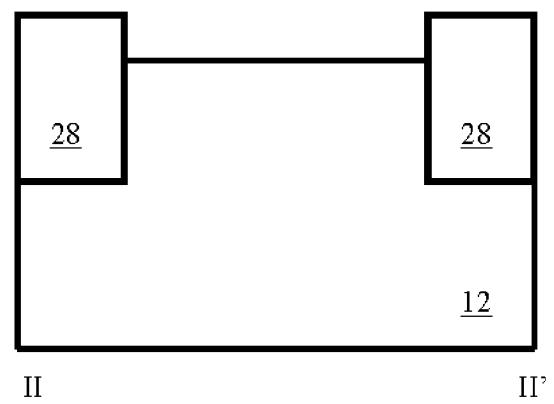


FIG. 36L

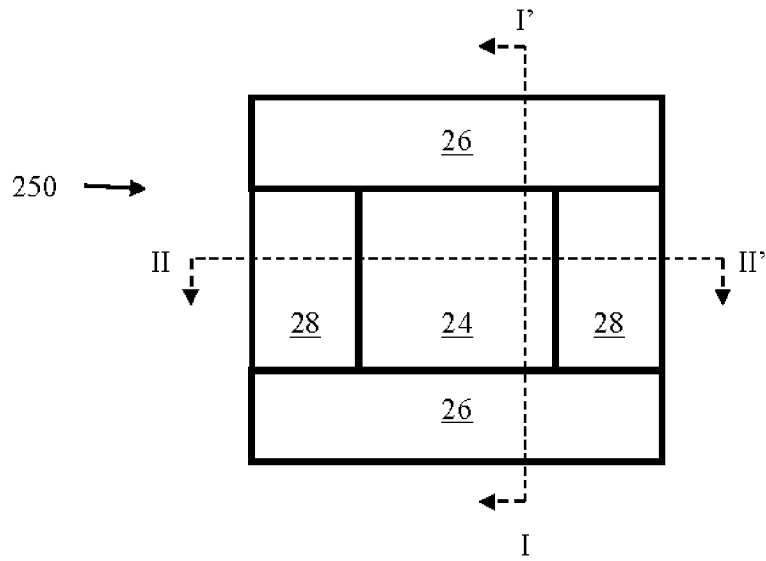


FIG. 36M

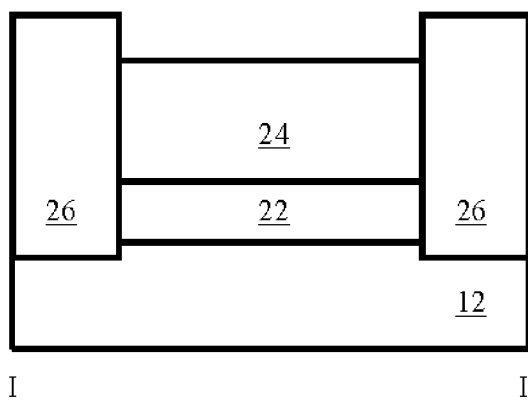


FIG. 36N

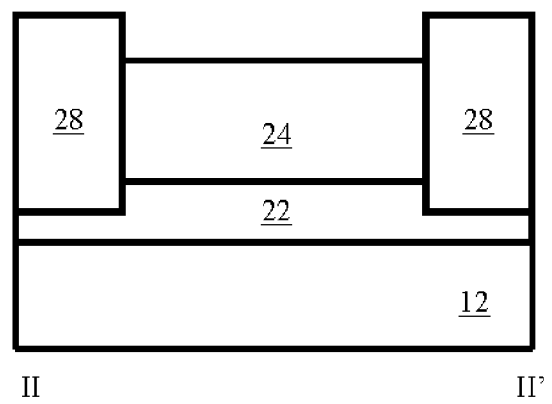


FIG. 36O

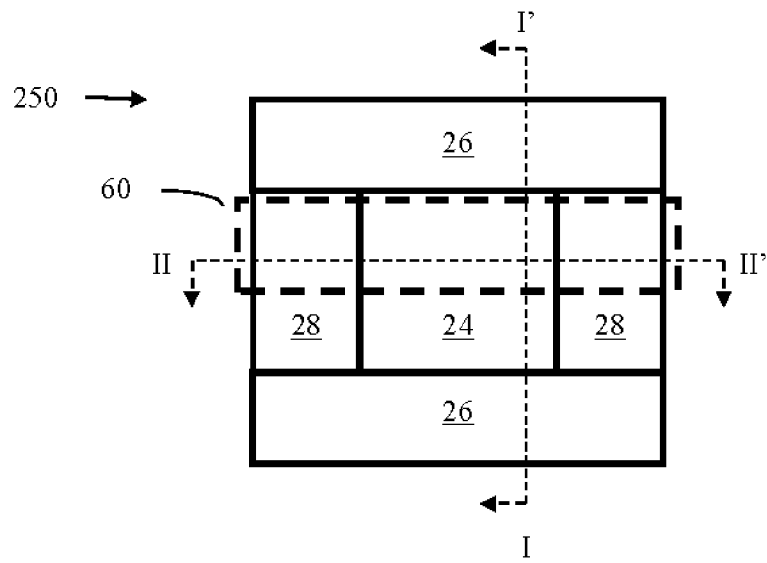


FIG. 36P

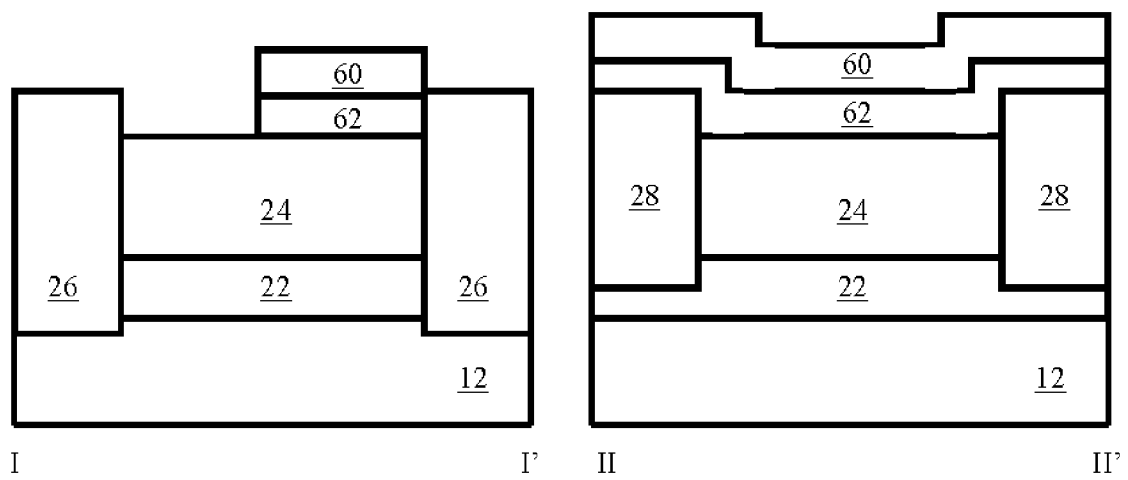


FIG. 36Q

FIG. 36R

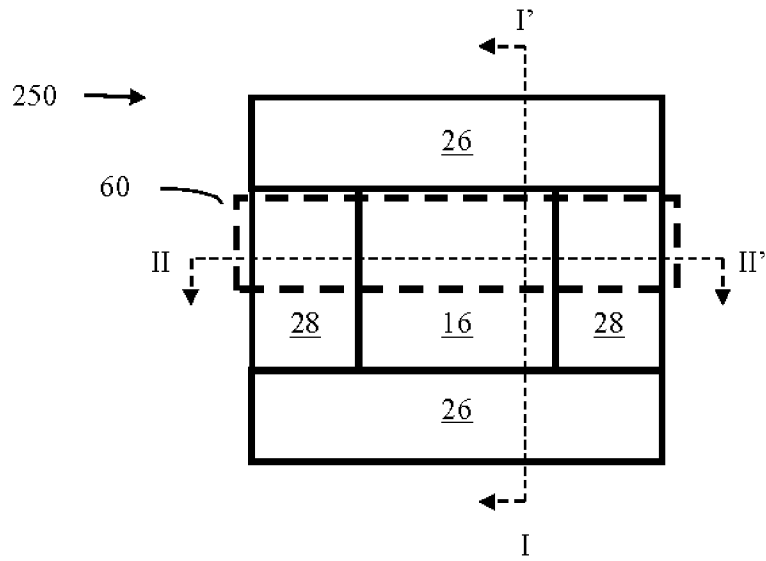


FIG. 36S

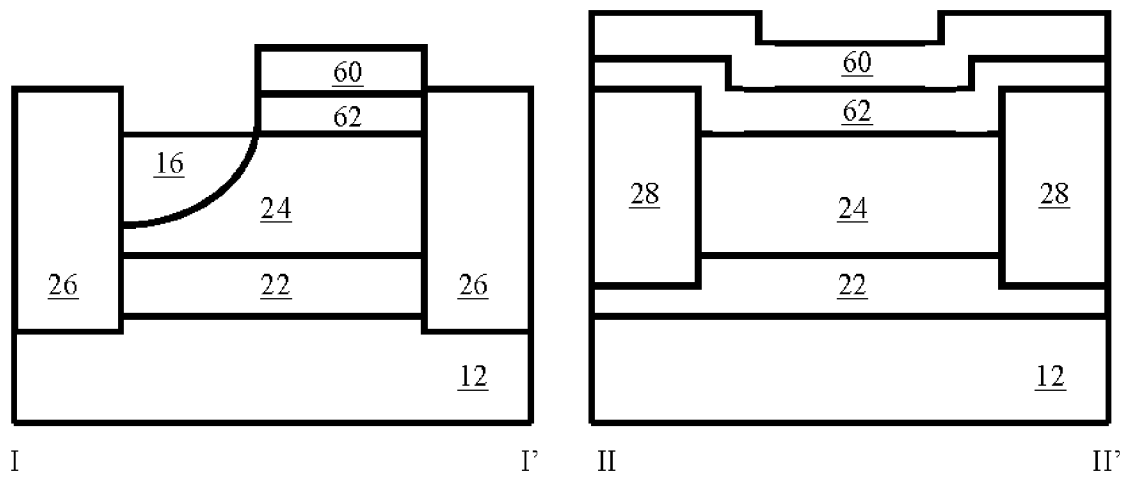


FIG. 36T

FIG. 36U

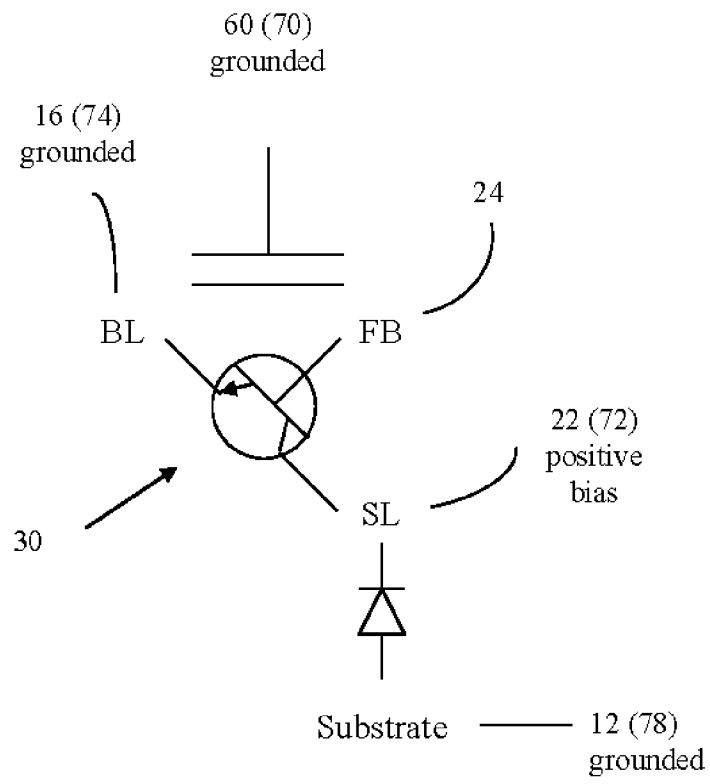


FIG. 37A

Floating Body 24 is positively charged and $V(\text{BL } 16) = 0.0\text{V}$

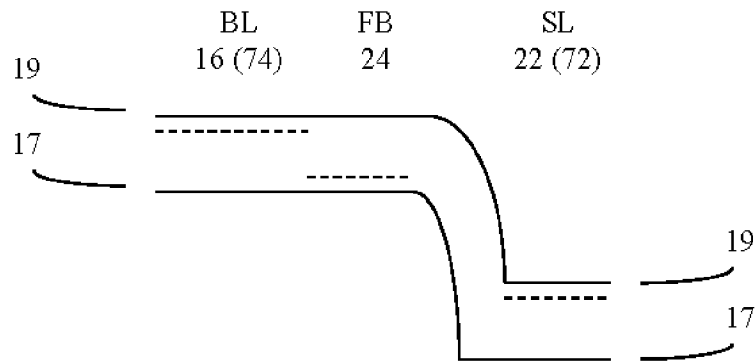


FIG. 37B

FB is neutrally charged; and $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

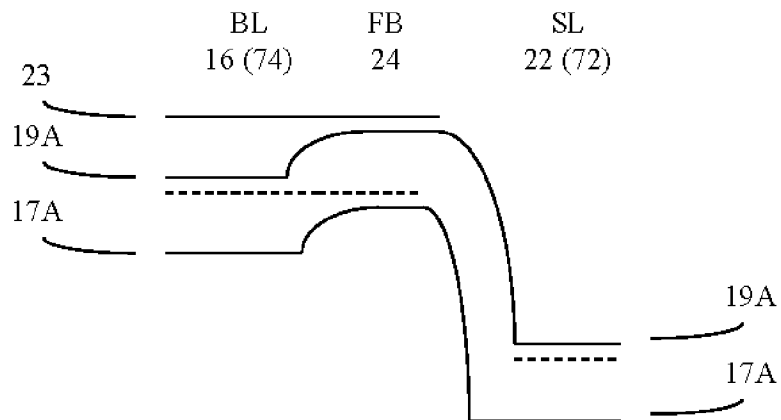


FIG. 37C

Exemplary Memory Array 280 with
Representative Memory Cells 250a, 250b, 250c and 250d

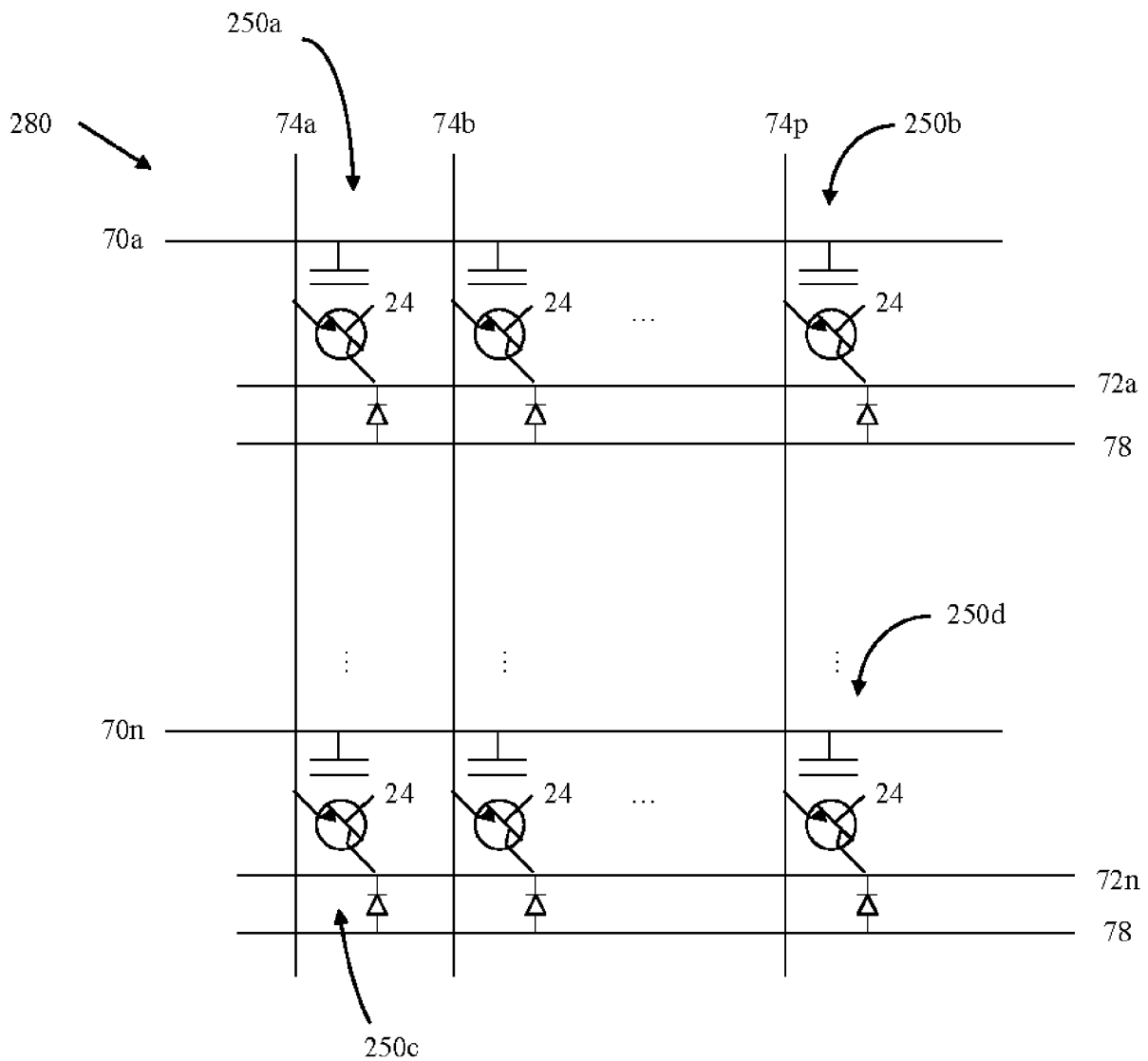


FIG. 38A

Array Hold Operation (All Memory Cells 250)

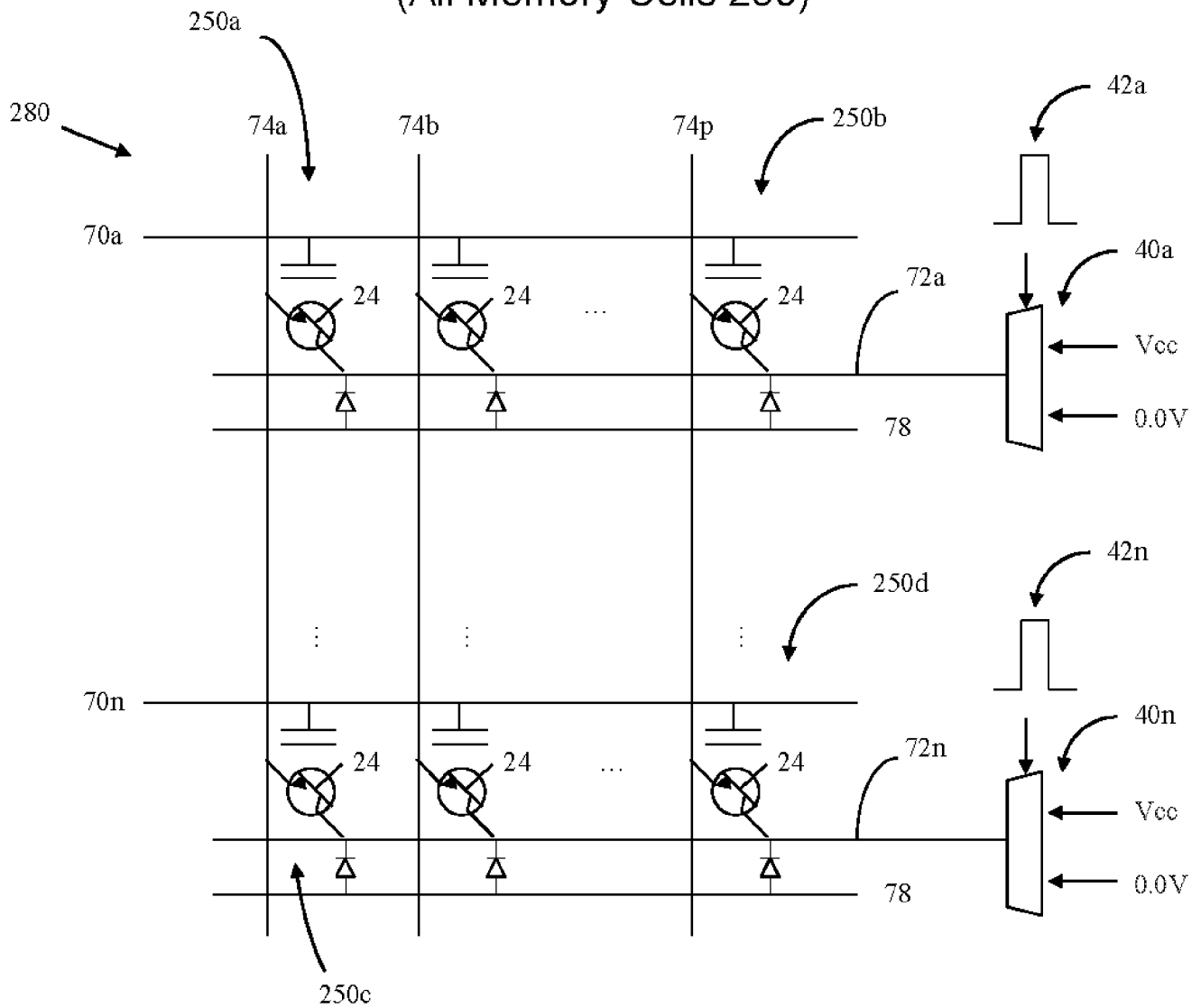


FIG. 38B

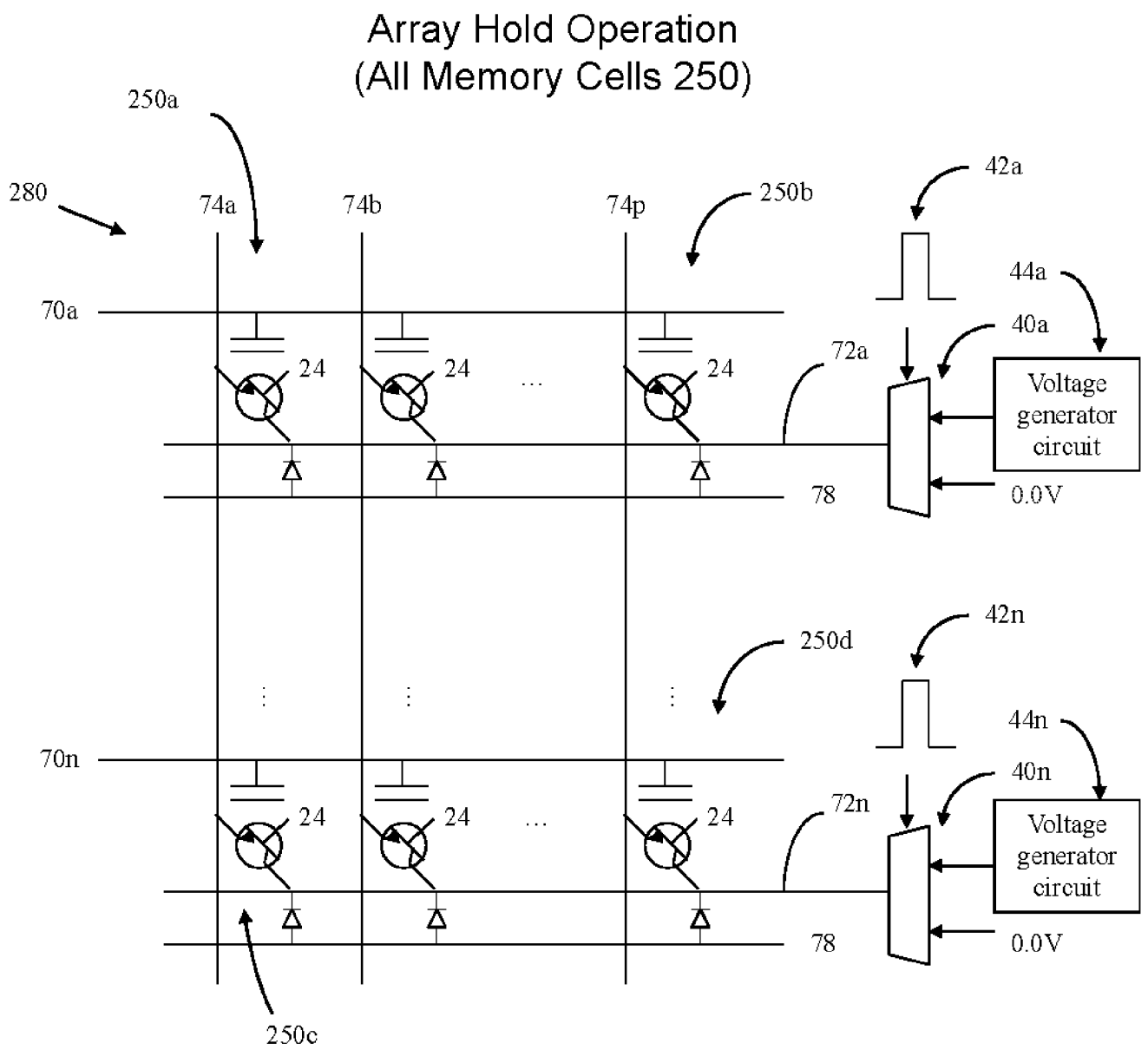


FIG. 38C

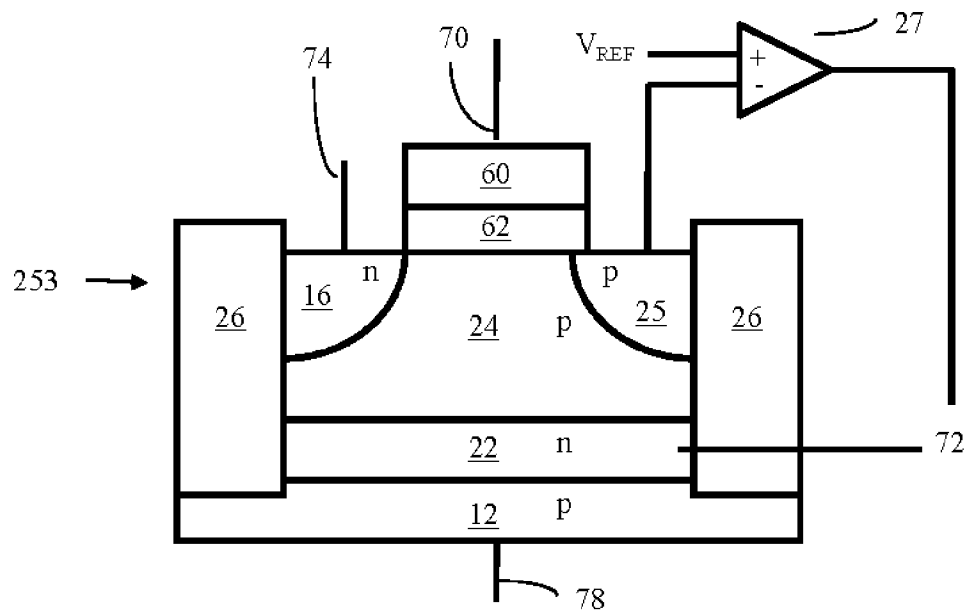


FIG. 38D

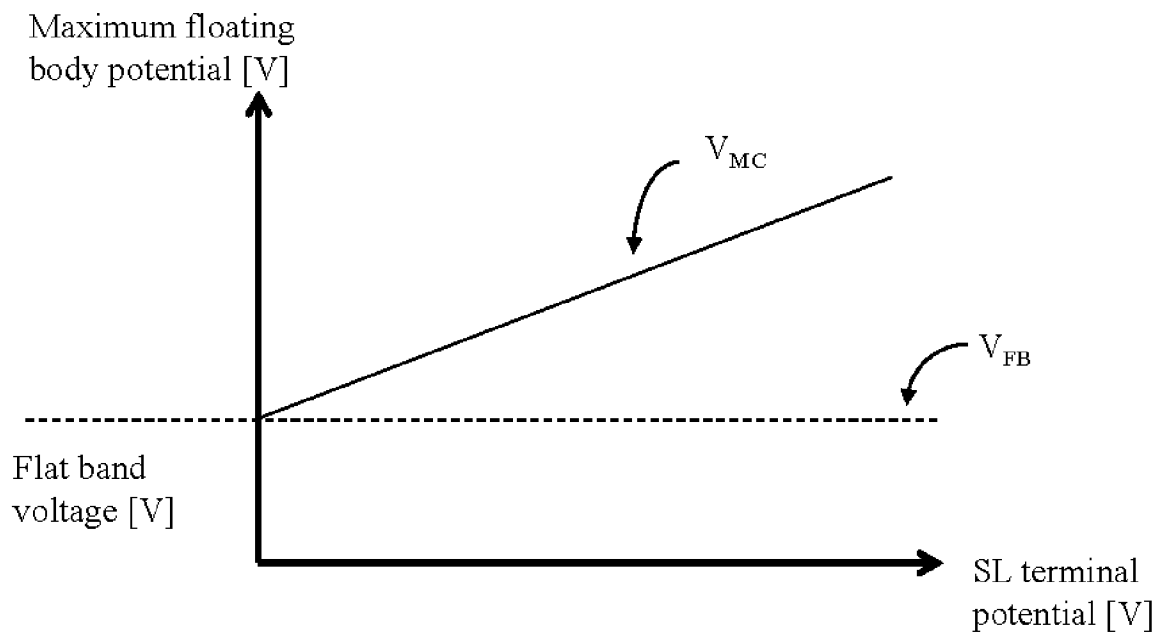


FIG. 39

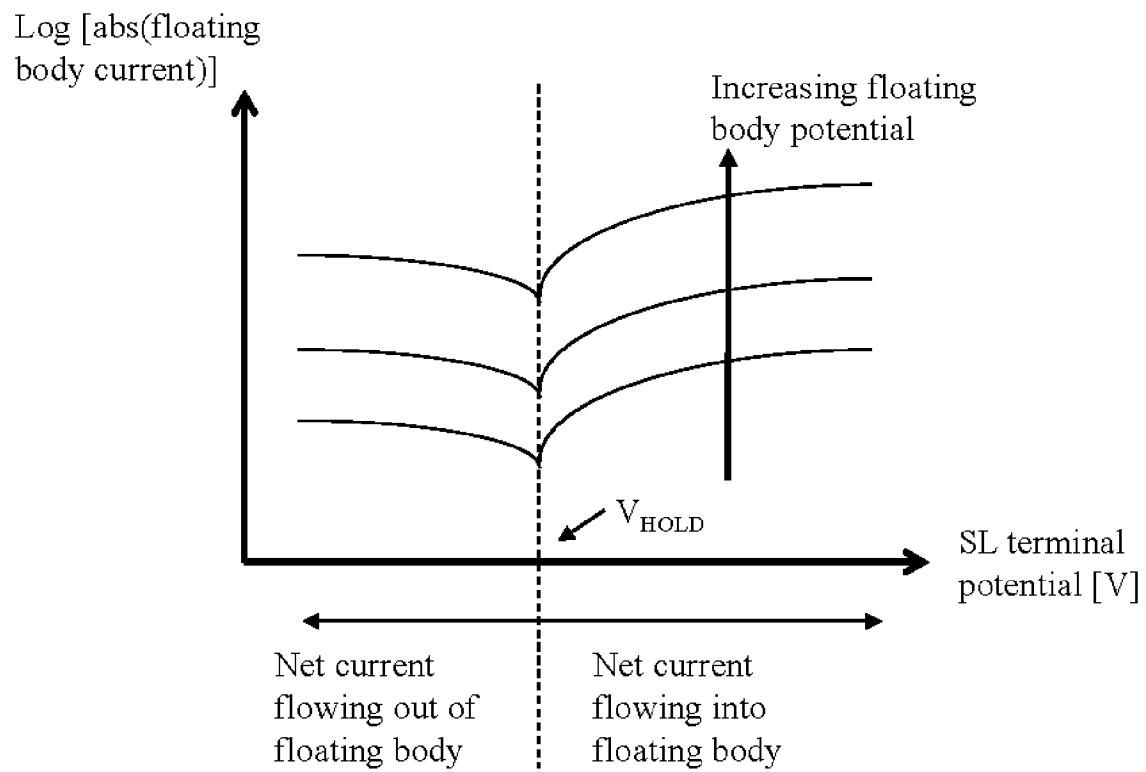


FIG. 40

Read Operation (Memory Cell 250a)

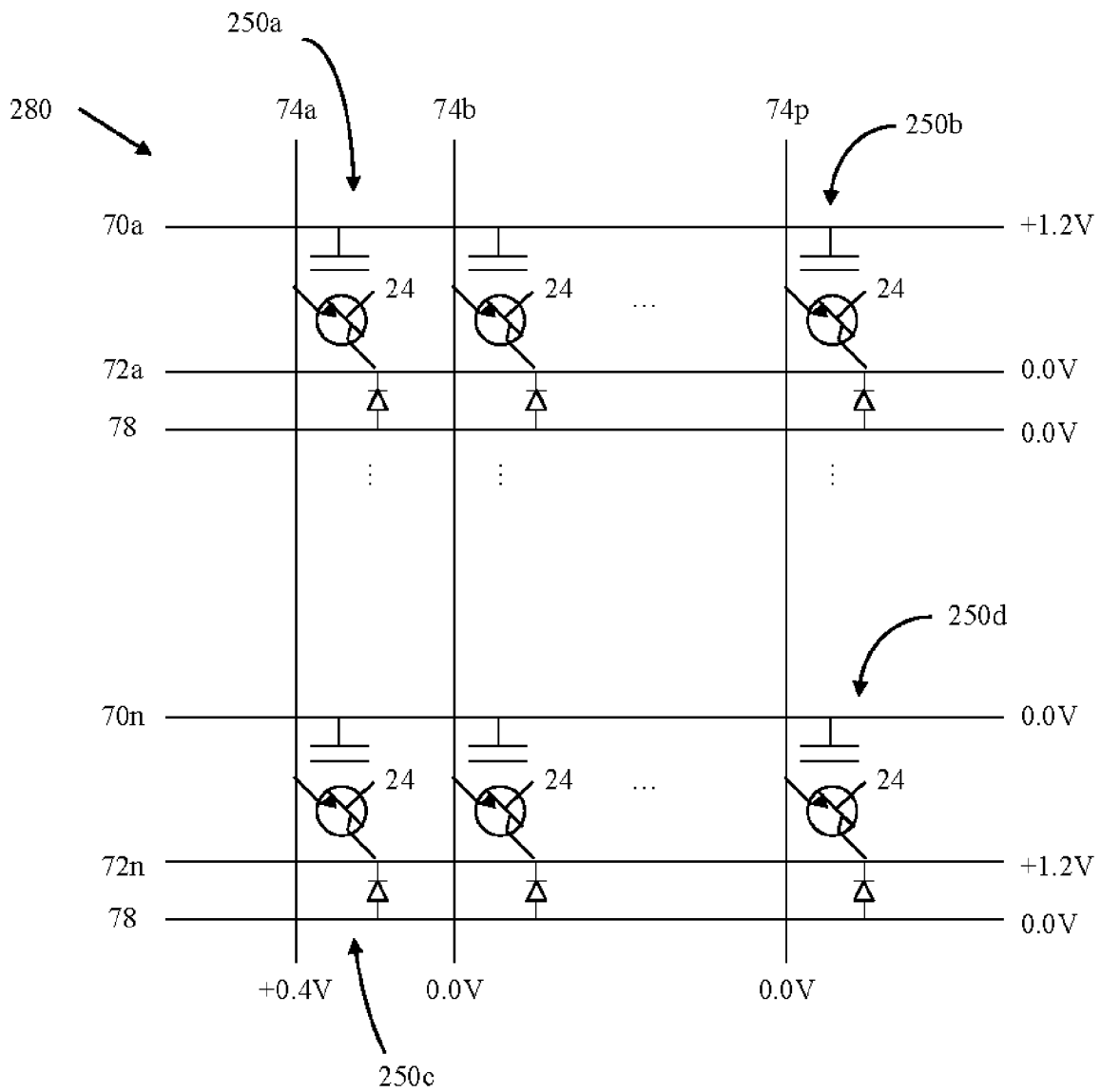


FIG. 41

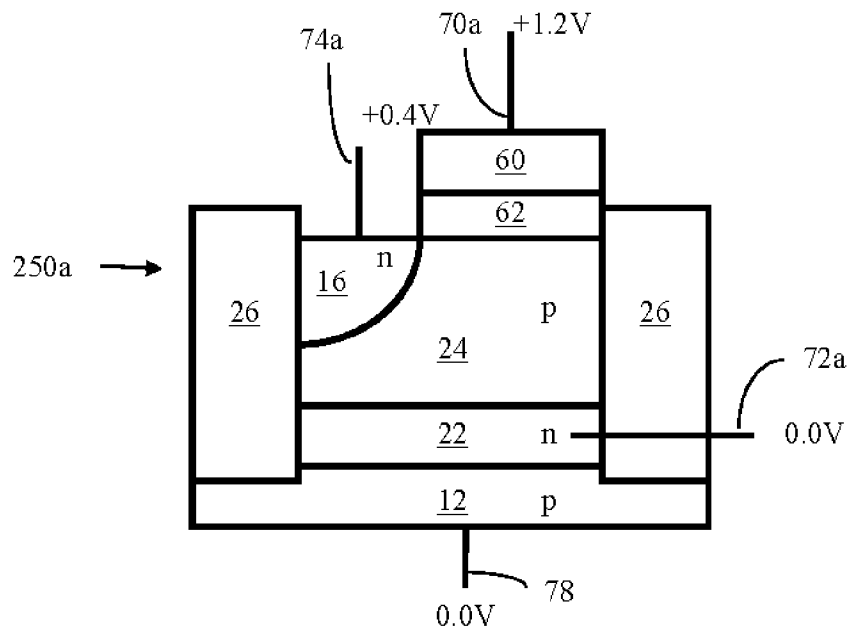


FIG. 42A

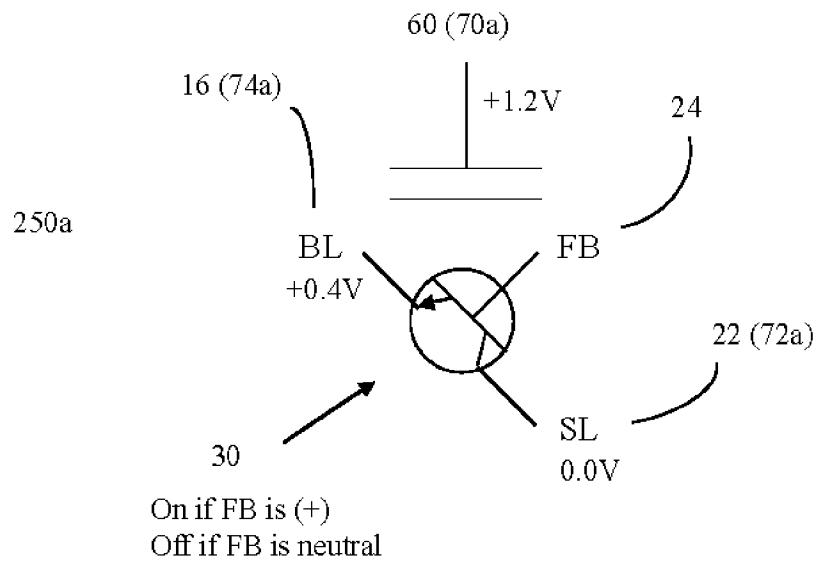


FIG. 42B

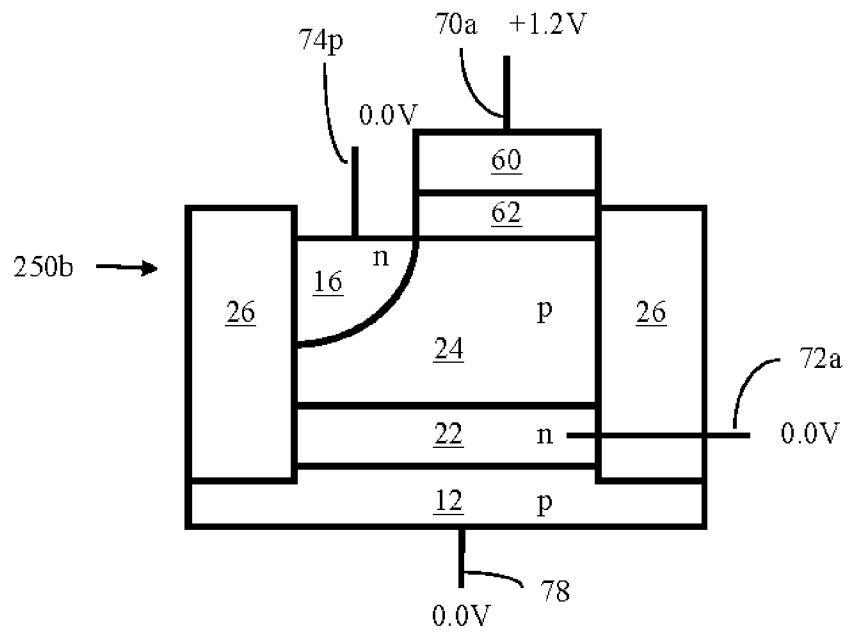


FIG. 42C

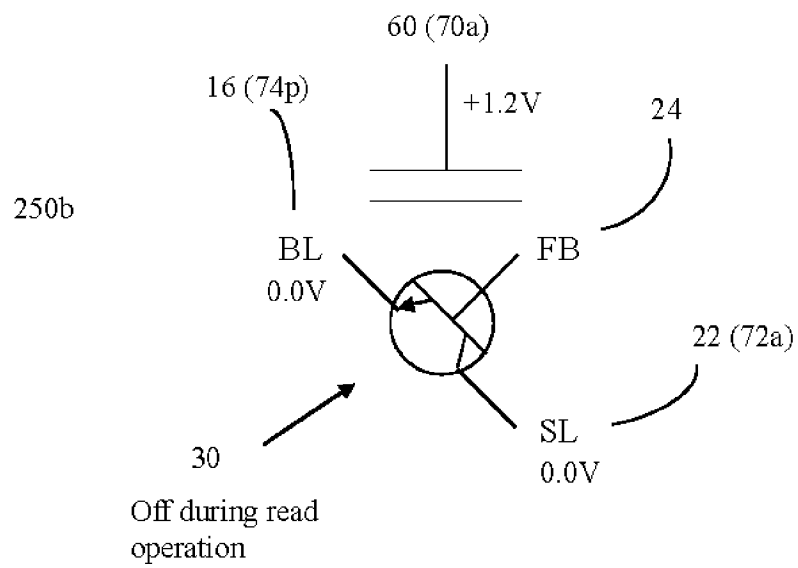


FIG. 42D

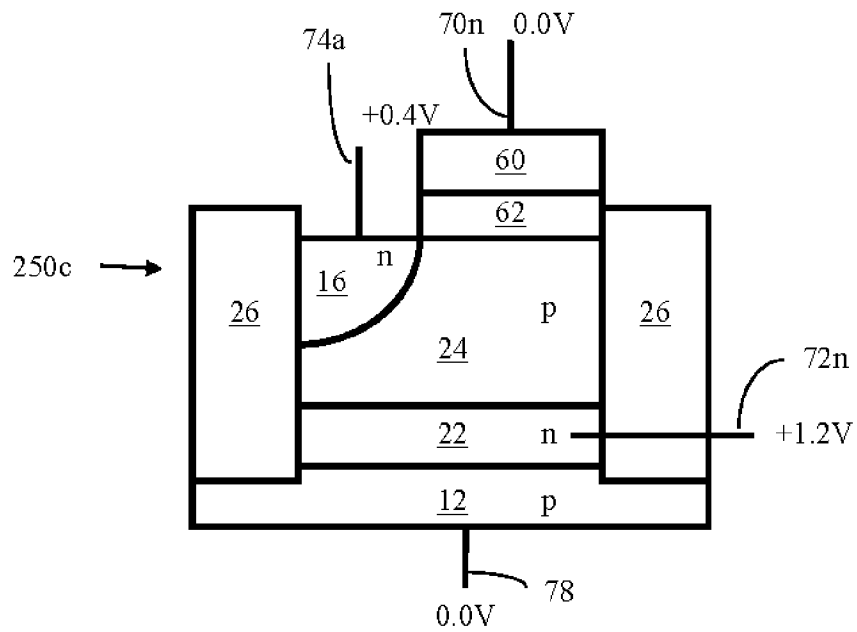


FIG. 42E

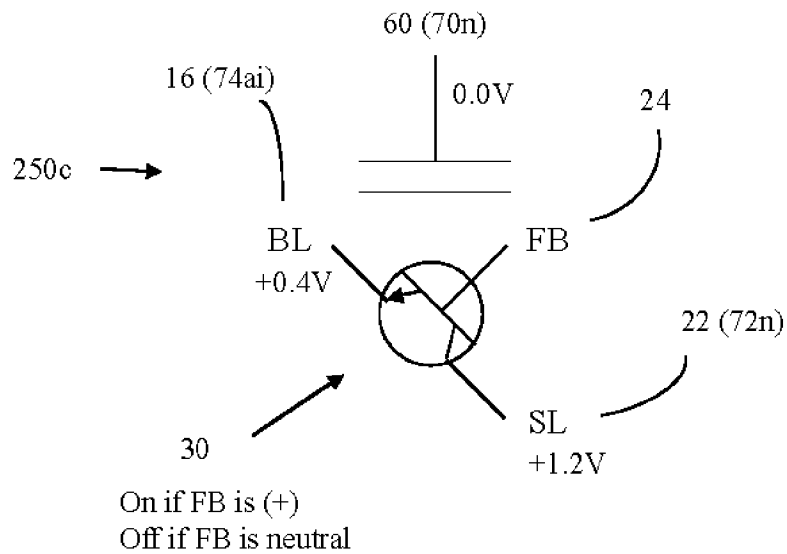


FIG. 42F

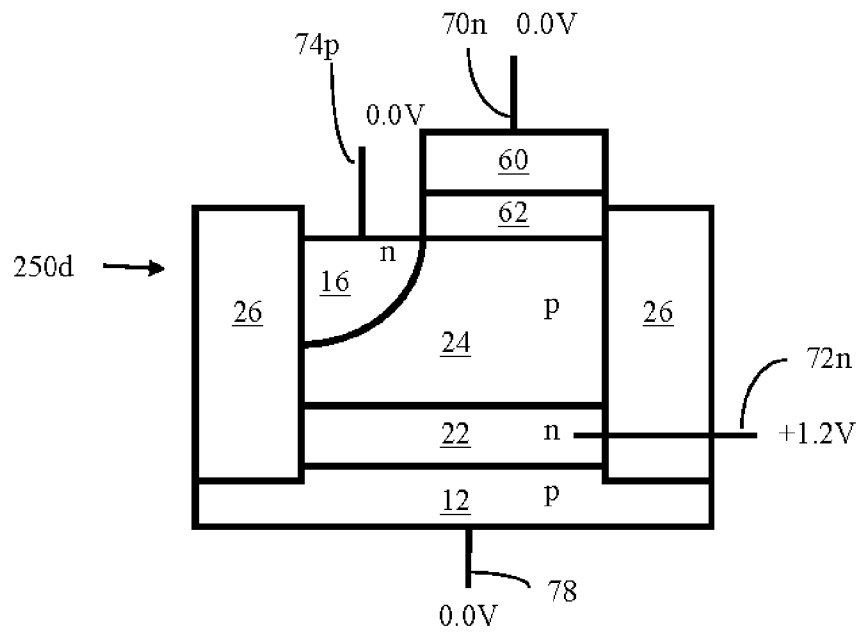


FIG. 42G

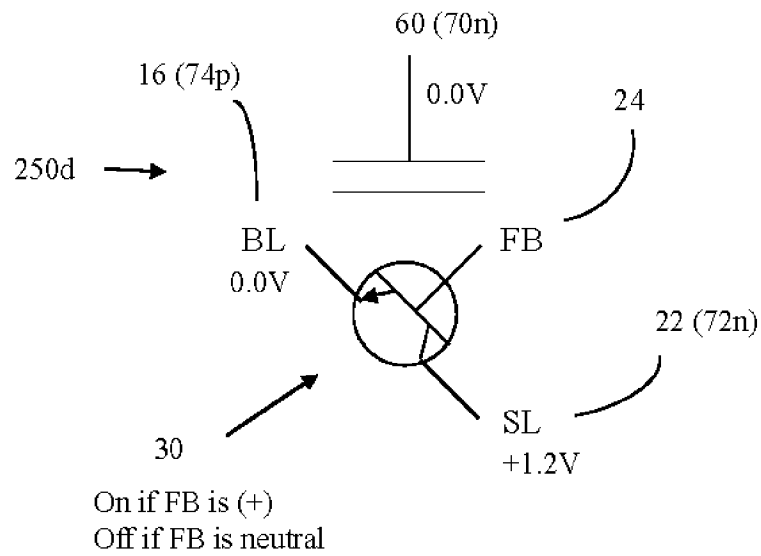


FIG.42H

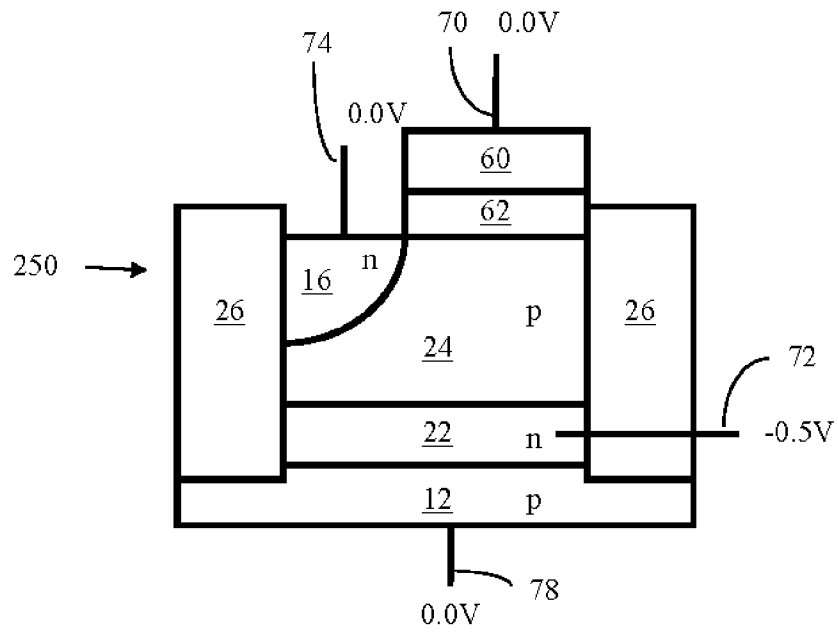


FIG. 43A

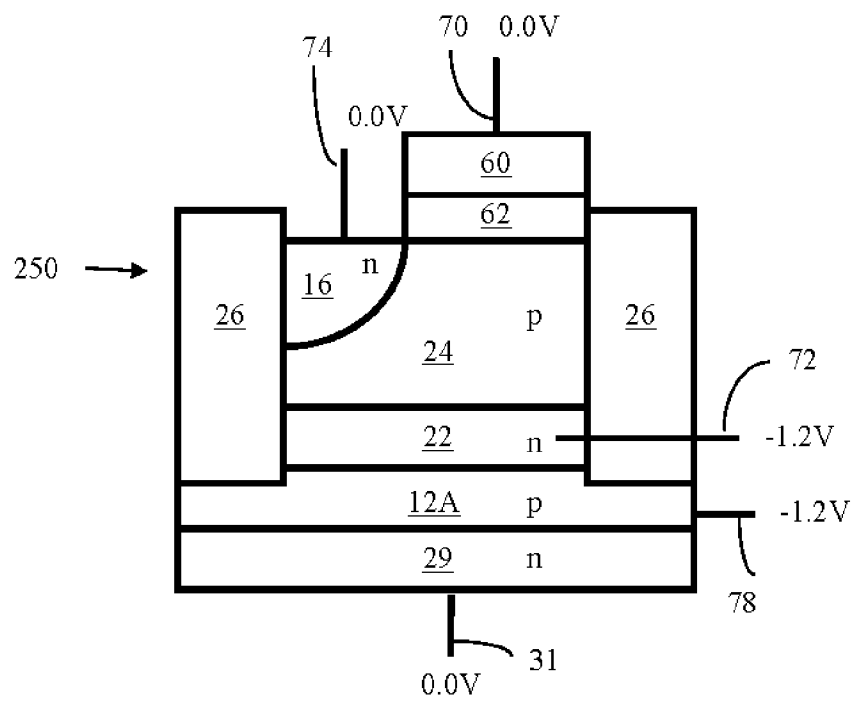


FIG. 43B

Row Write Logic-0 Operation (Memory Cells 250a and 250b)

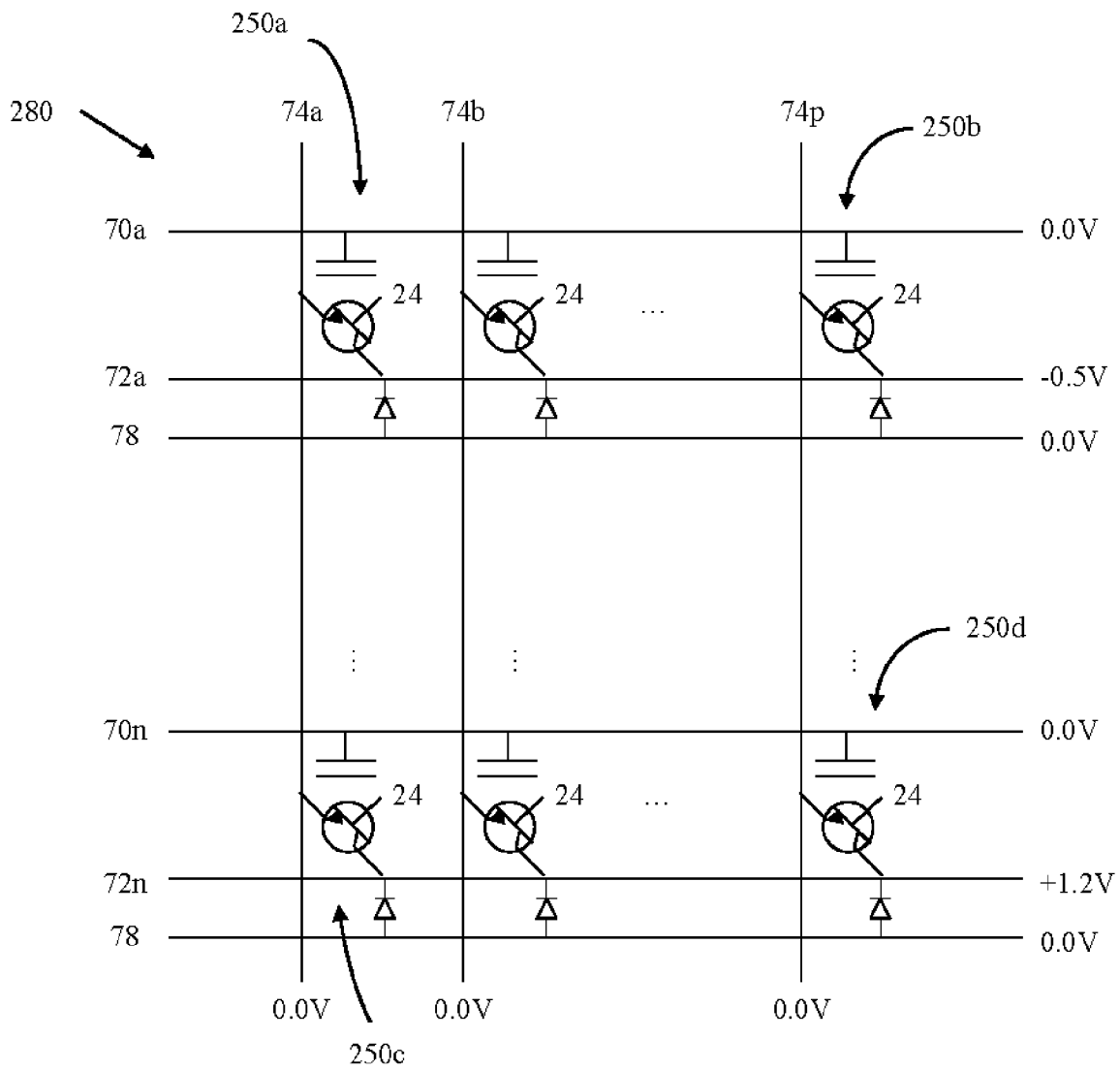
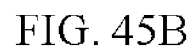
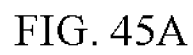


FIG. 44



Column Write Logic-0 Operation (Memory Cells 250a and 250c)

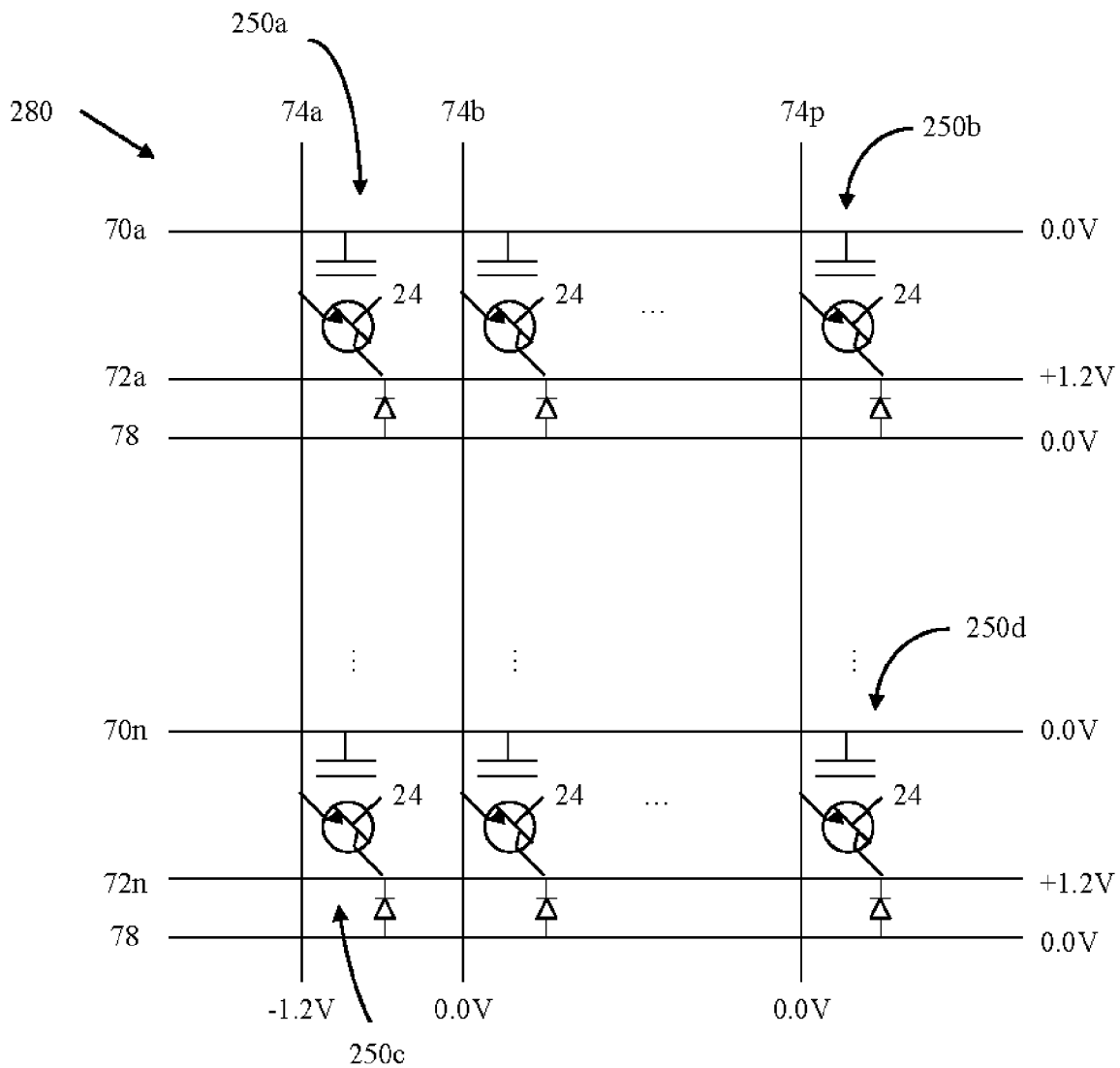


FIG. 46

Write Logic-0 Operation (Single Memory Cell 250a)

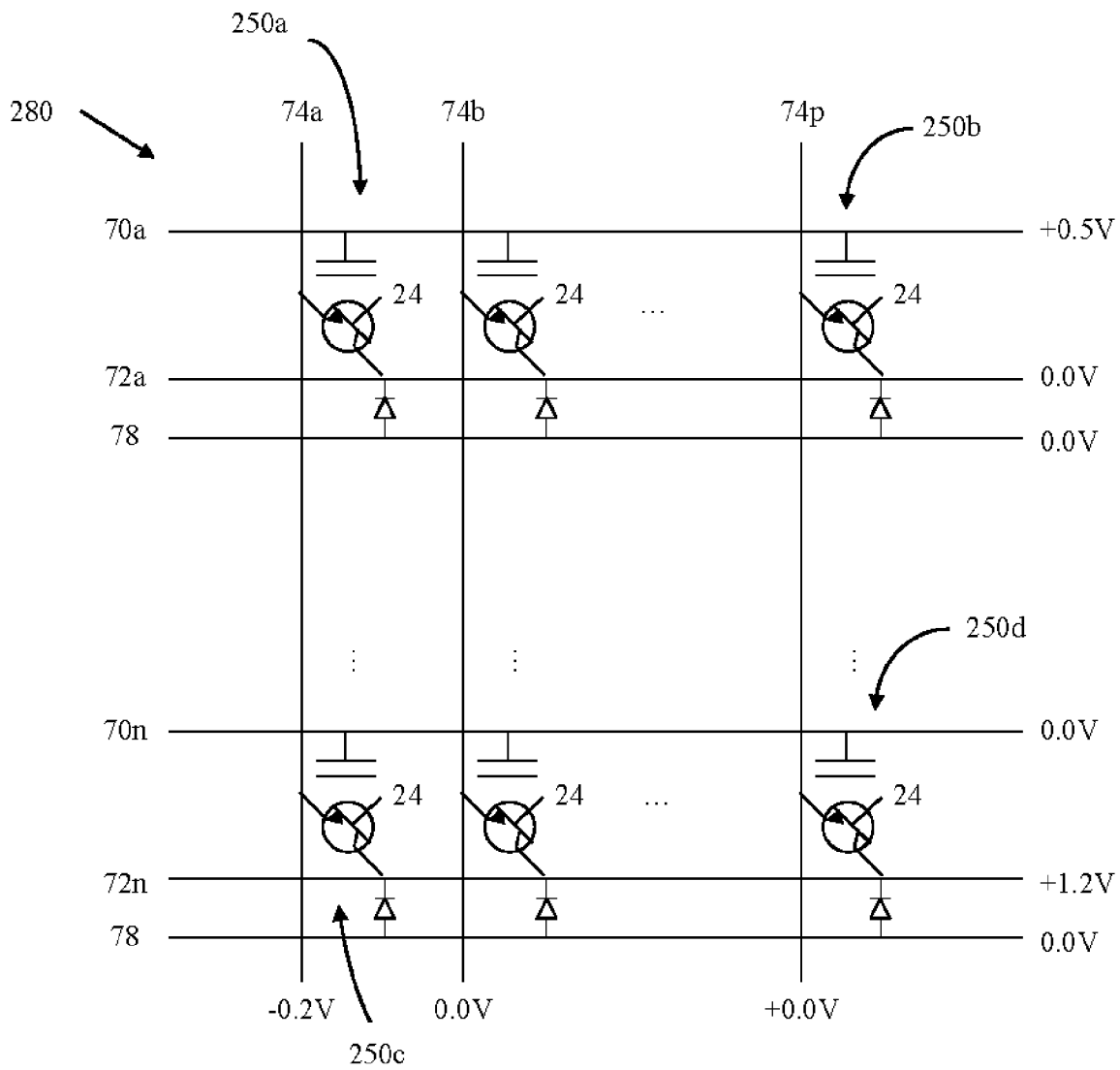


FIG. 47

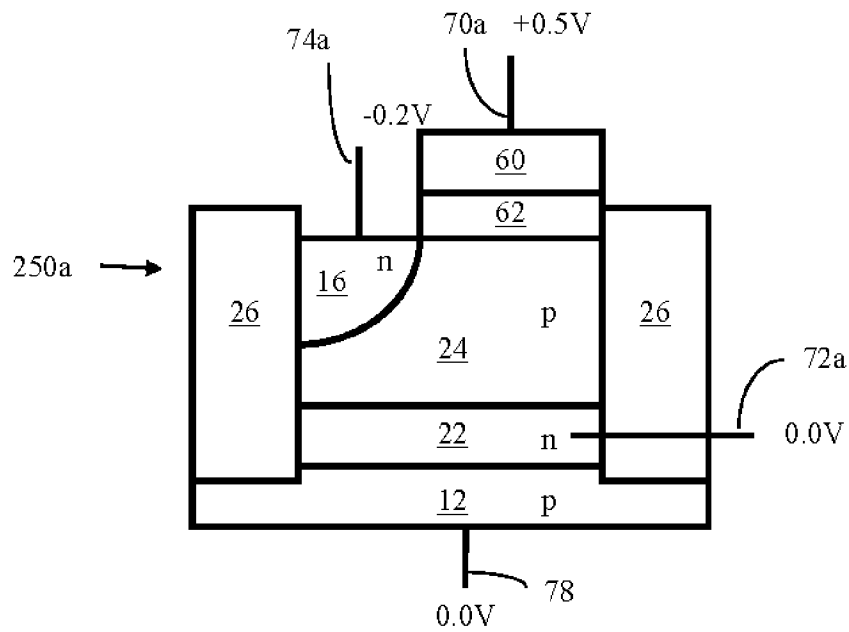


FIG. 48A

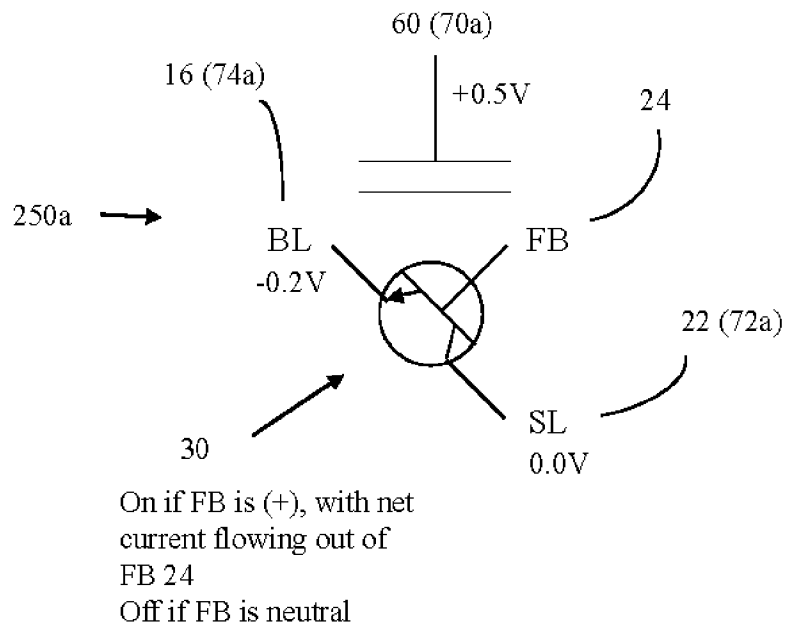


FIG. 48B

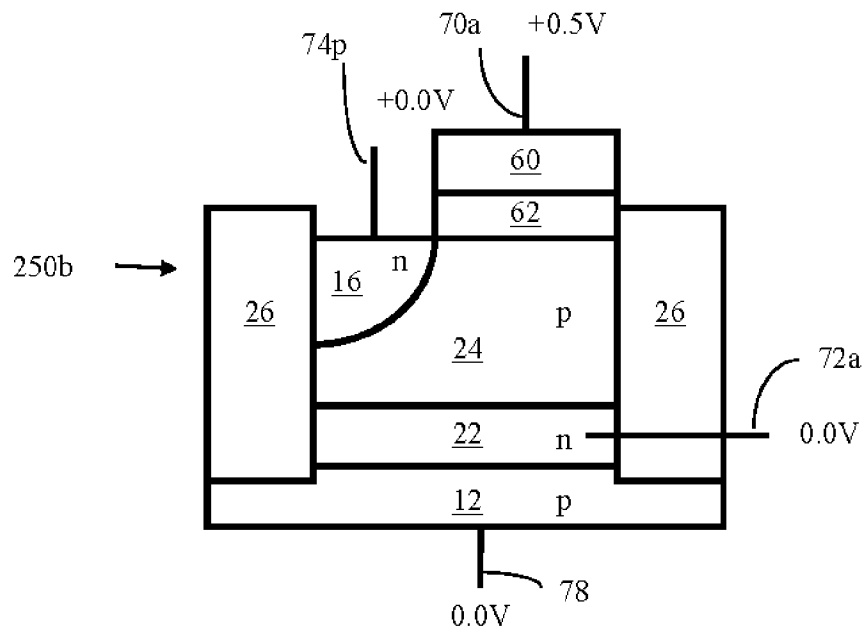


FIG. 48C

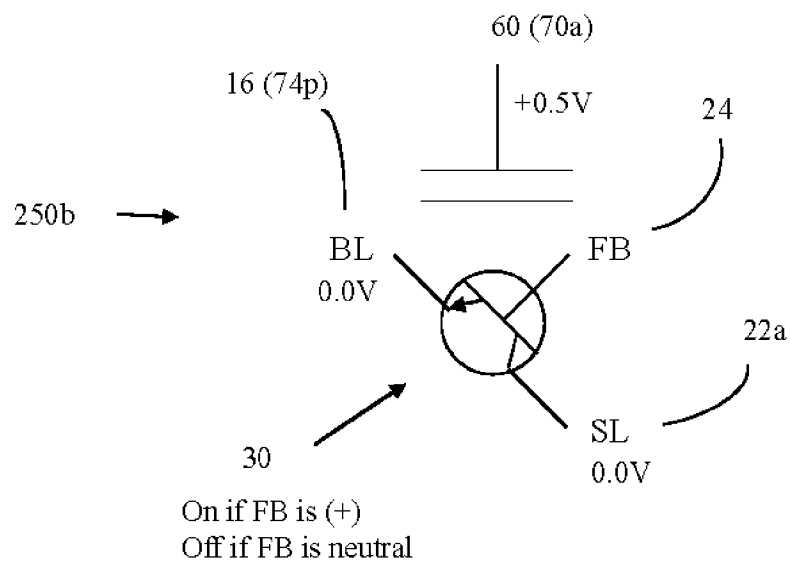


FIG. 48D

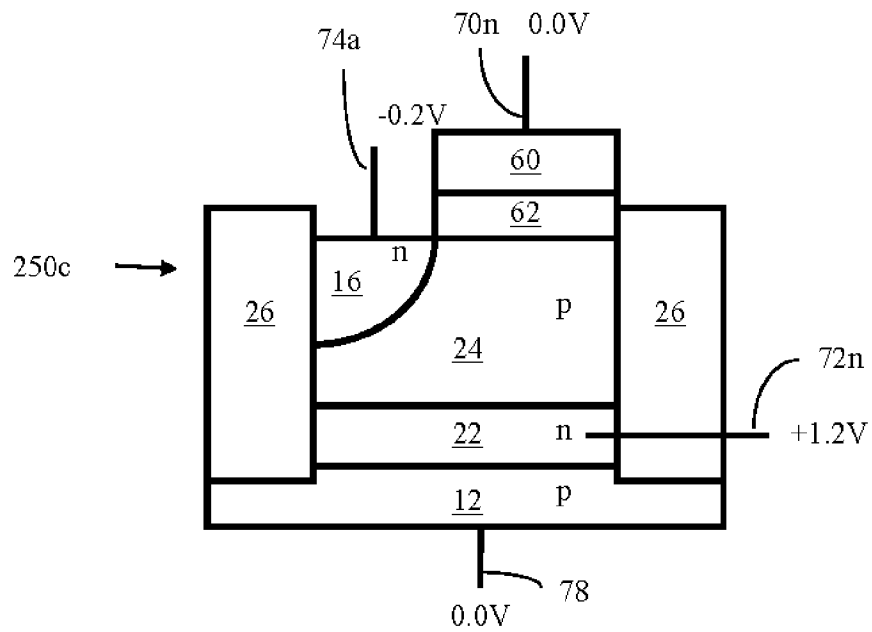
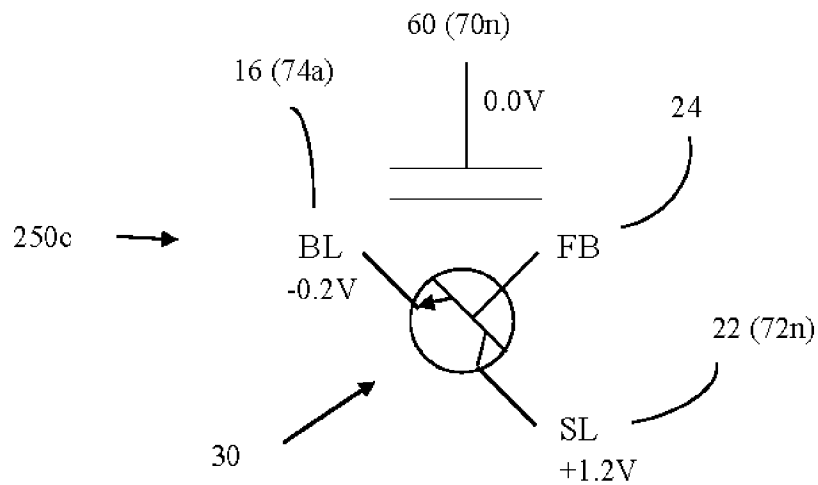


FIG. 48E



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 48F

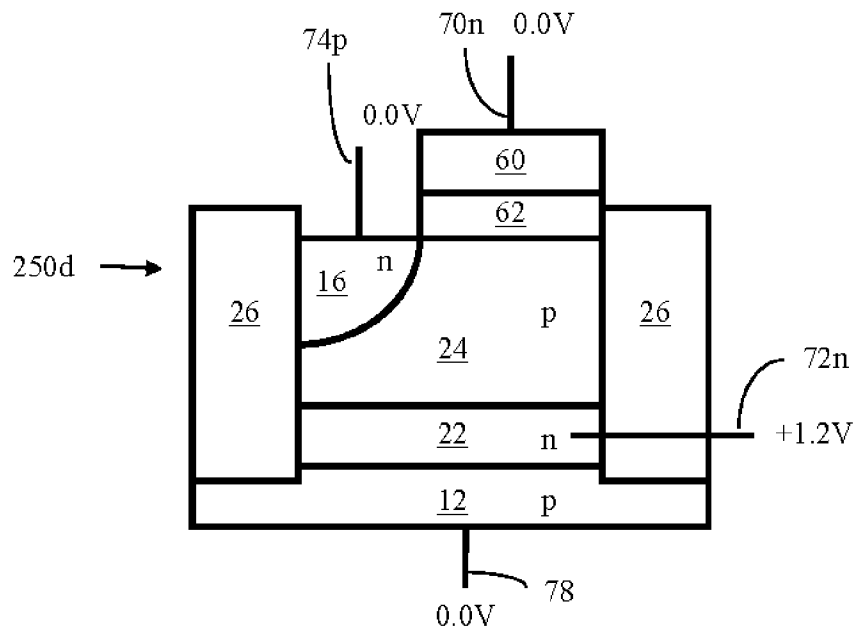


FIG. 48G

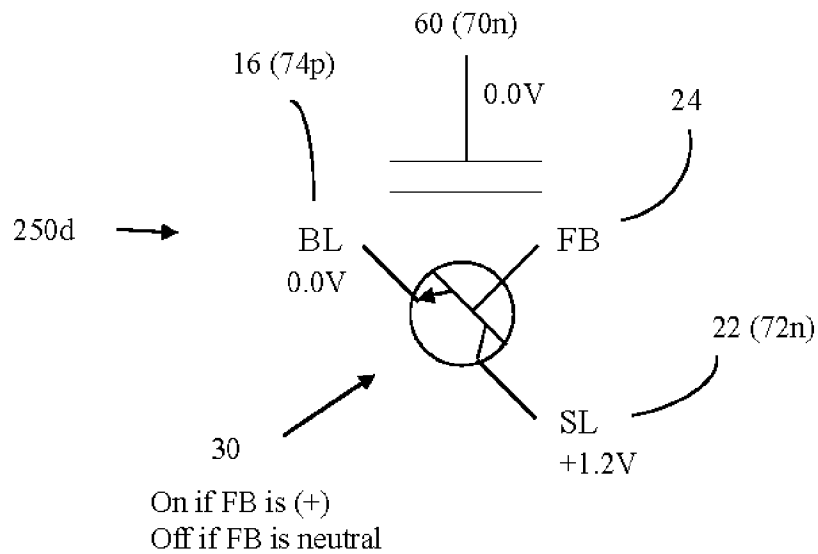


FIG. 48H

The diagram illustrates a grid-like structure of a semiconductor device. It features several horizontal lines representing different voltage levels: -1.2V, 0.0V, +1.2V, and 0.0V. Vertical lines represent individual columns or channels, labeled 74a, 74b, ..., 74p, ..., 74n. Each column contains a series of components: a top terminal (e.g., 70a, 70n), a central component (labeled 24) connected to a middle line (e.g., 72a, 72n), and a bottom terminal (labeled 78). The components are connected to the middle line via diagonal lines. Arrows indicate specific connections or regions: 250a points to the top connection area, 250b points to the middle connection area, 250c points to the bottom connection area, and 250d points to the bottom connection area.

FIG. 49

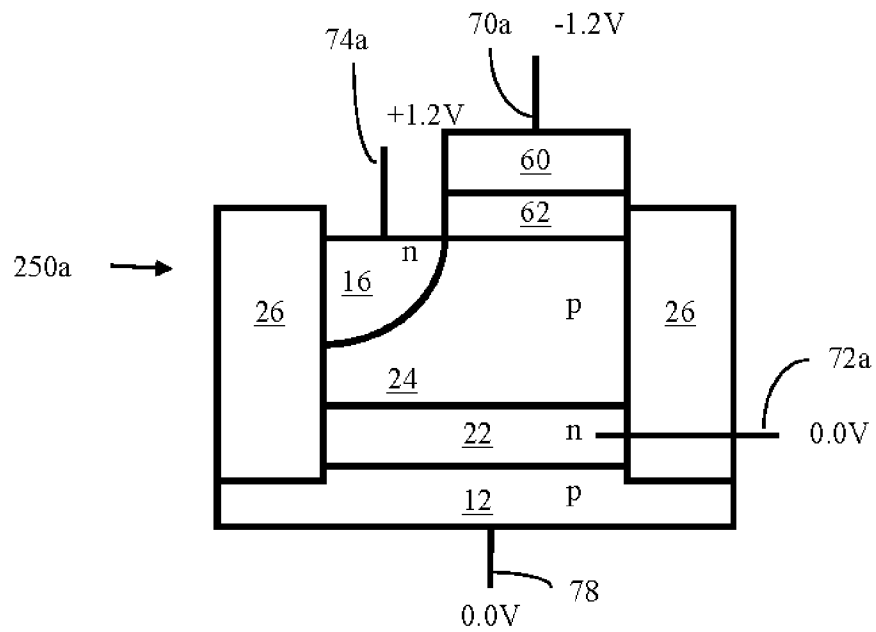


FIG. 50A

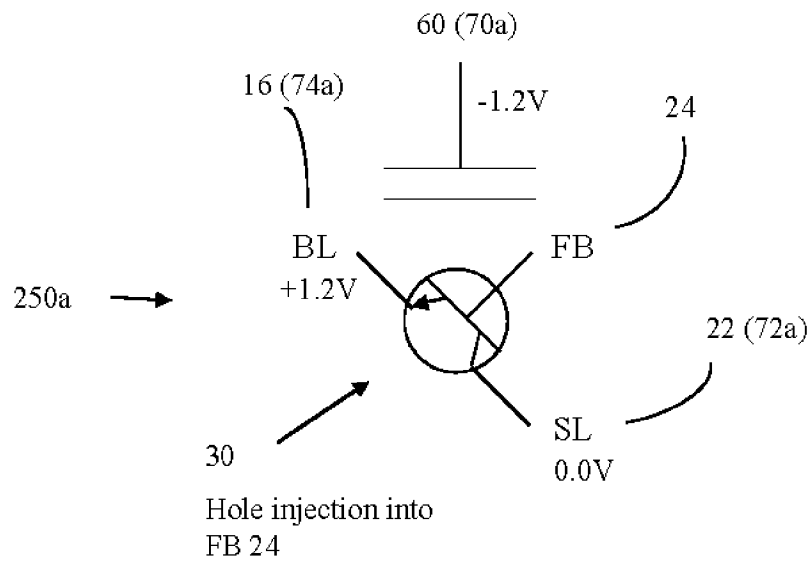


FIG. 50B

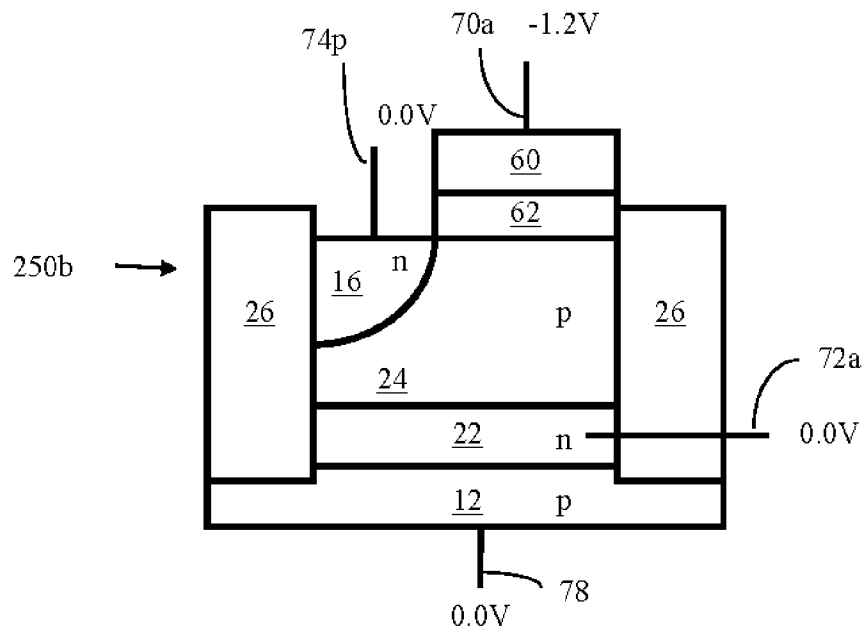


FIG. 50C

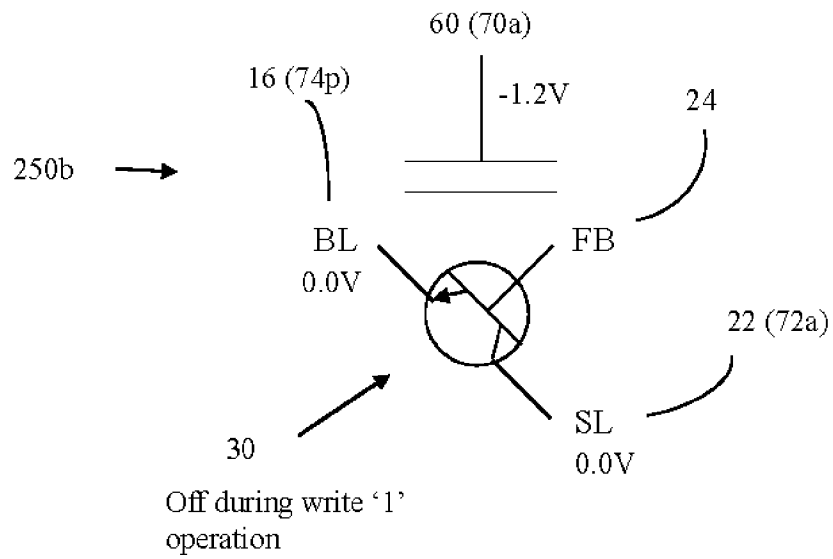


FIG. 50D

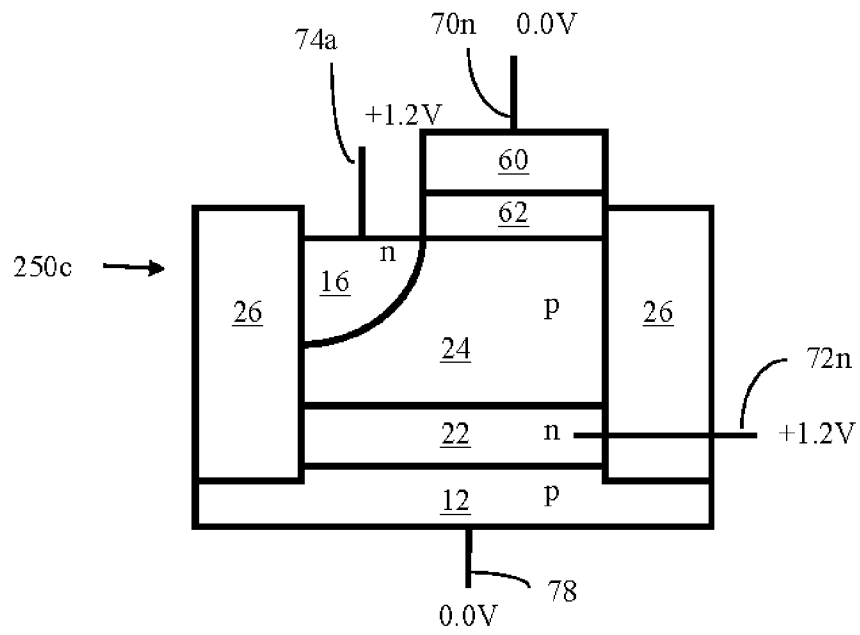


FIG. 50E

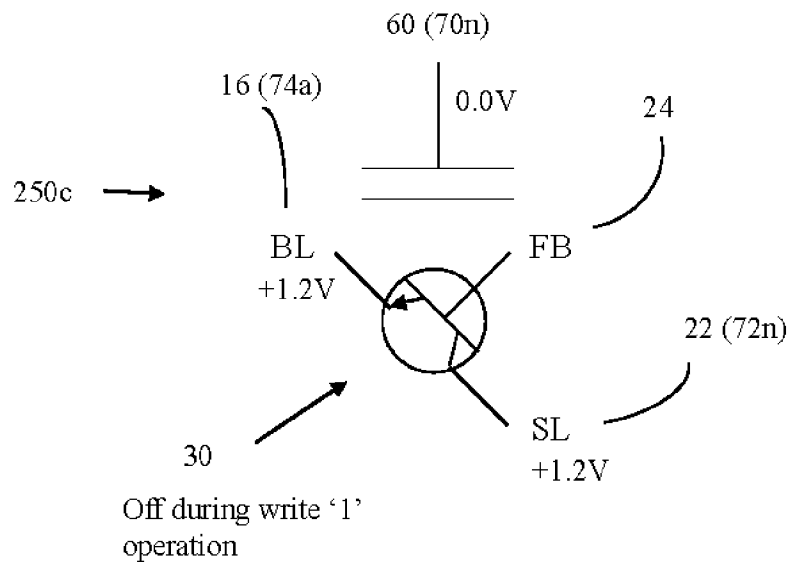


FIG. 50F

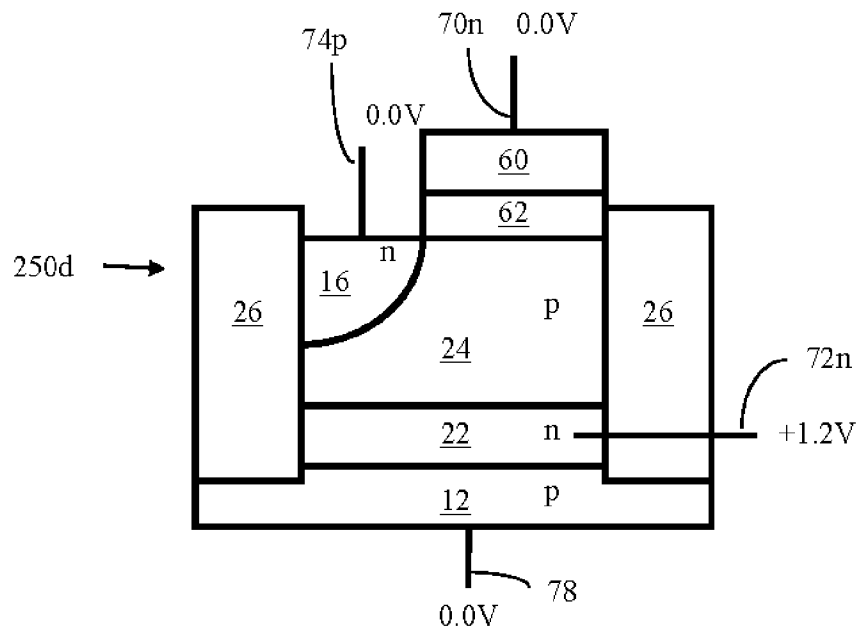


FIG. 50G

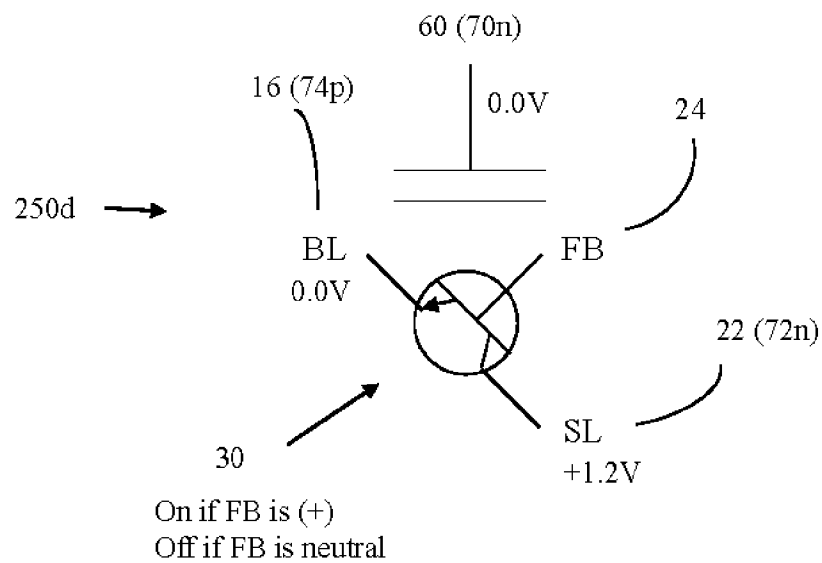


FIG. 50H

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 250a)

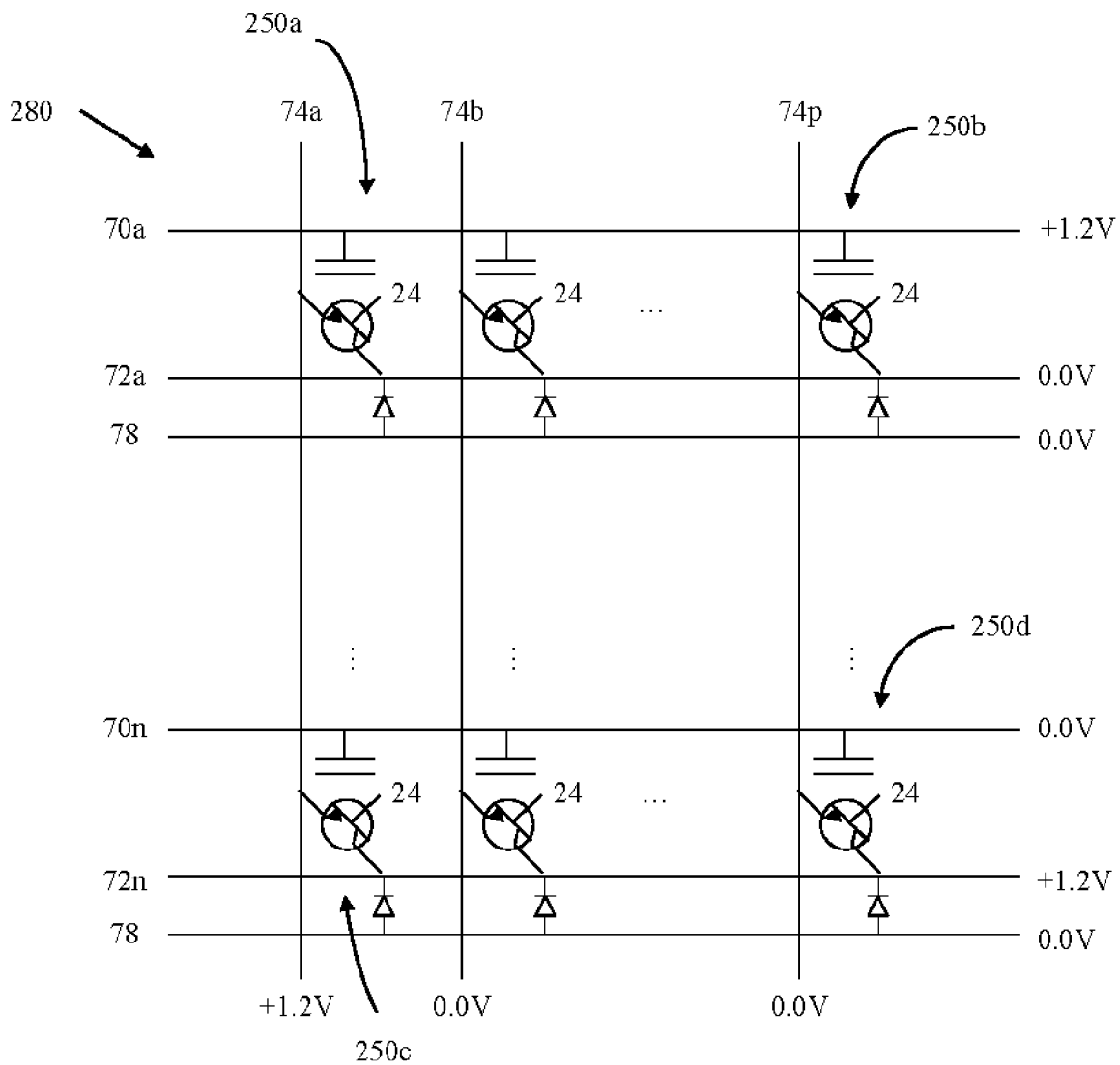


FIG. 51

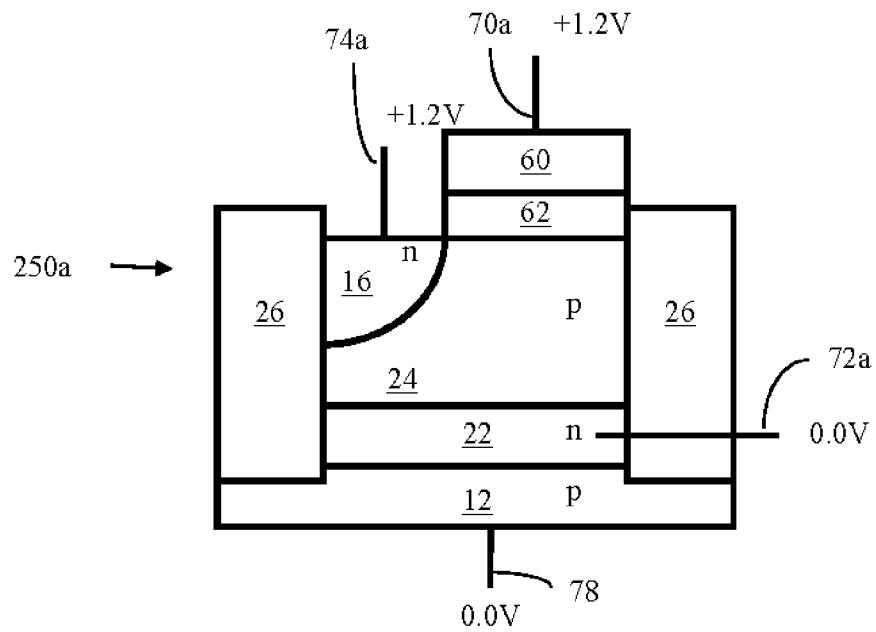


FIG. 52A

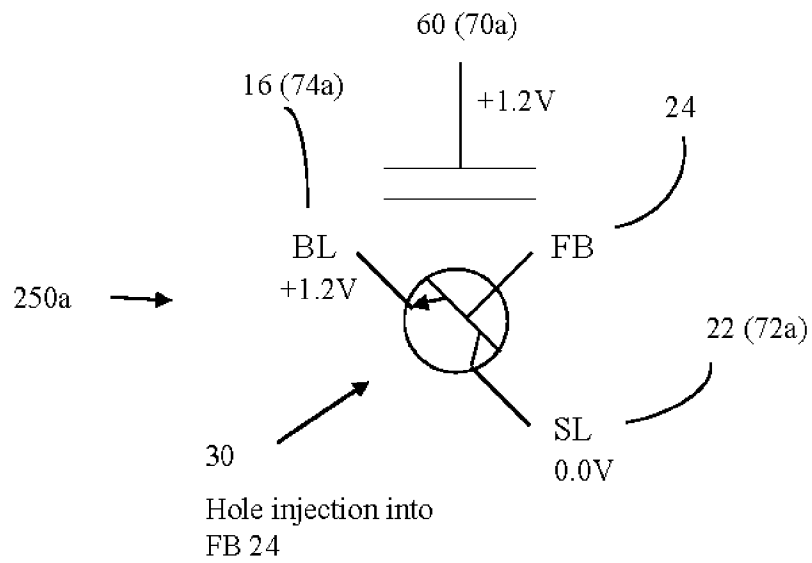


FIG. 52B

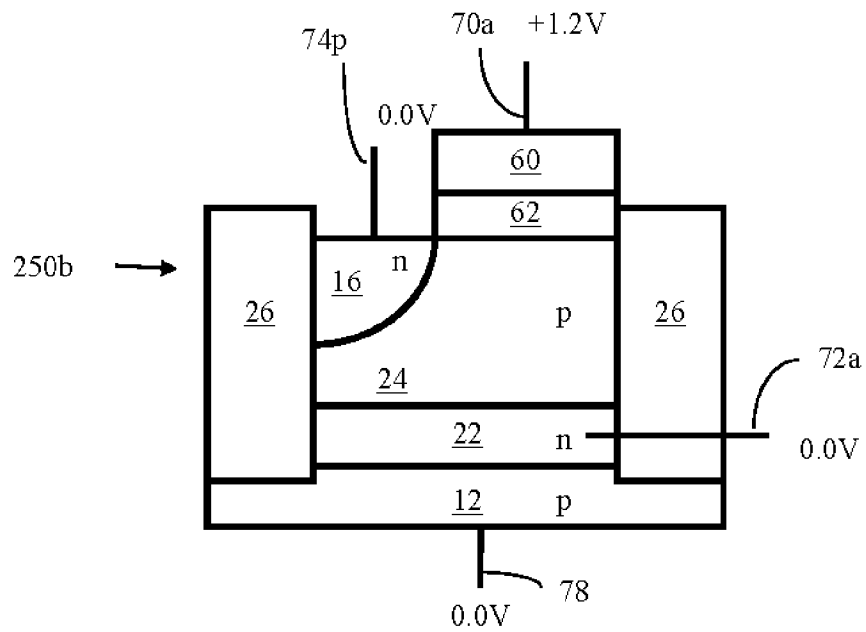


FIG. 52C

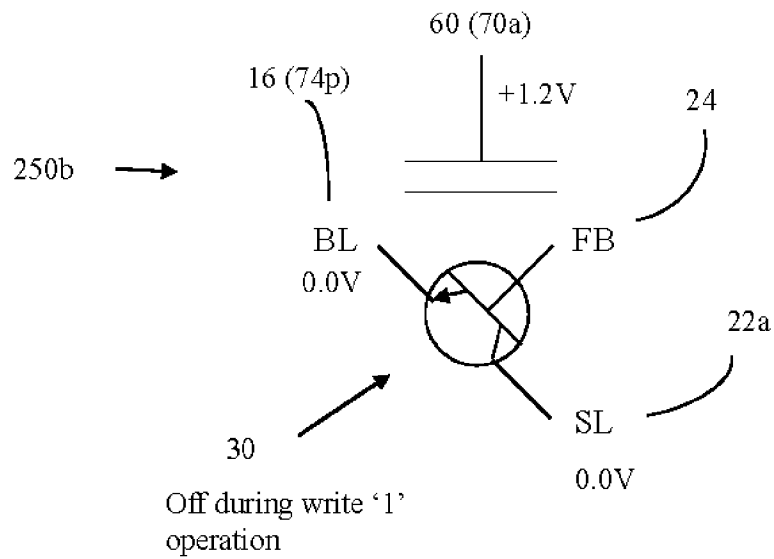


FIG. 52D

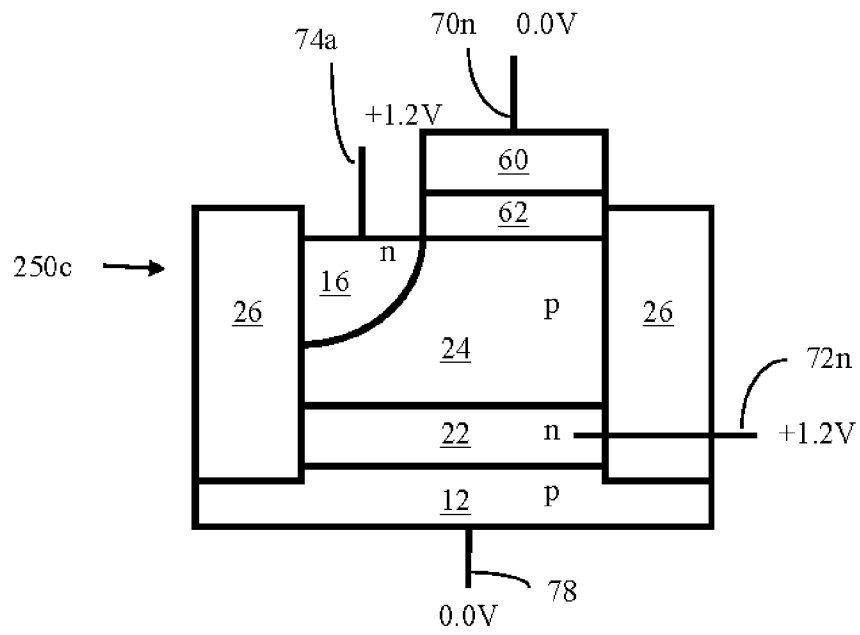


FIG. 52E

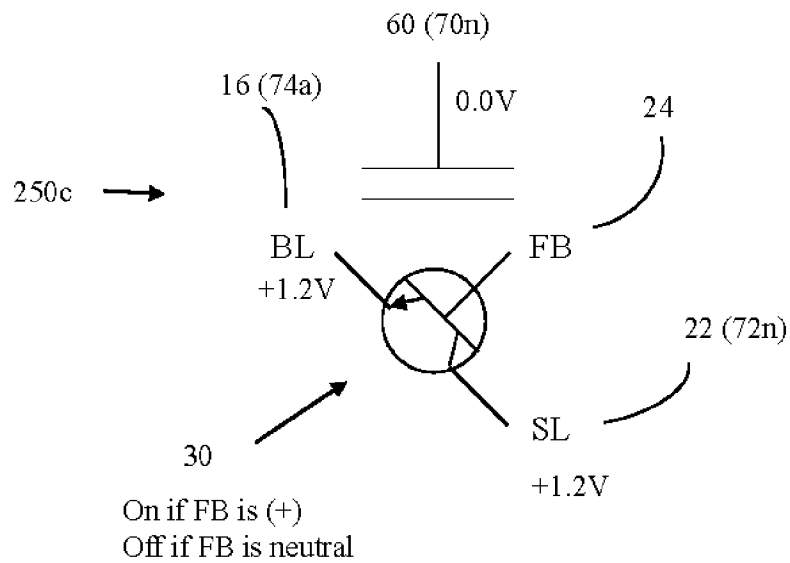


FIG. 52F

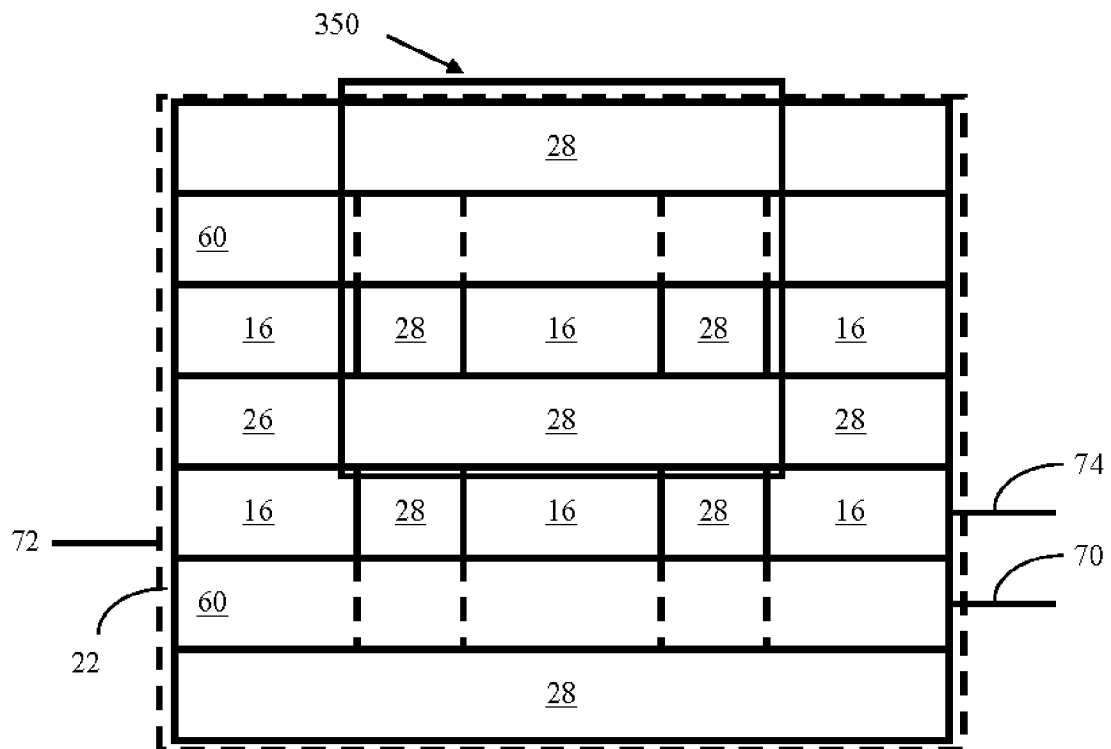


FIG. 53A

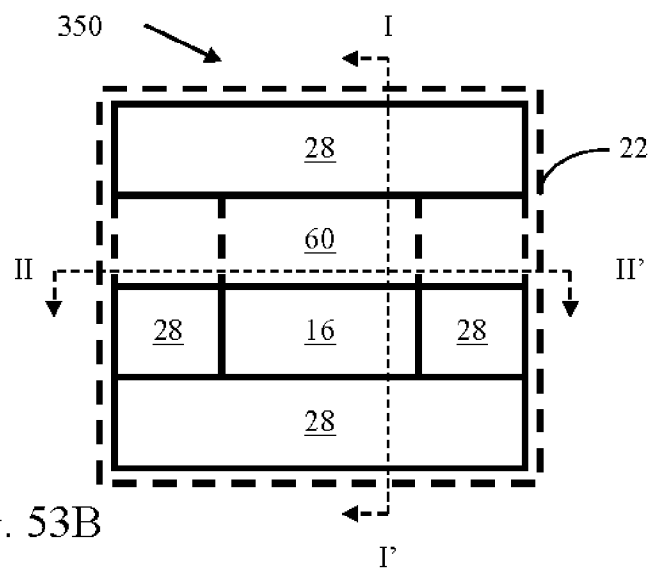


FIG. 53B

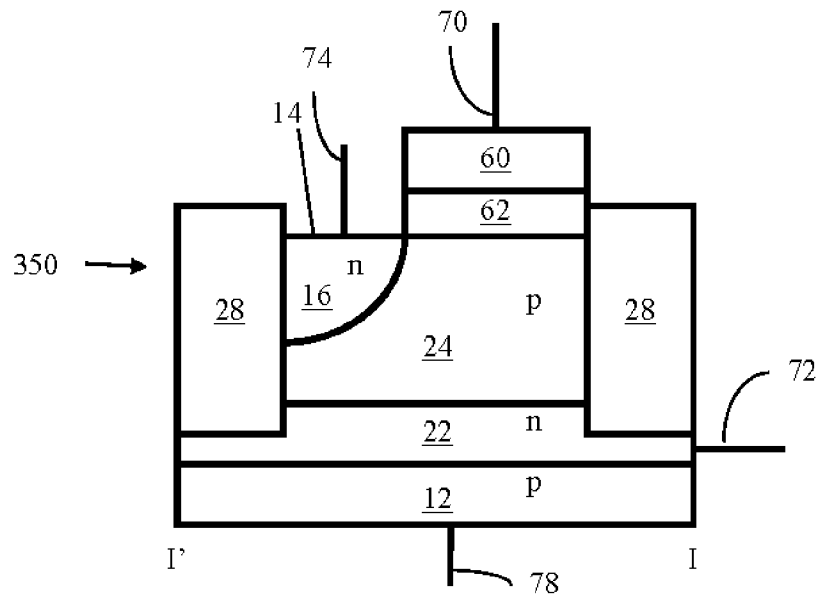


FIG. 53C

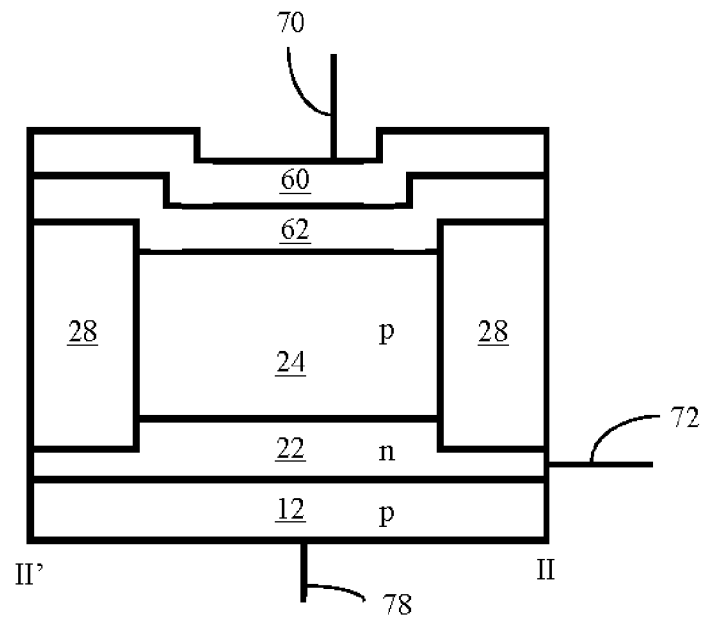


FIG. 53D

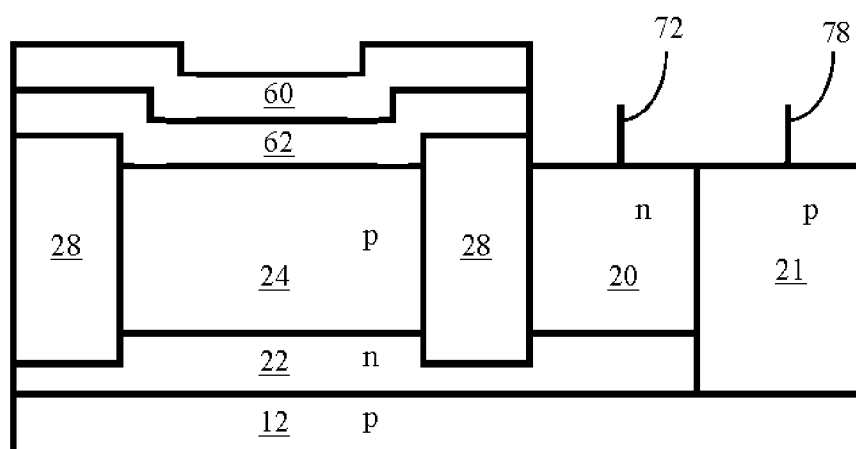


FIG. 53E

Exemplary Memory Array 380 with Representative
Memory Cells 350a, 350b, 350c and 350d

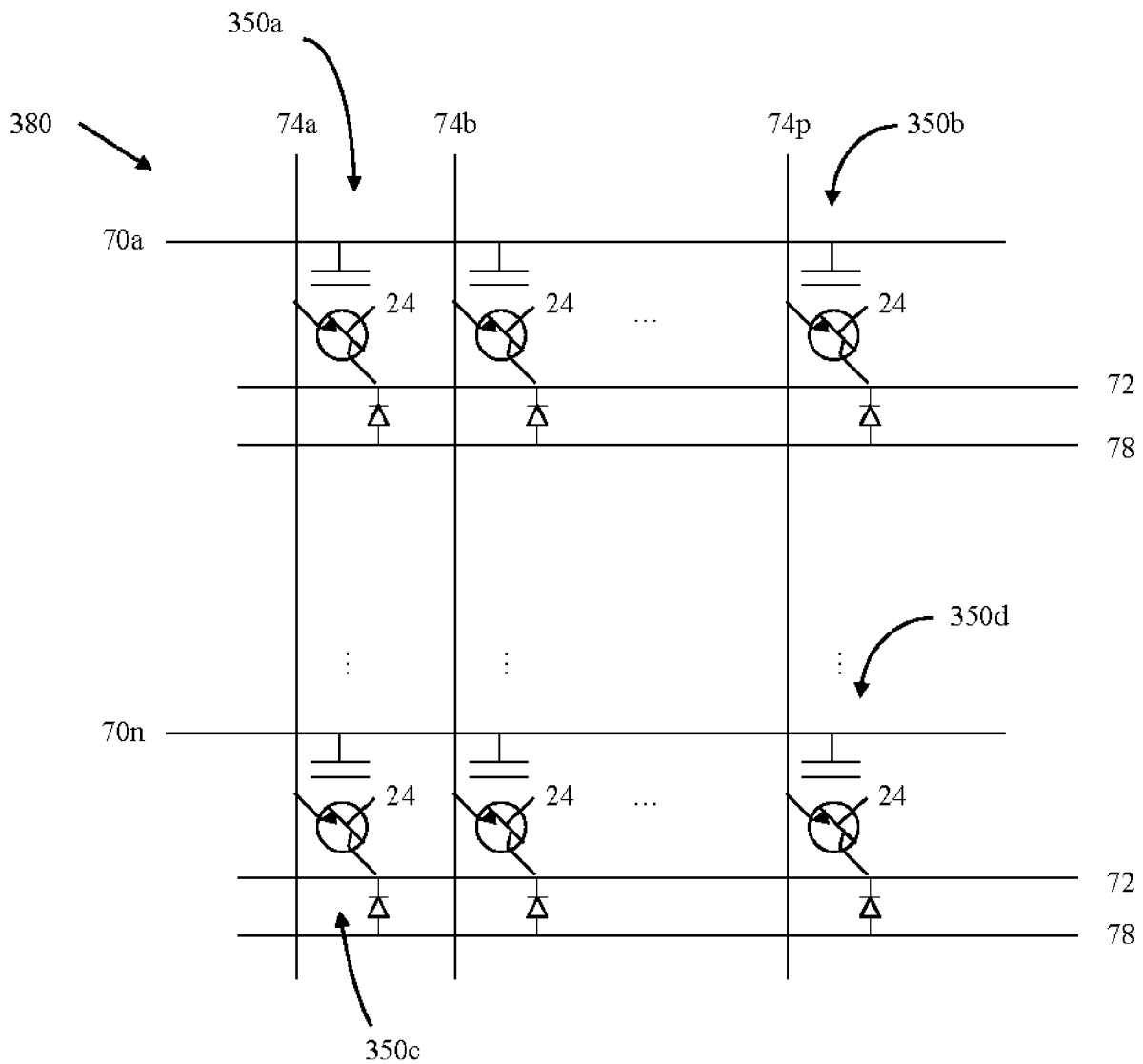


FIG. 54A

Array Hold Operation (All Memory Cells 350)

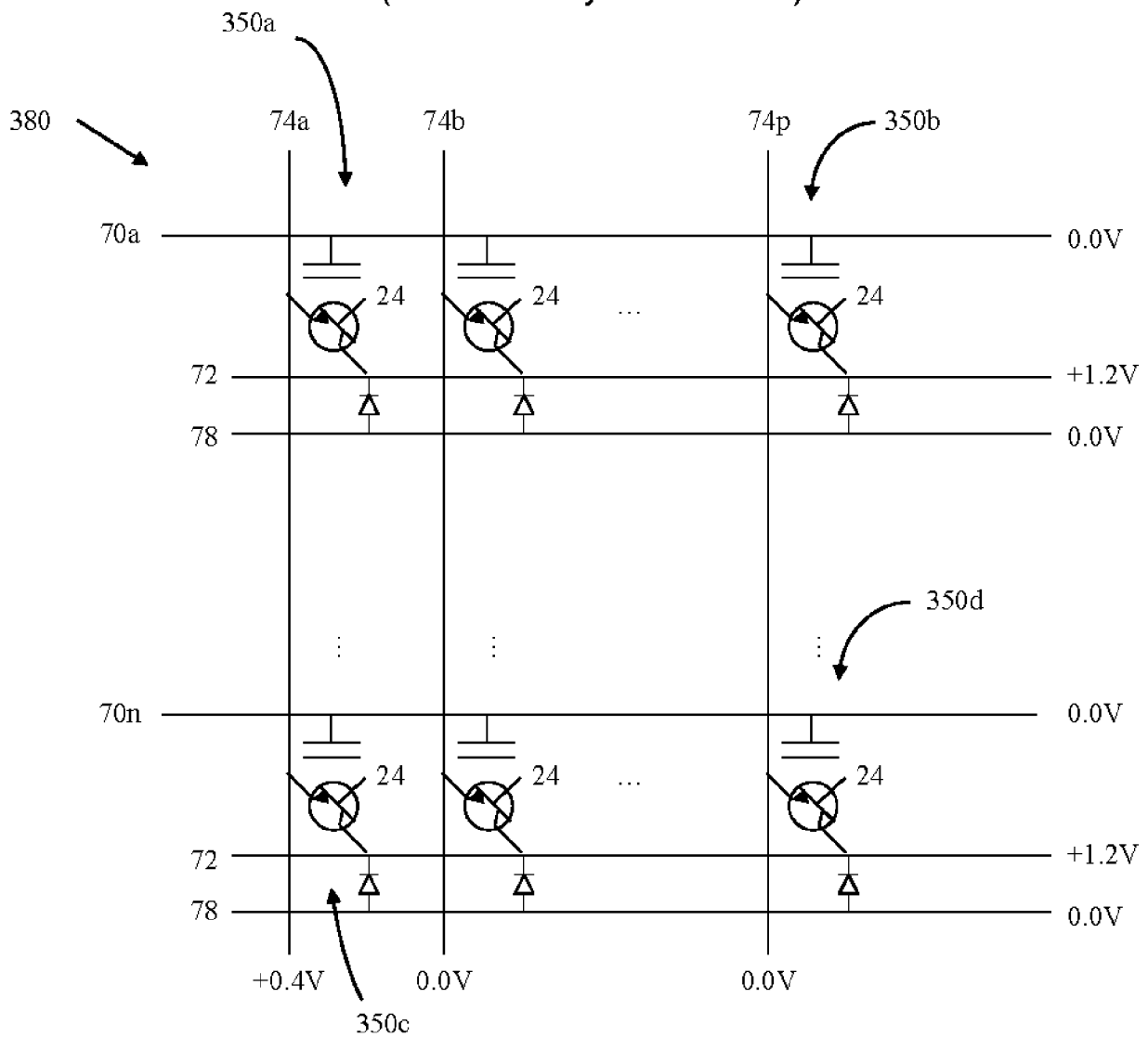


FIG. 54B

Read Operation (Single Memory Cell 350a)

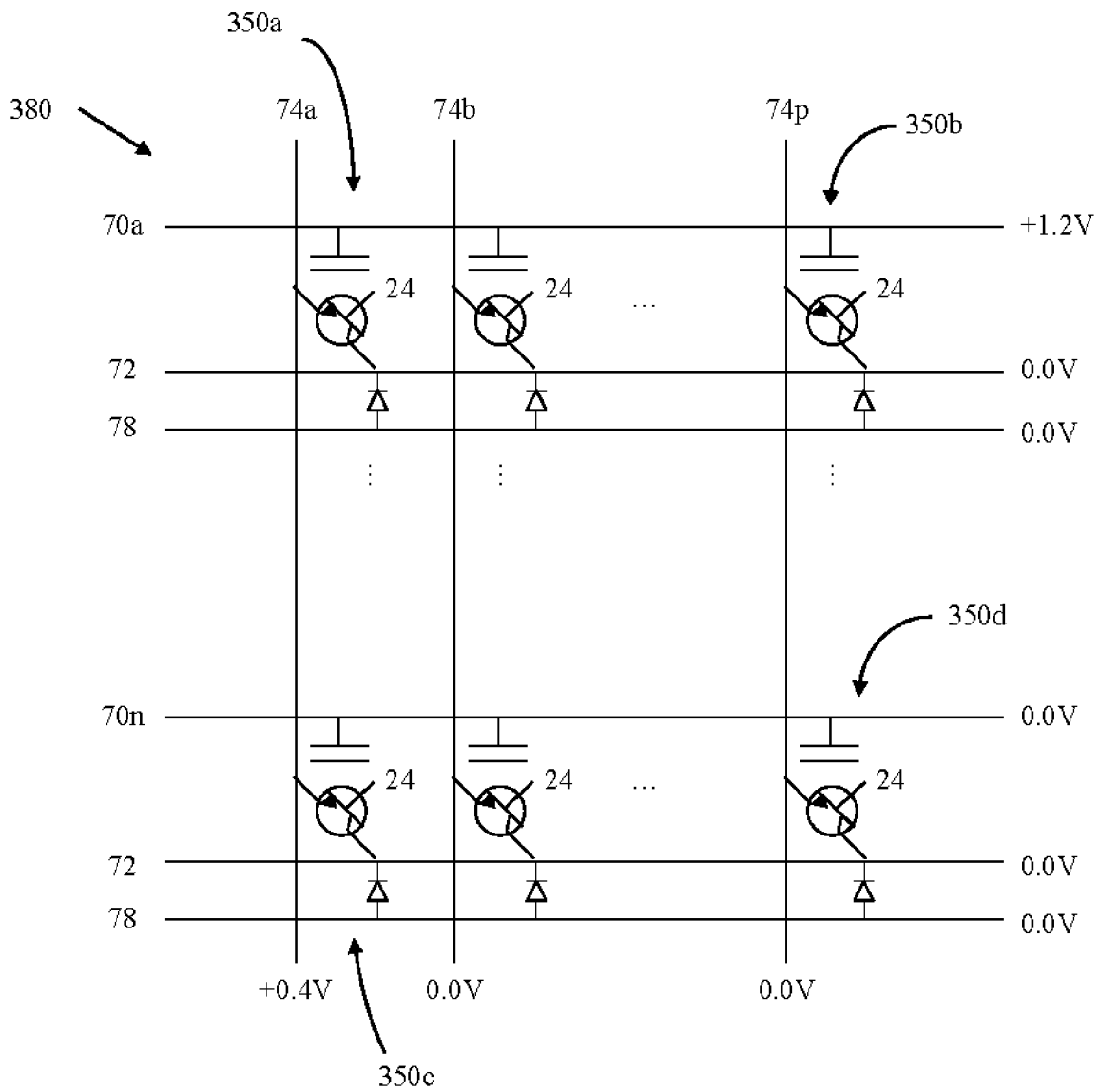


FIG. 54C

Array Write Logic-0 Operation
(All Memory Cells 350)

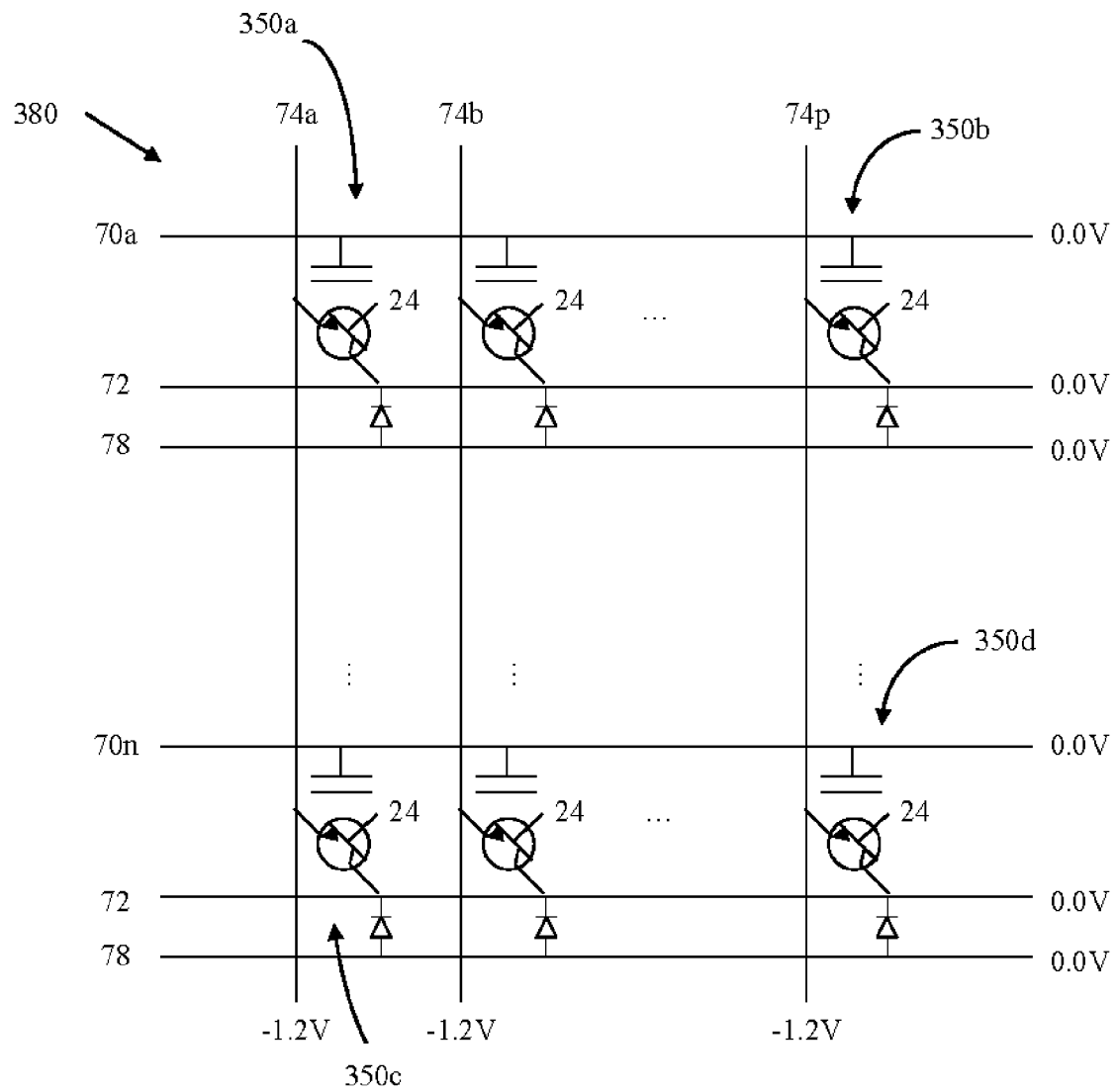


FIG. 54D

Column Write Logic-0 Operation (Memory Cells 350a and 350c)

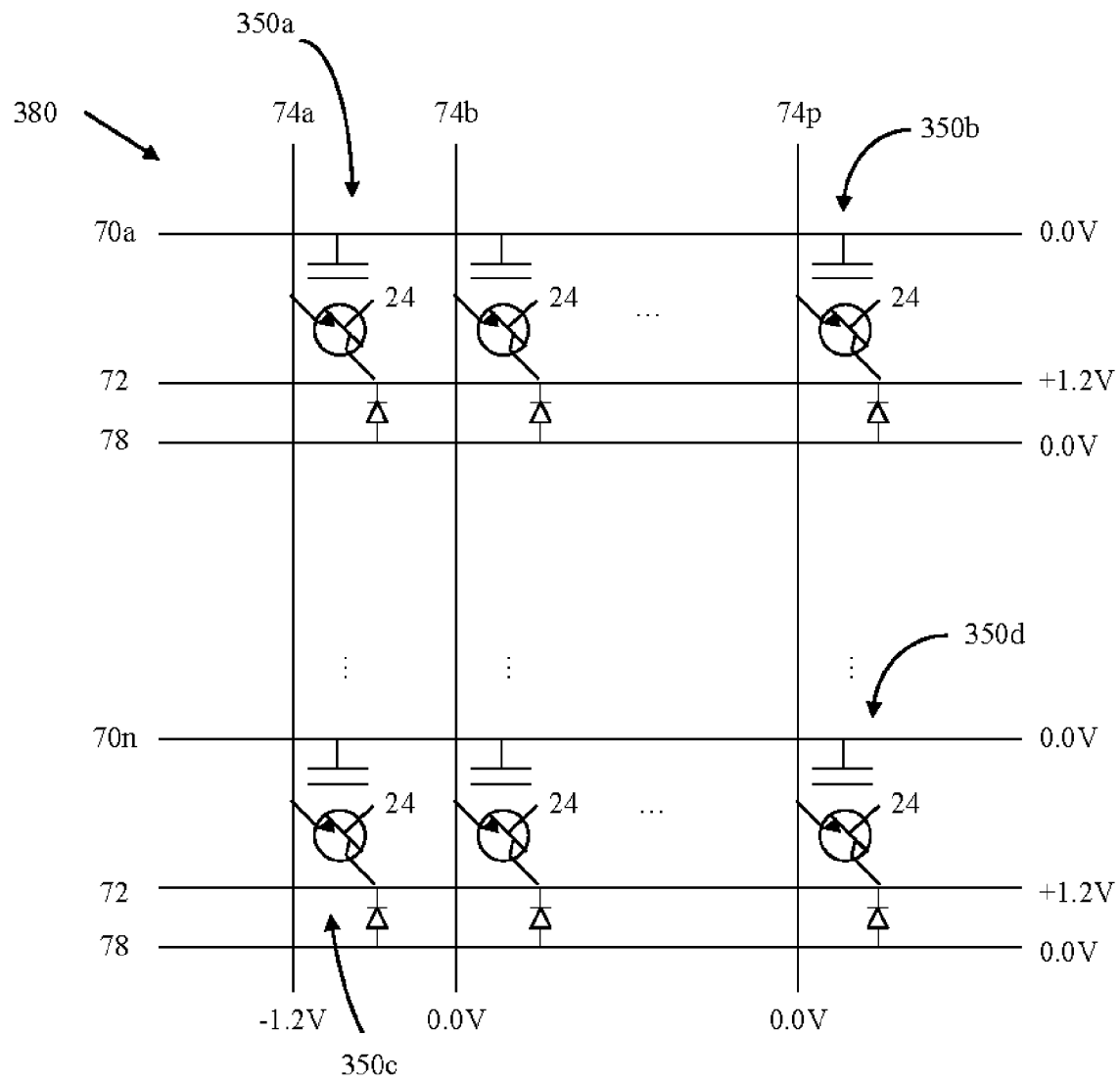


FIG. 54E

Write Logic-0 Operation
(Single Memory Cell 350a)

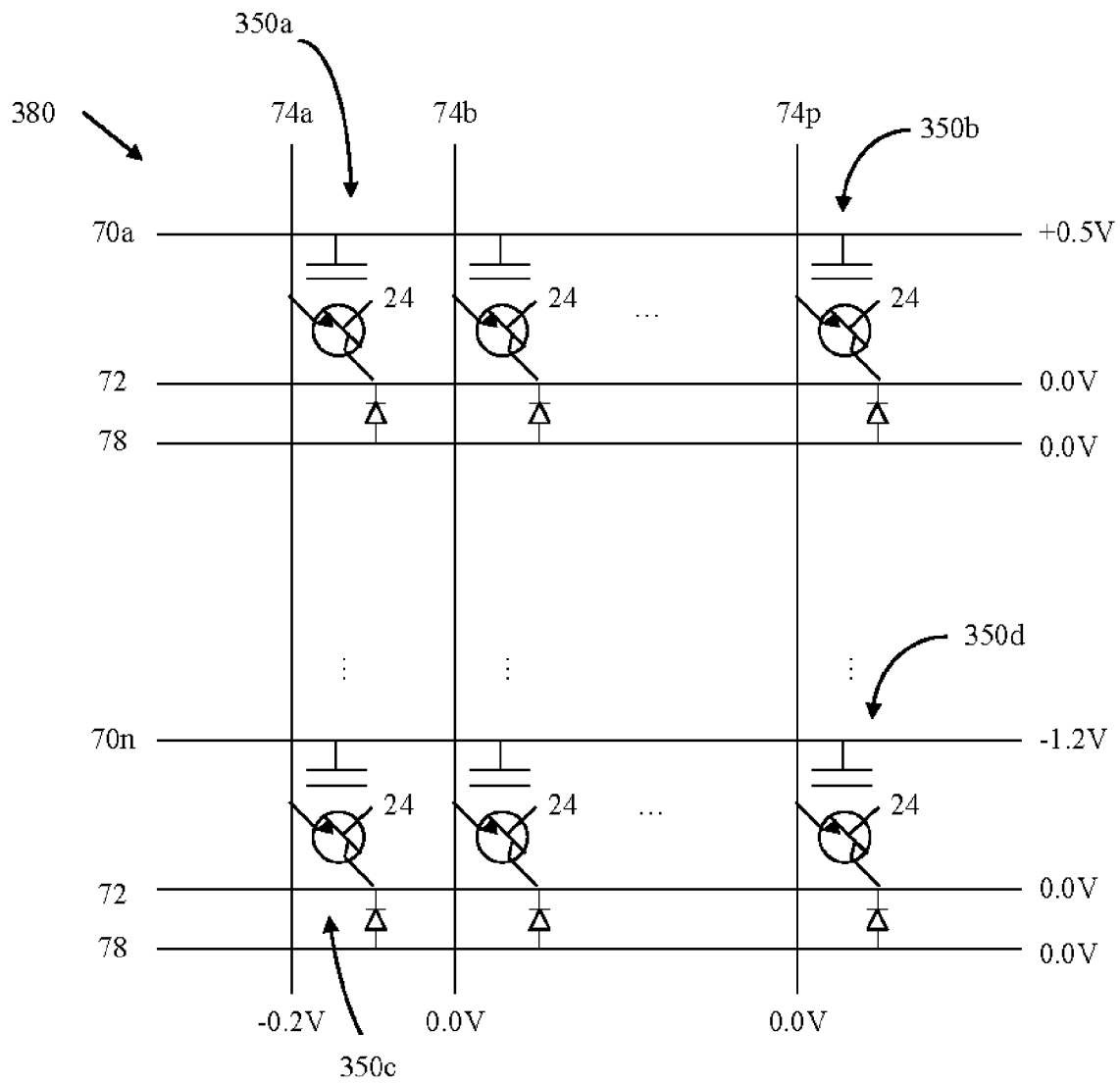


FIG. 54F

Write Logic-1 Operation – GIDL
(Single Memory Cell 350a)

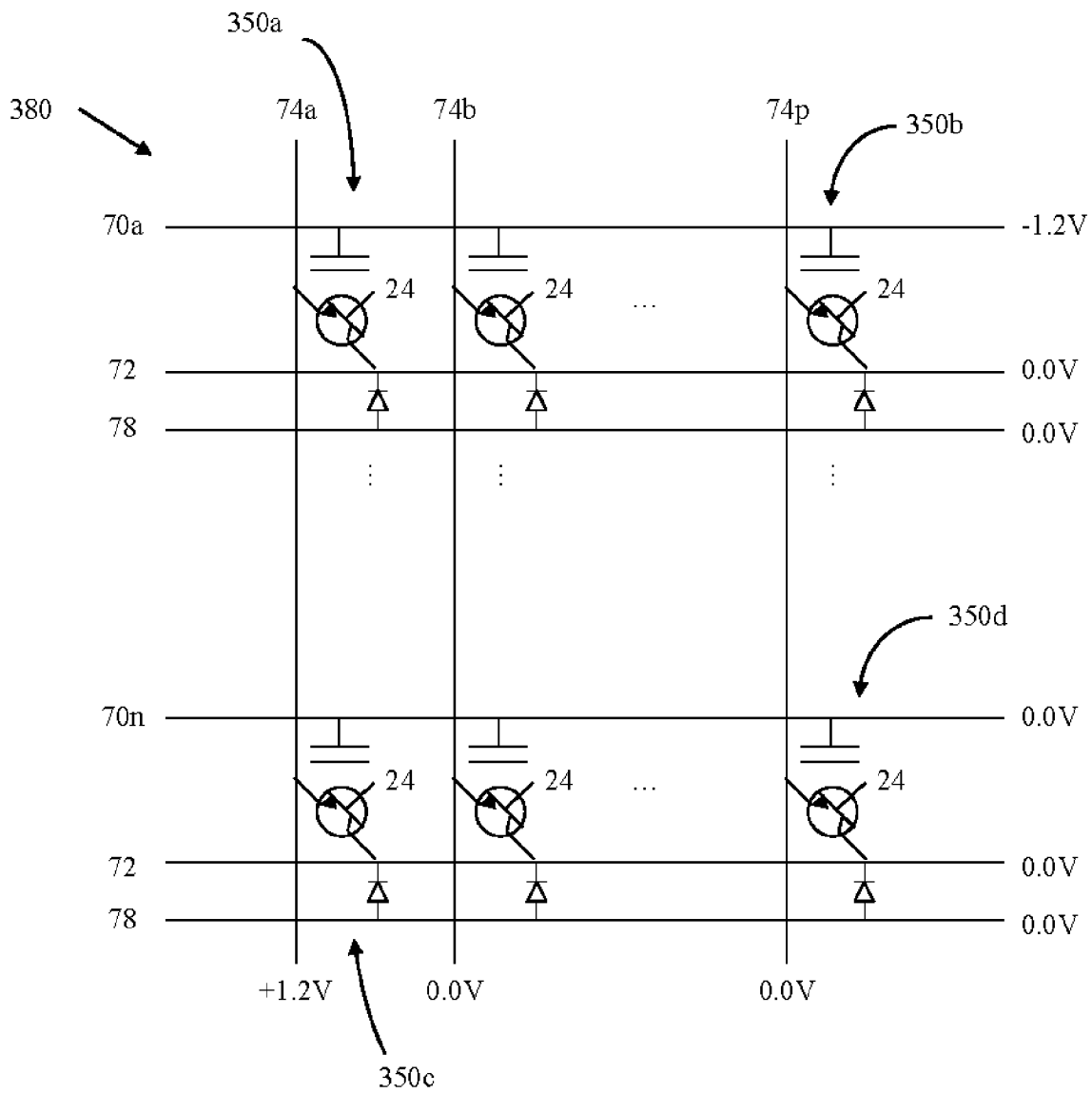


FIG. 54G

Write Logic-1 Operation – Impact Ionization
(Single Memory Cell 350a)

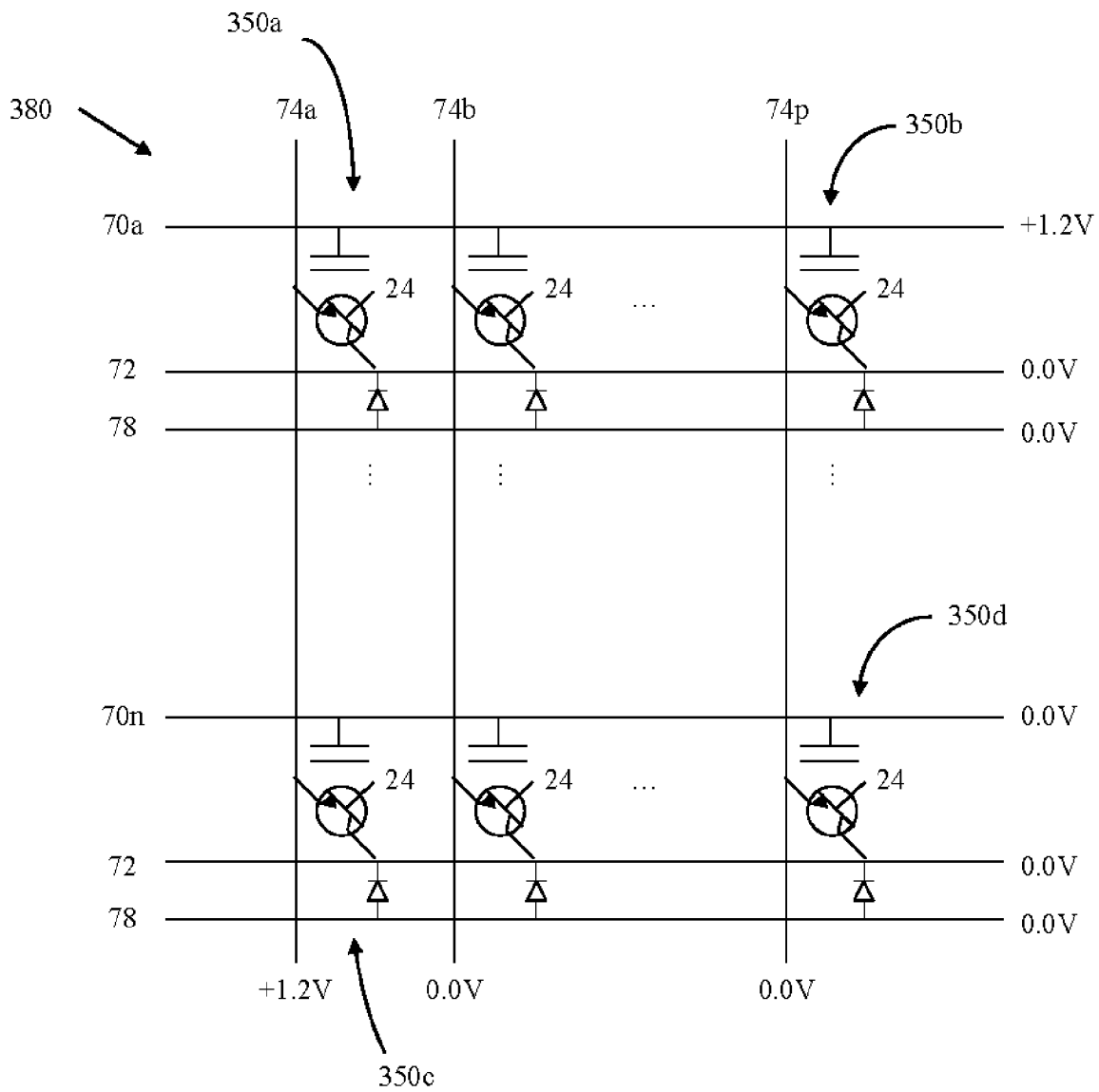


FIG. 54H

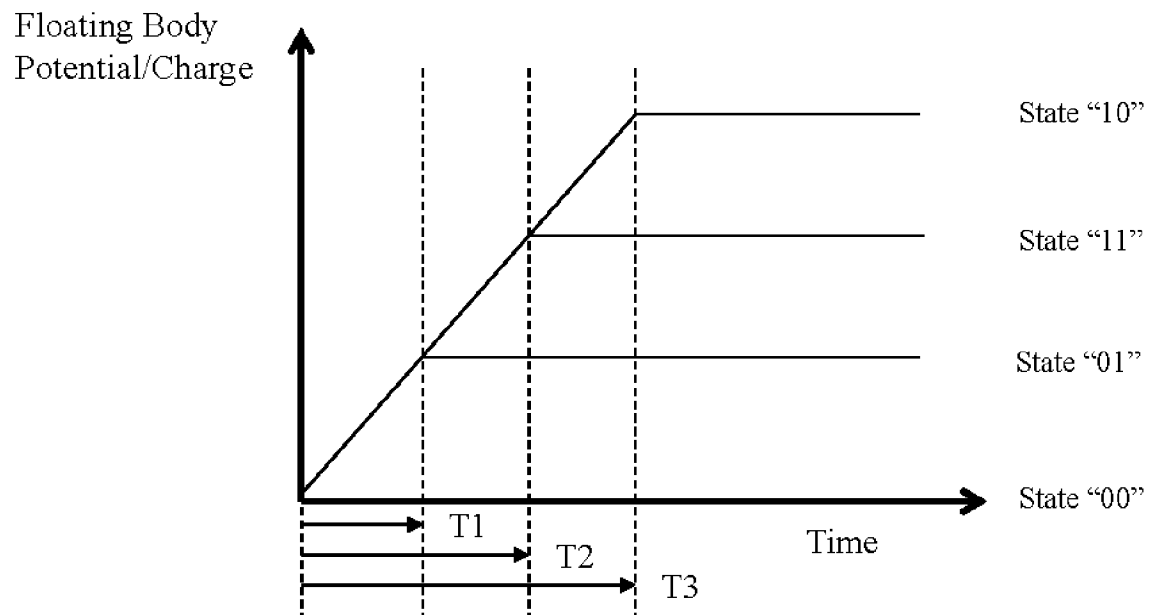


FIG. 55A

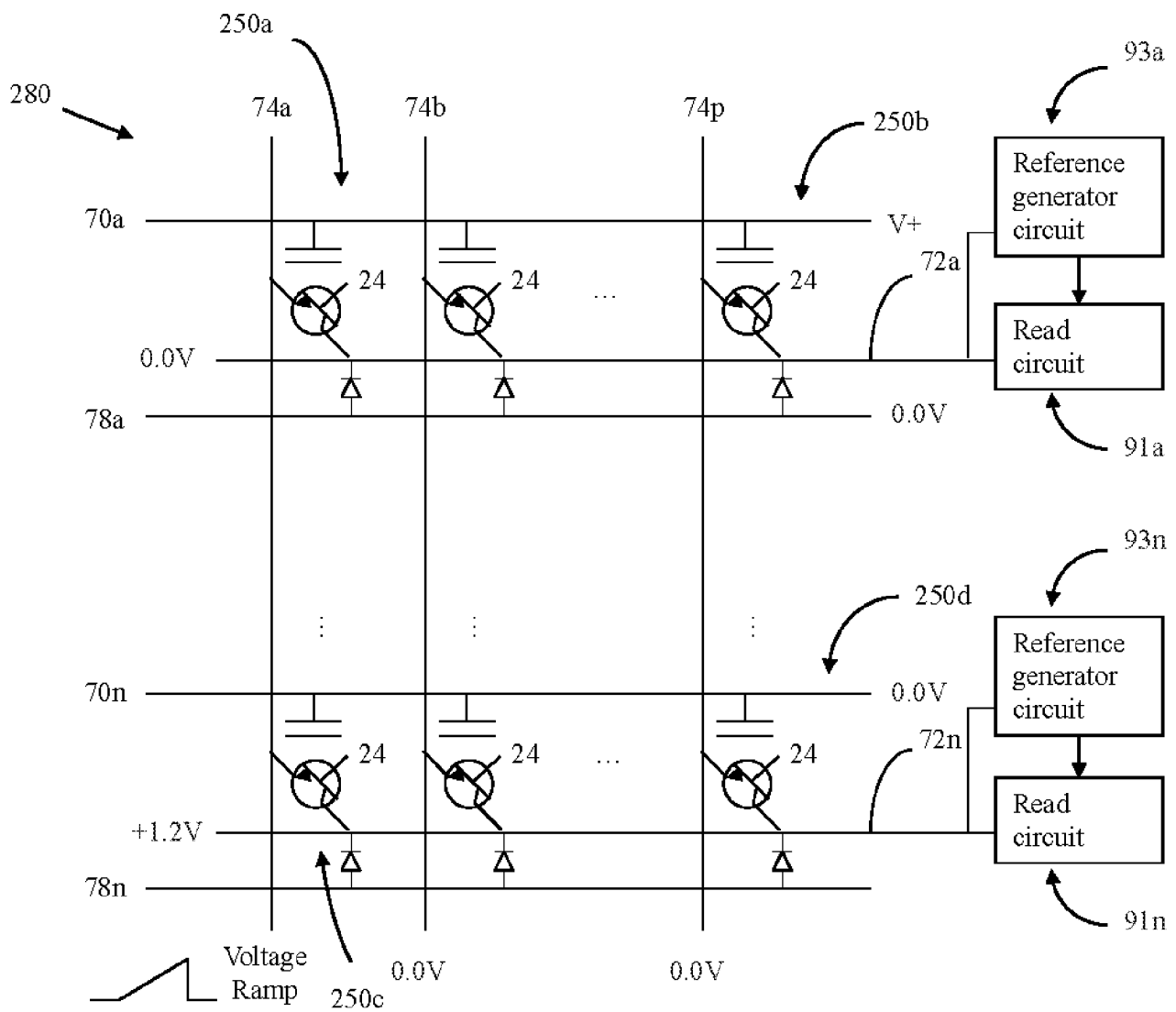


FIG. 55B

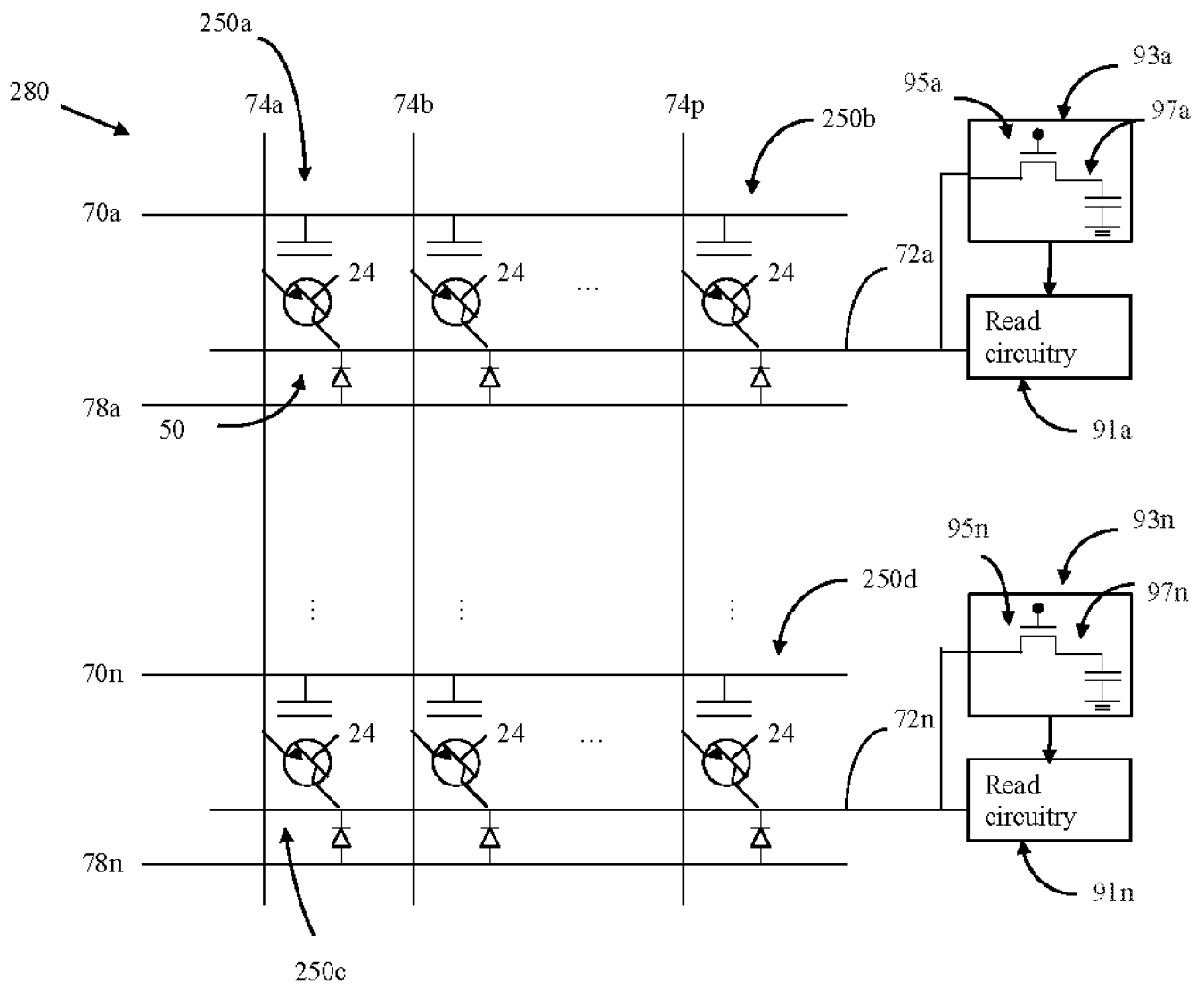


FIG. 55C

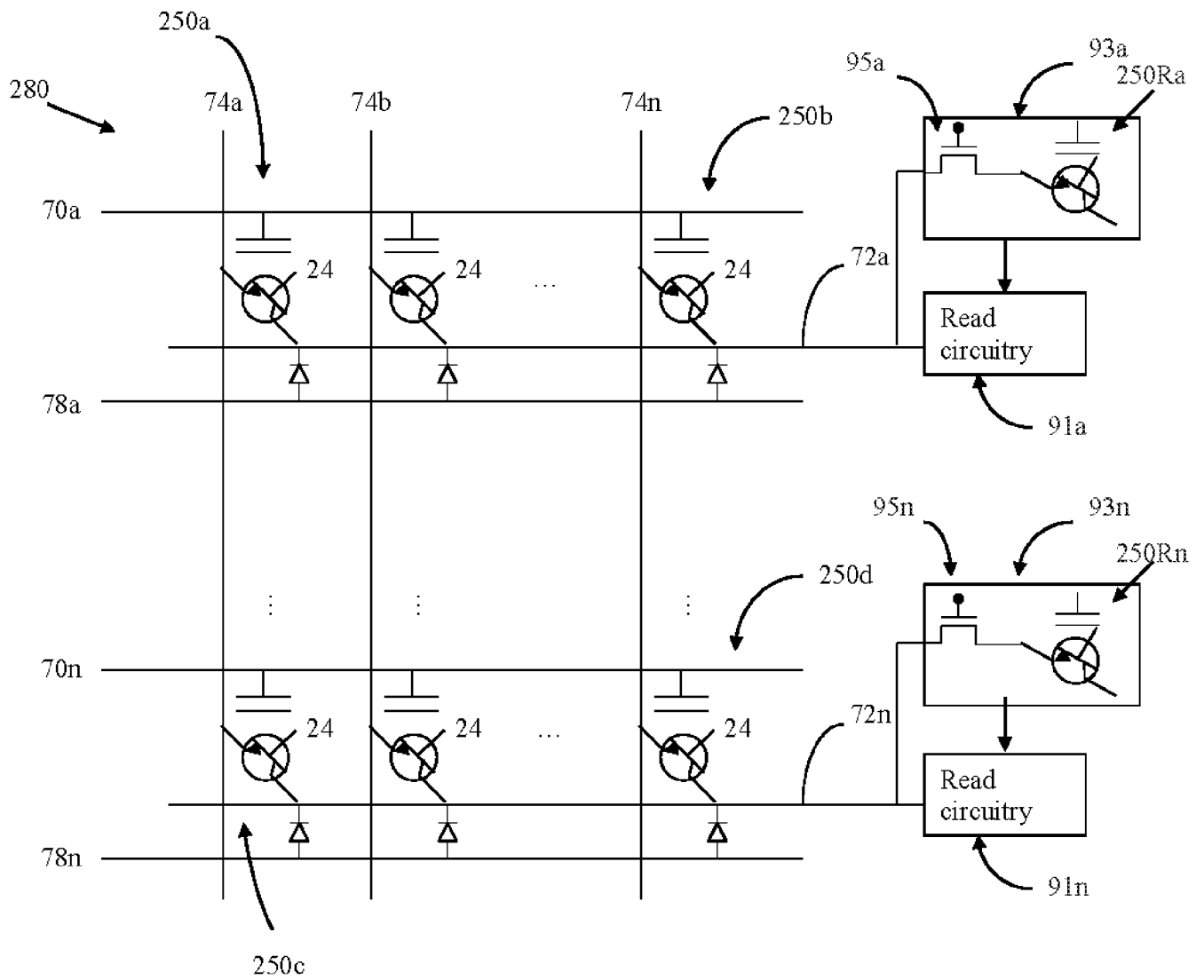


FIG. 55D

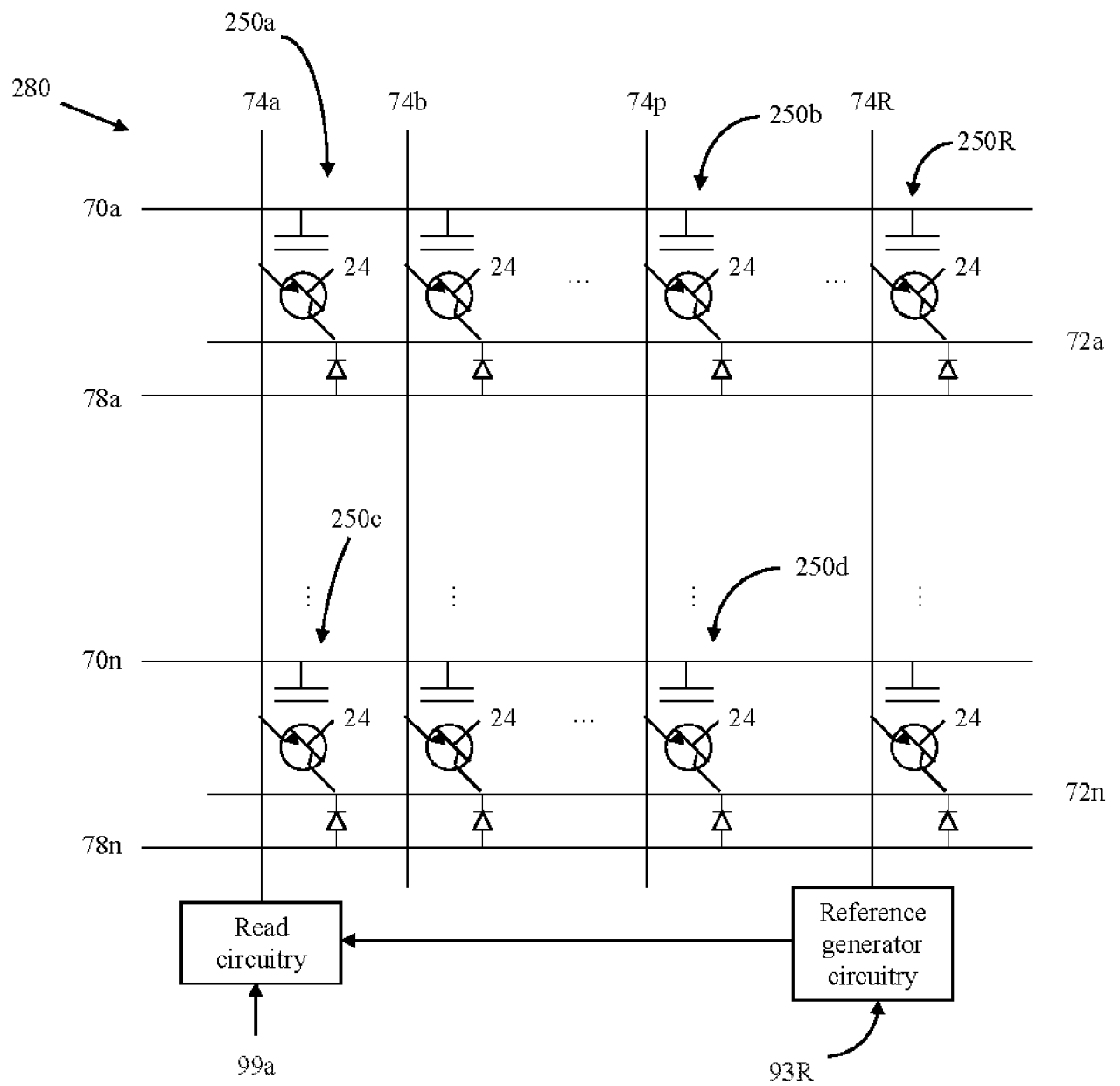


FIG. 55E

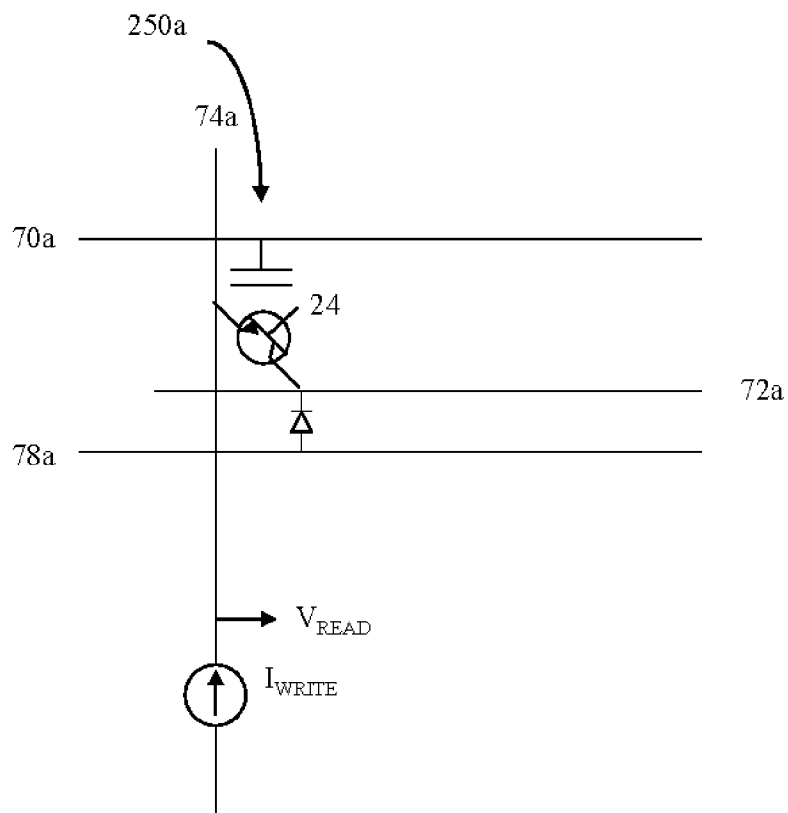


FIG. 55F

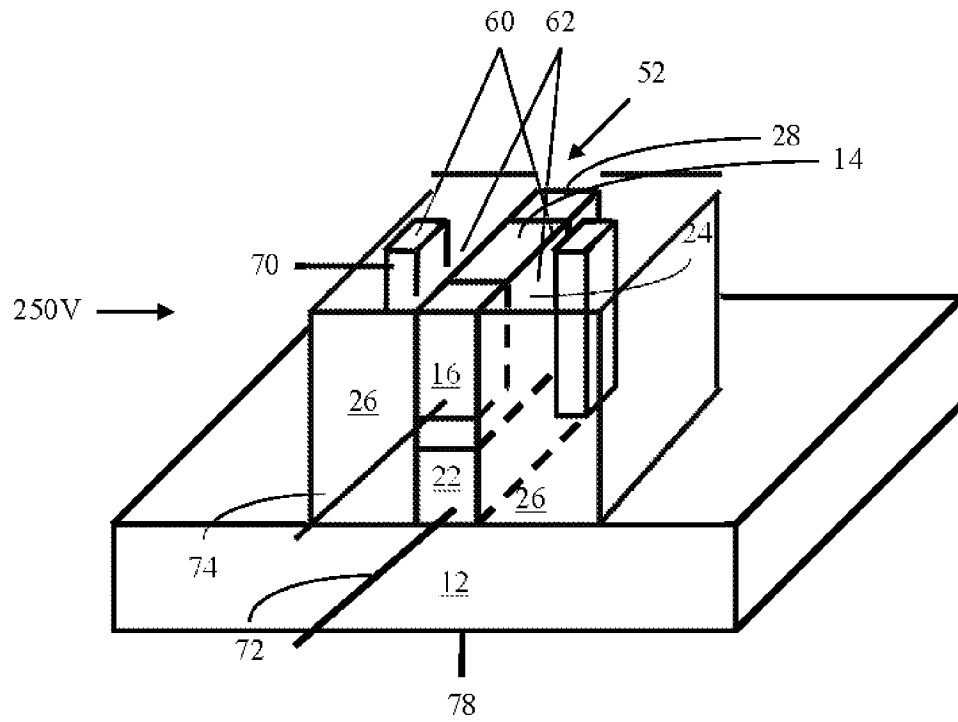


FIG. 56

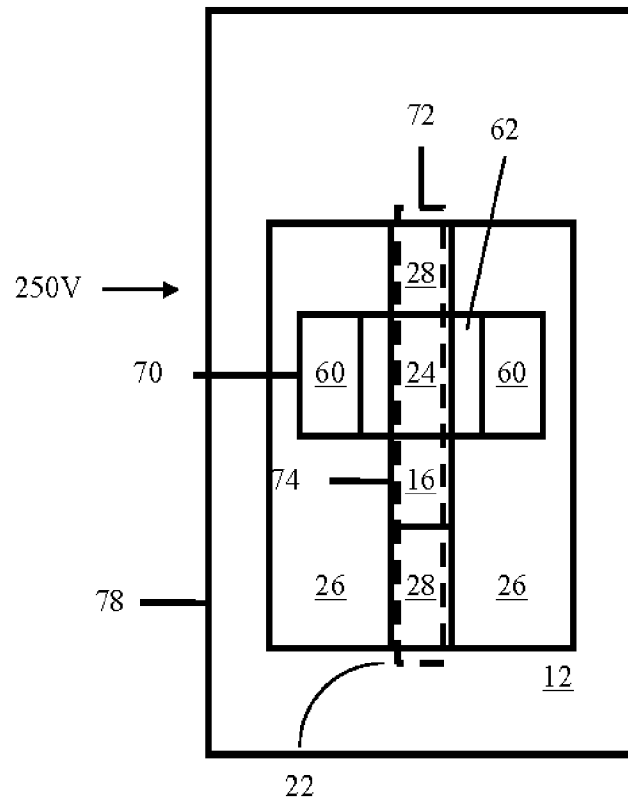


FIG. 57

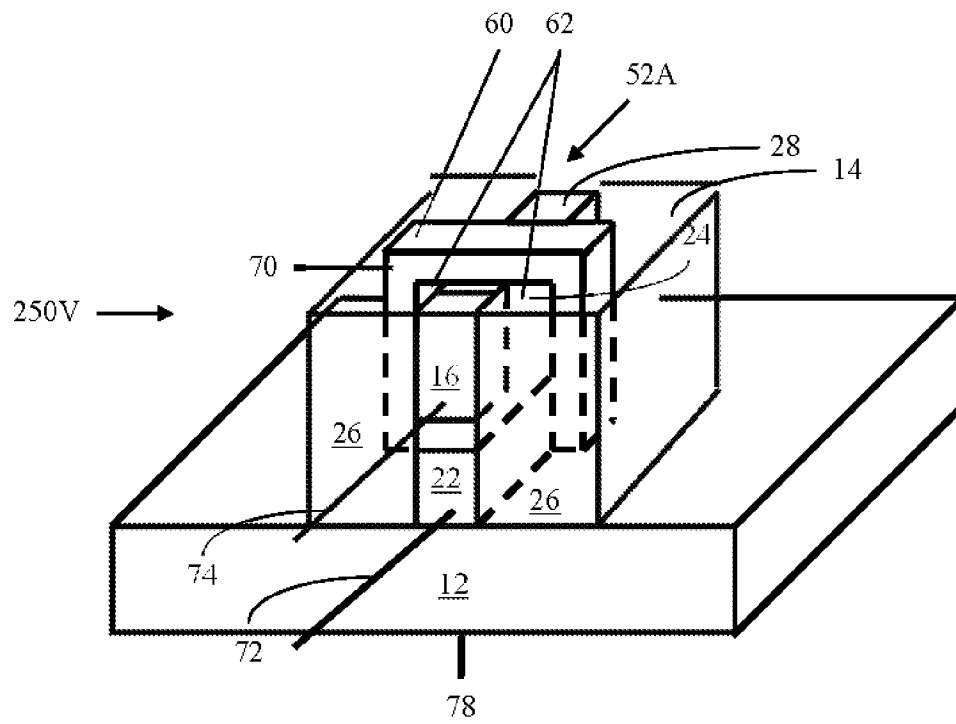


FIG. 58A

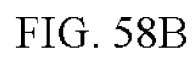


FIG. 58B

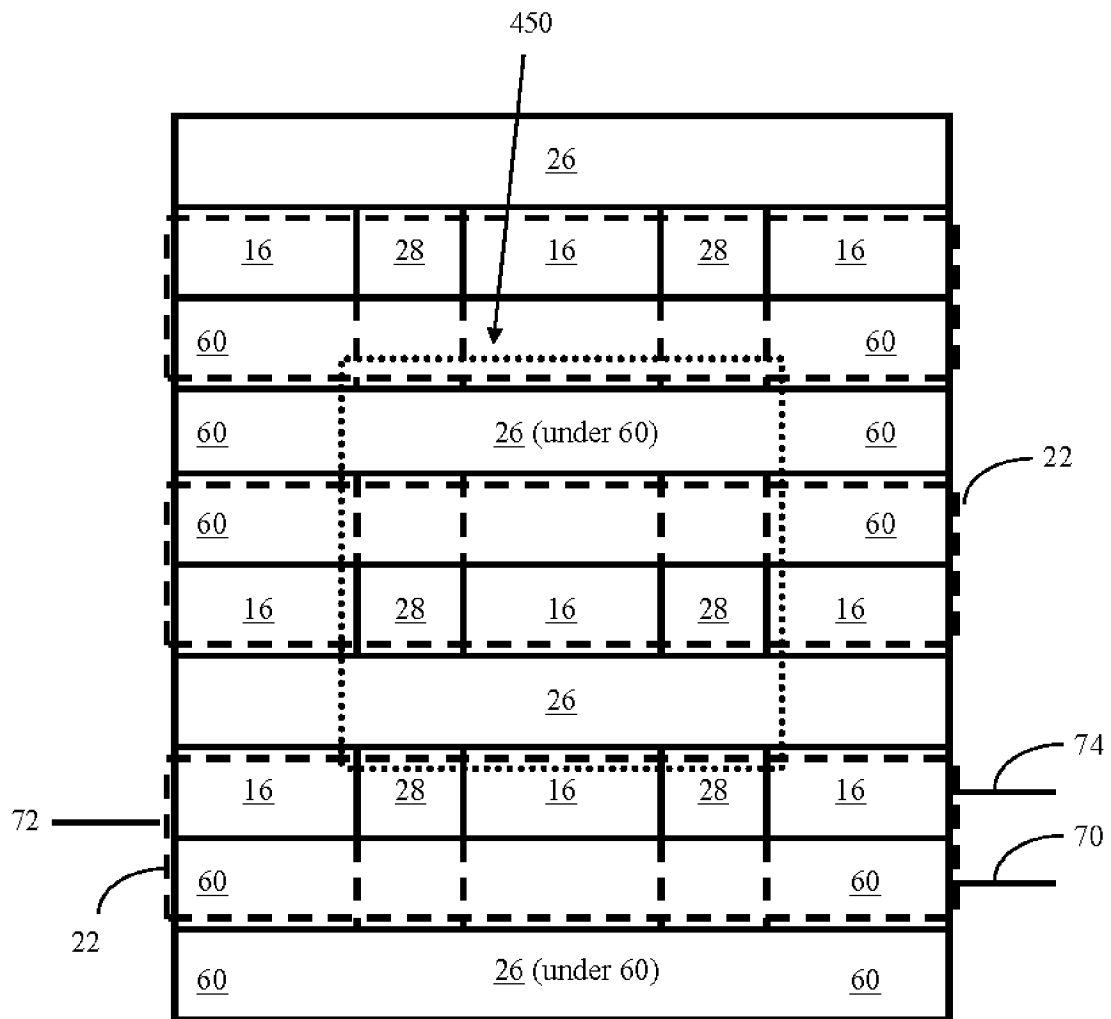


FIG. 59A

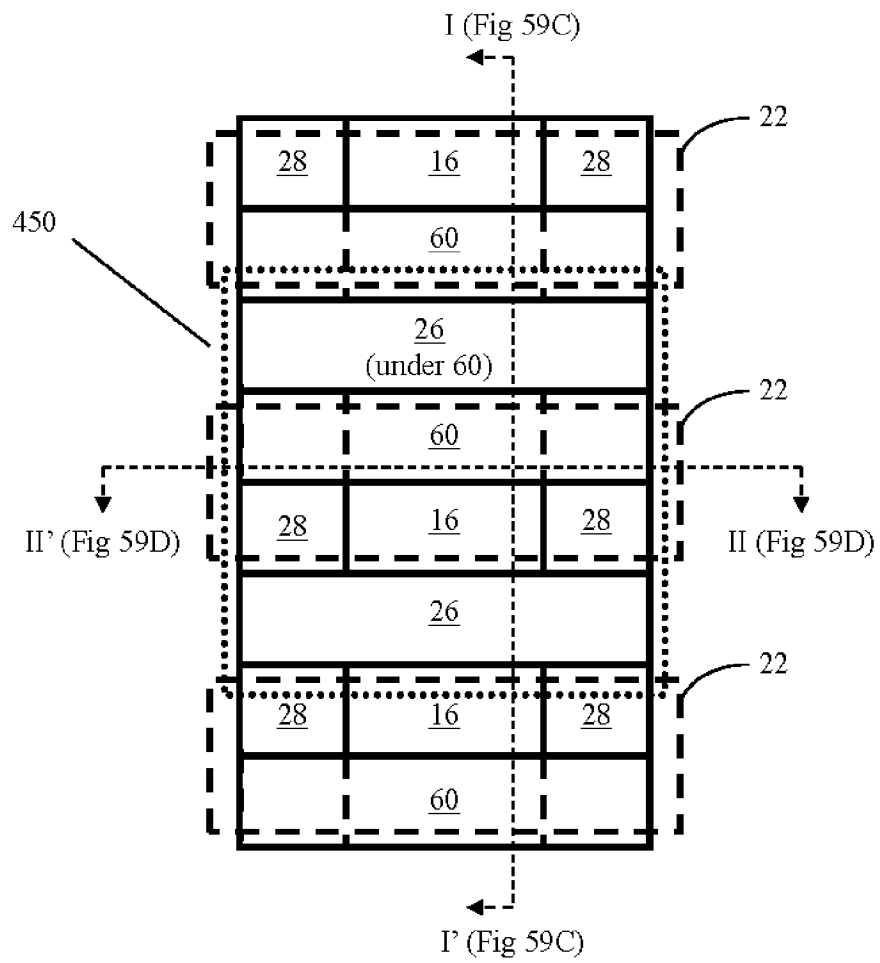


FIG. 59B

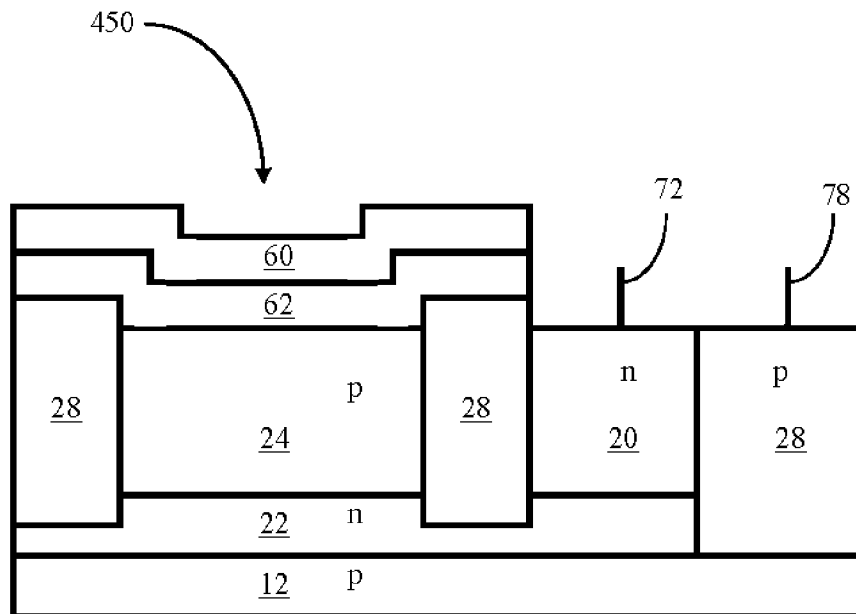


FIG. 59E

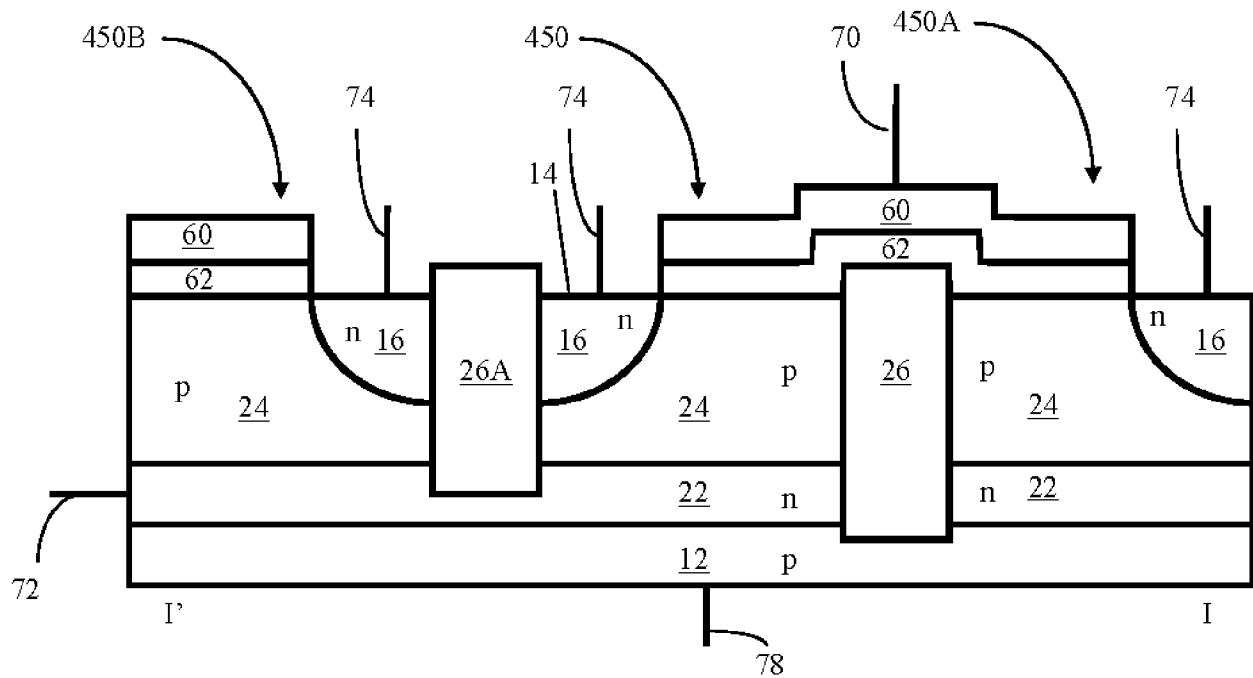


FIG. 59F

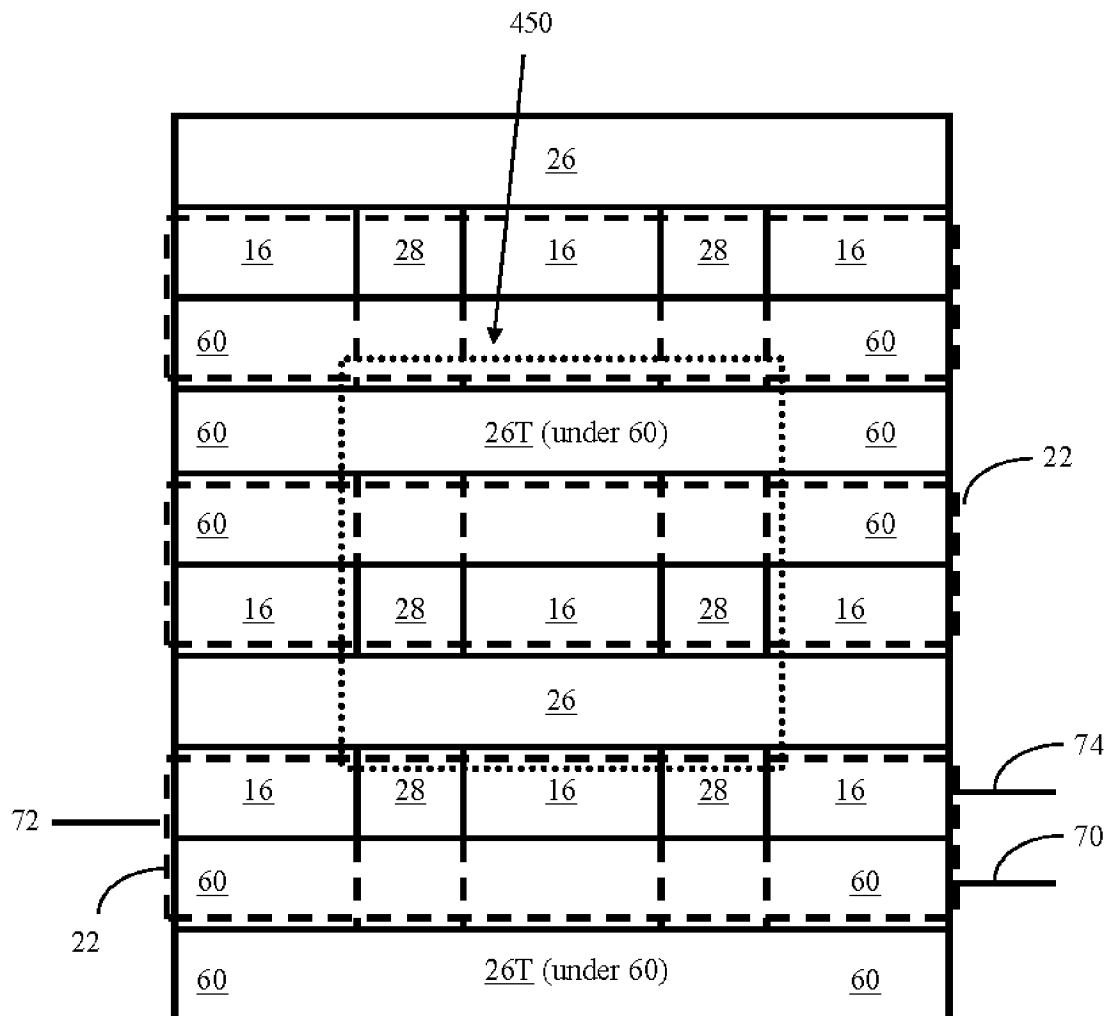


FIG. 60A

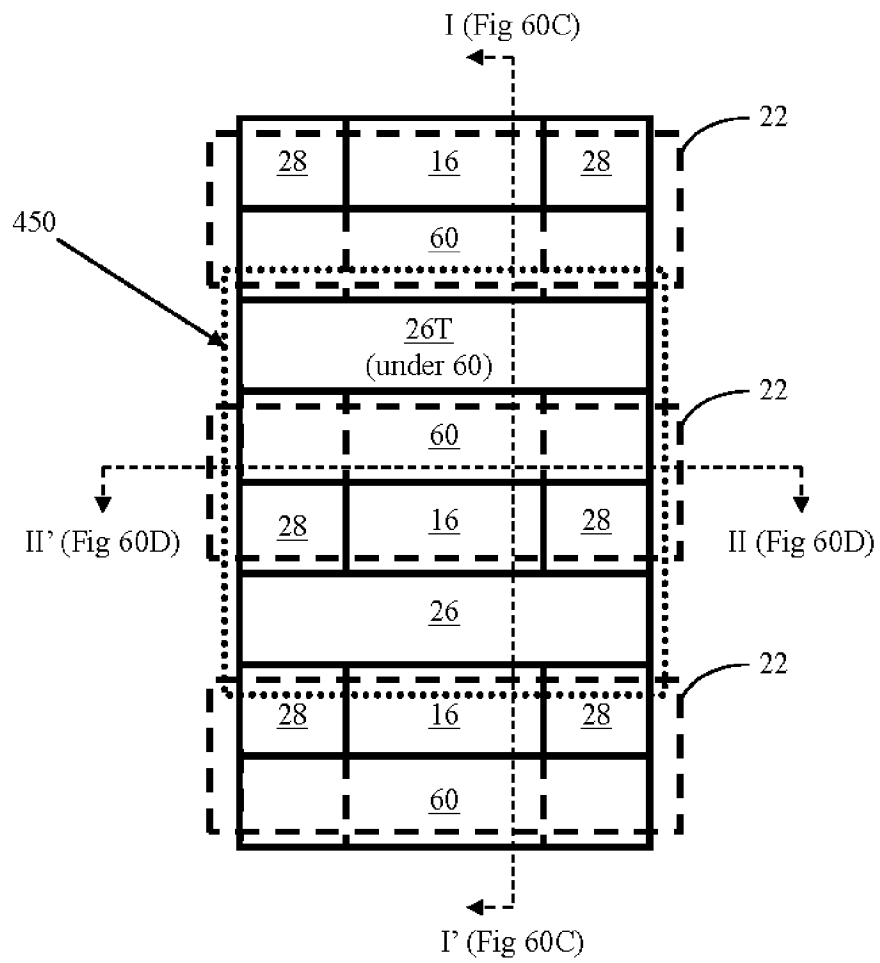


FIG. 60B

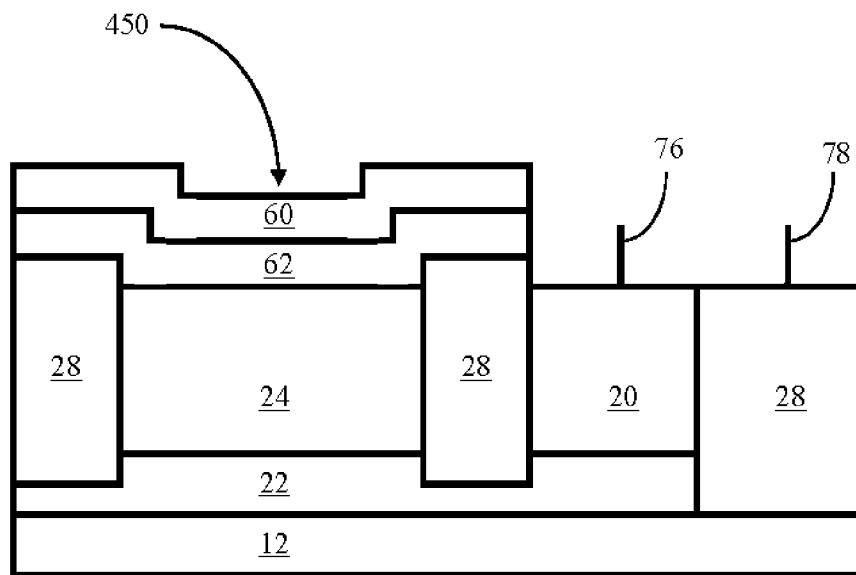


FIG. 60E

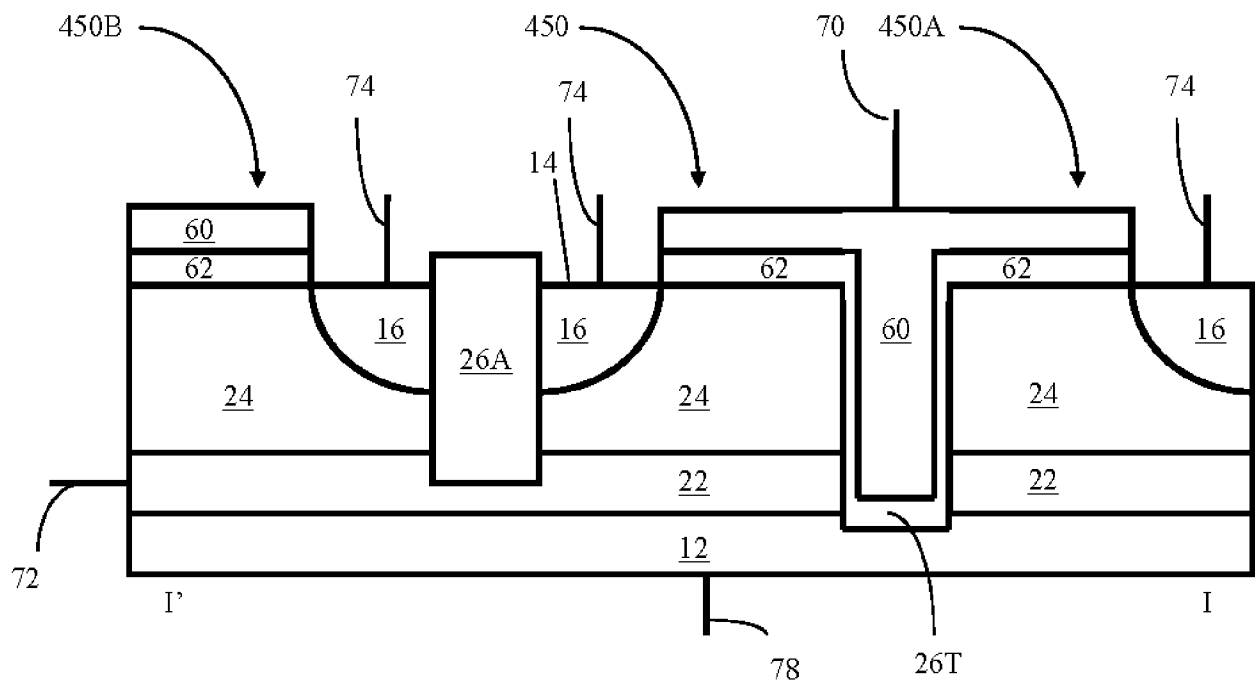


FIG. 60F

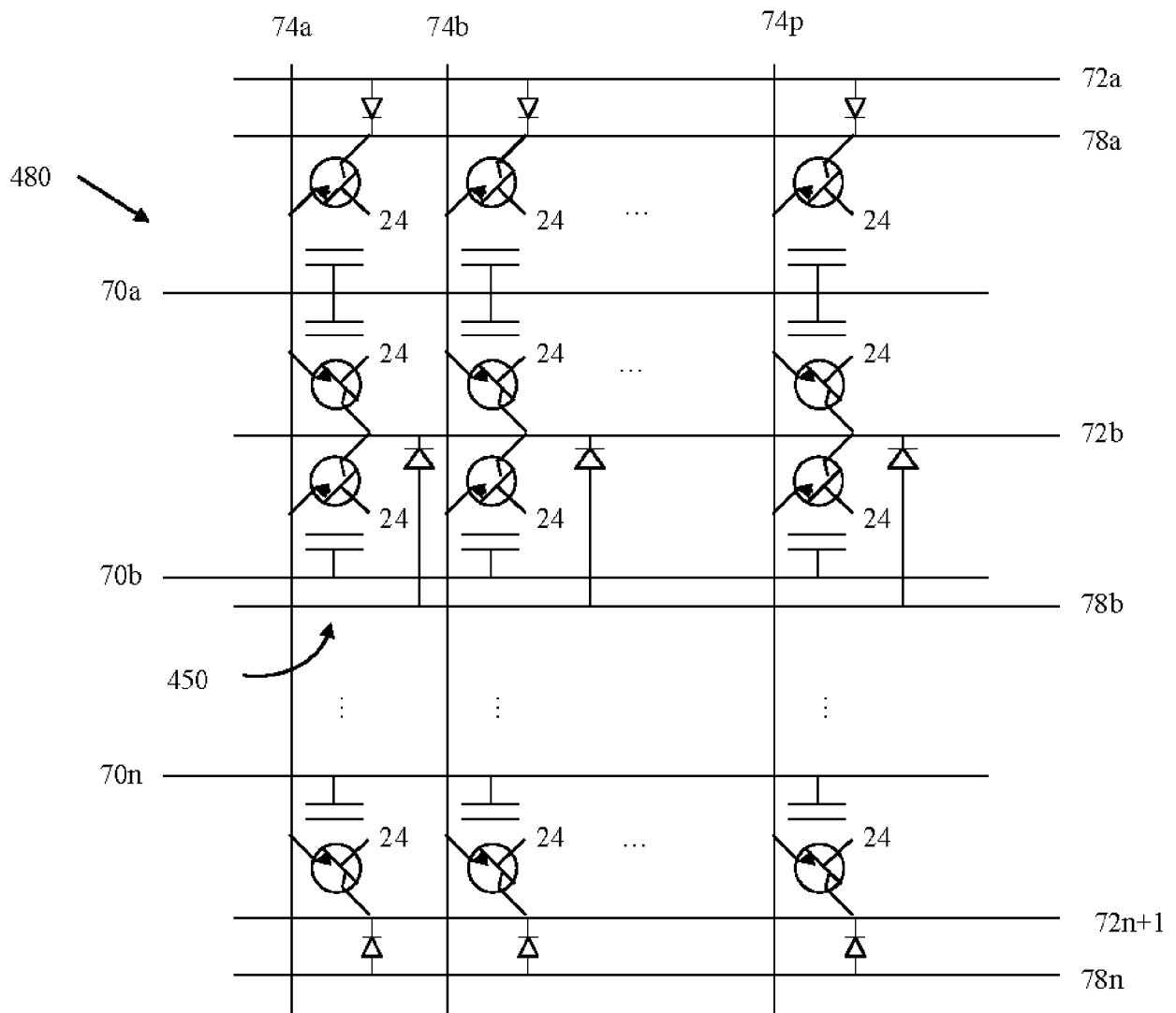


FIG. 61A

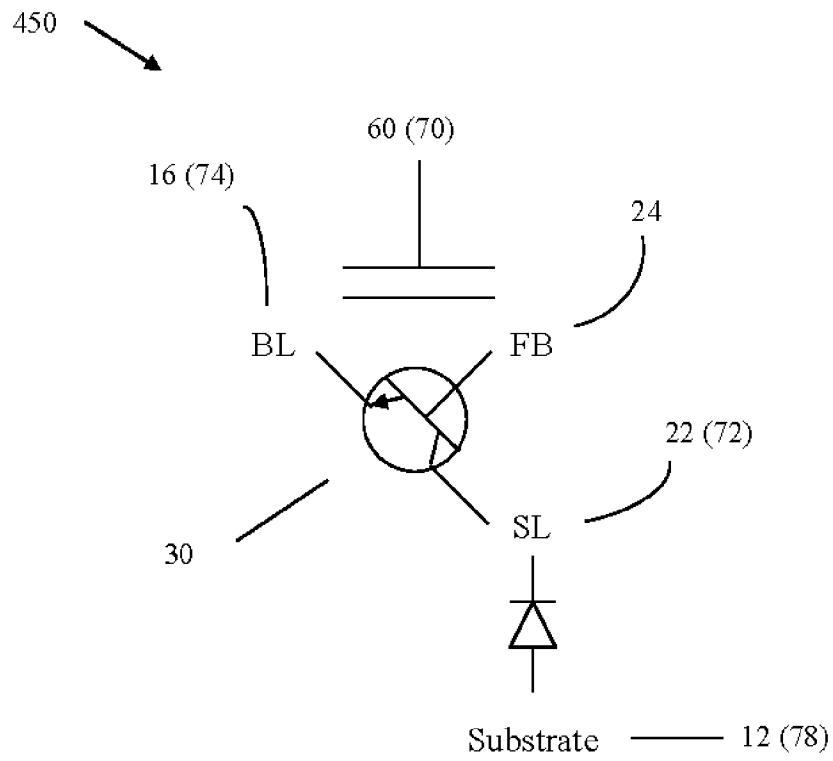


FIG. 61B

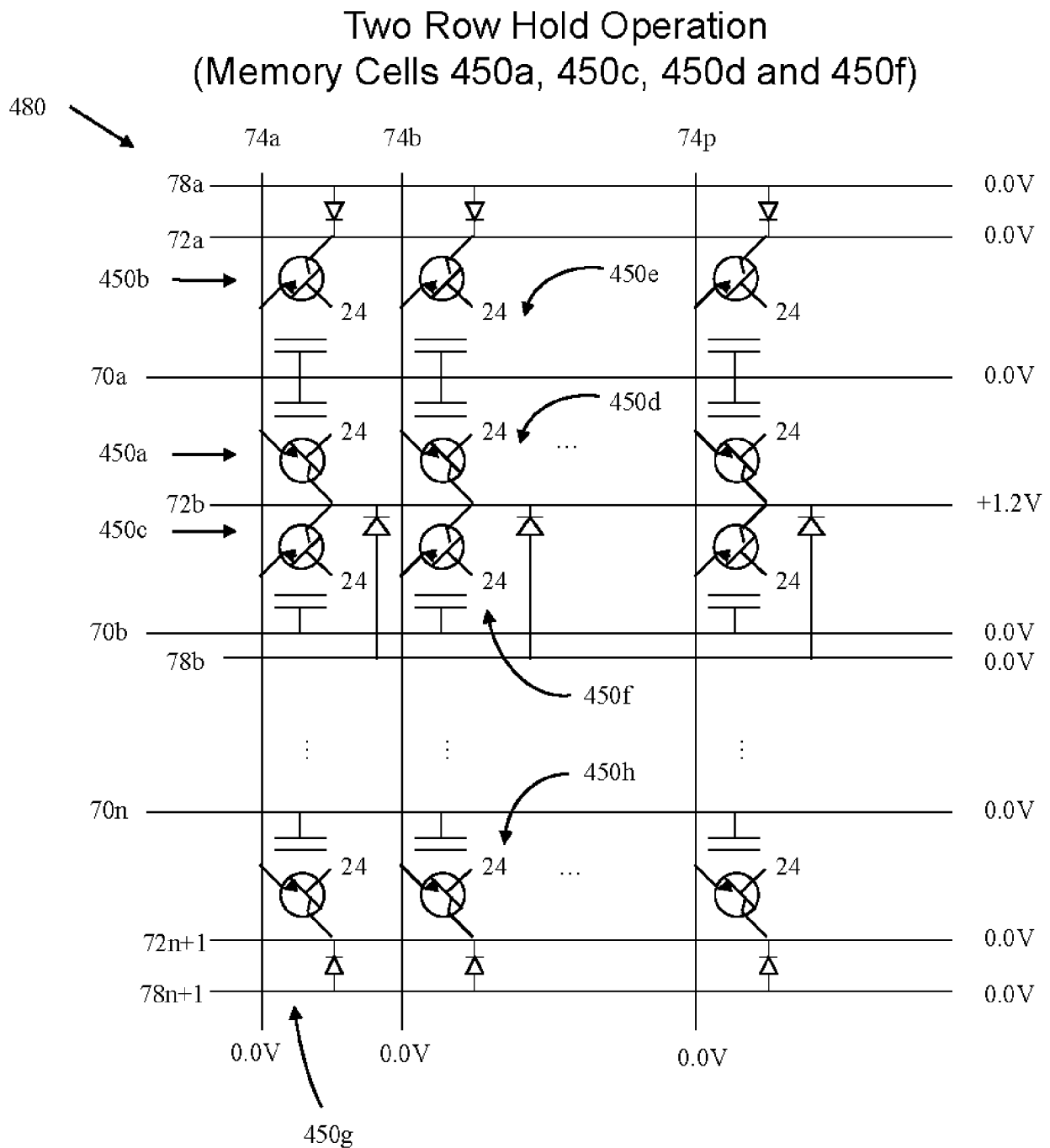


FIG. 62

Read Operation (Single Memory Cell 450a)

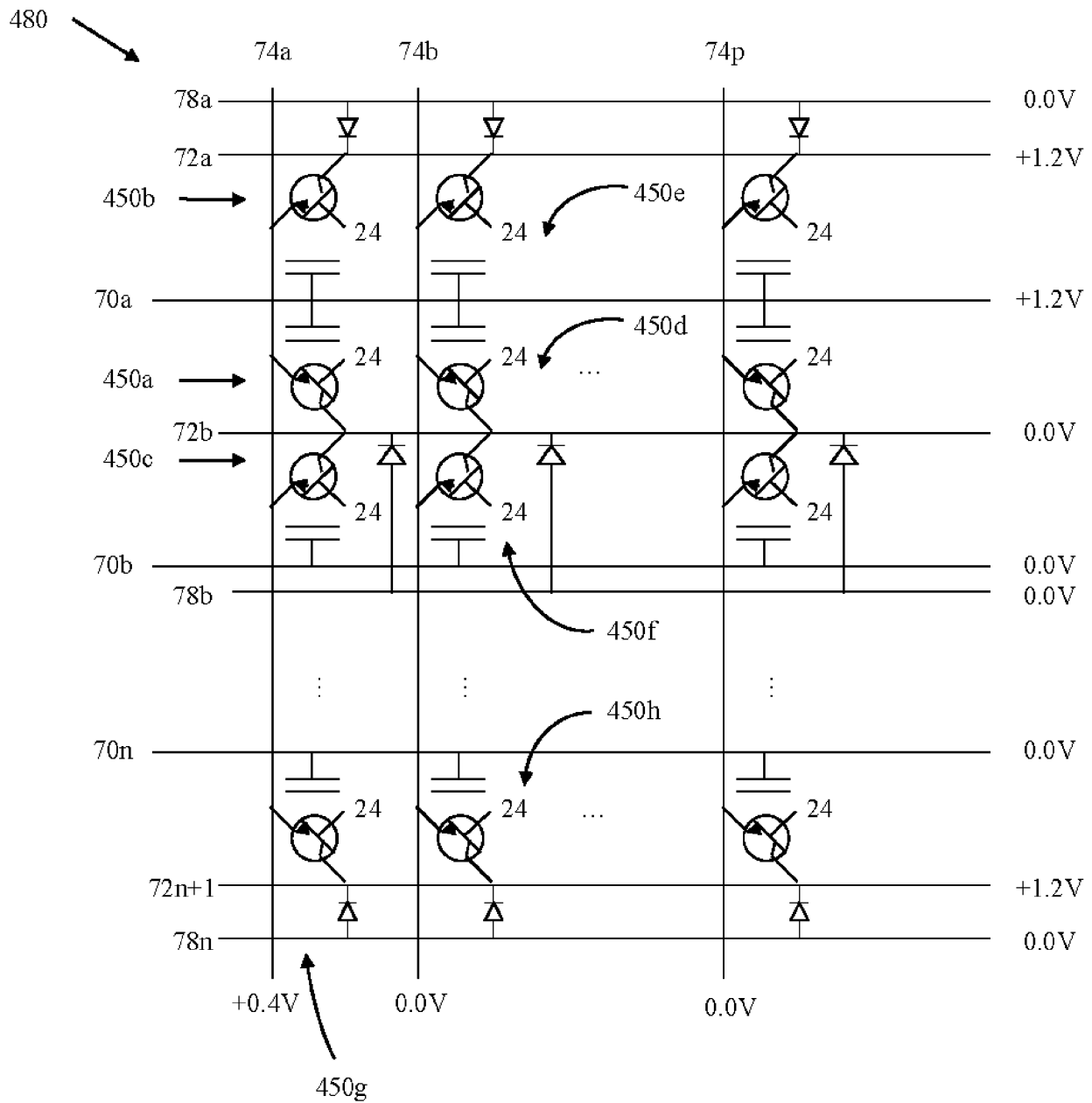


FIG. 63

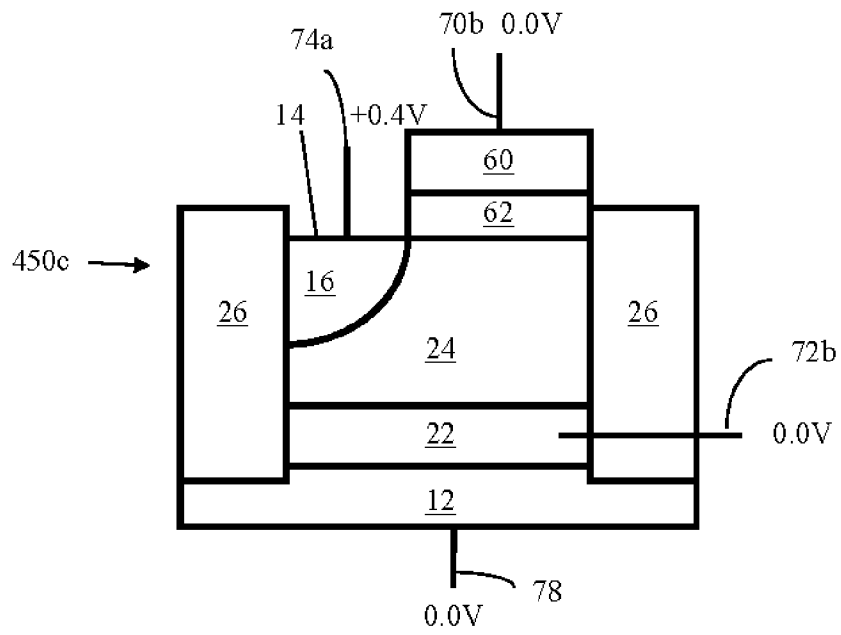


FIG. 64E

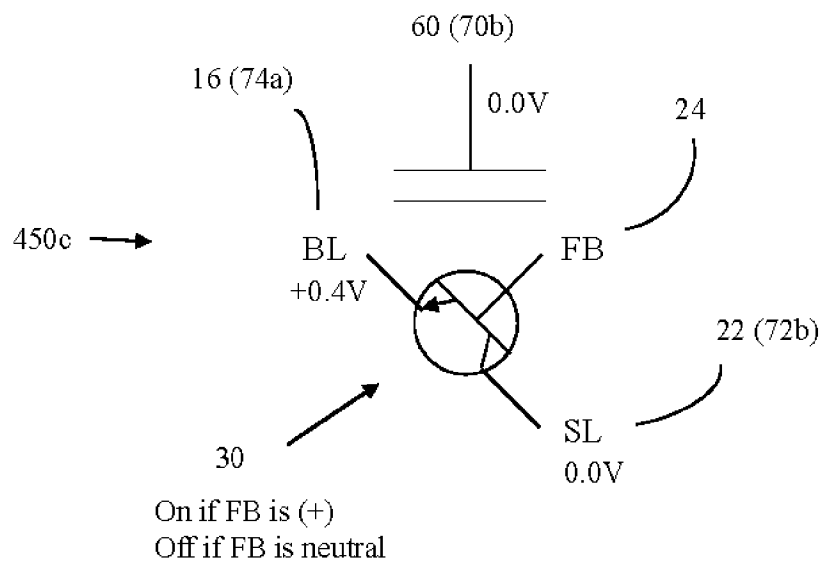


FIG. 64F

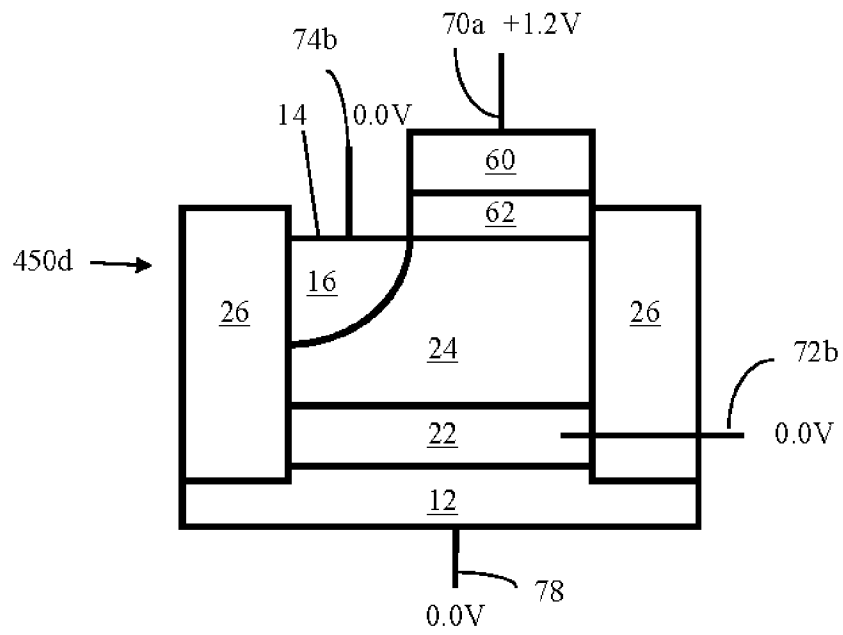


FIG. 64G

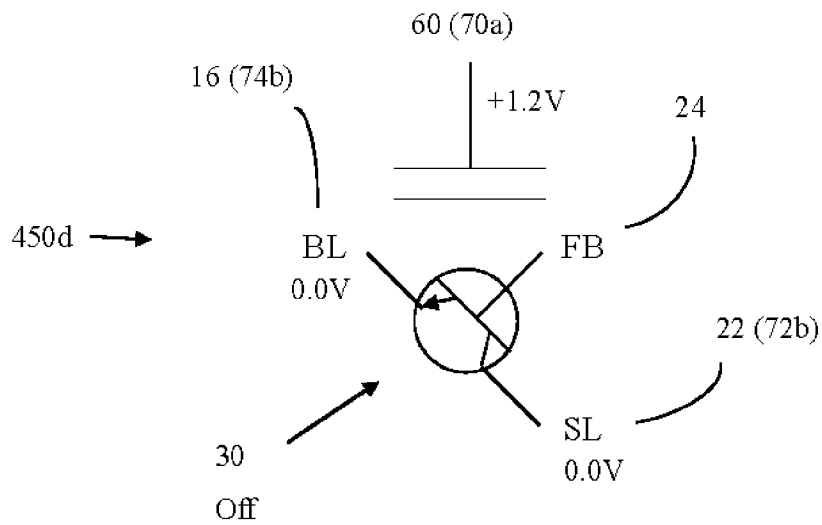
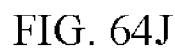


FIG. 64H



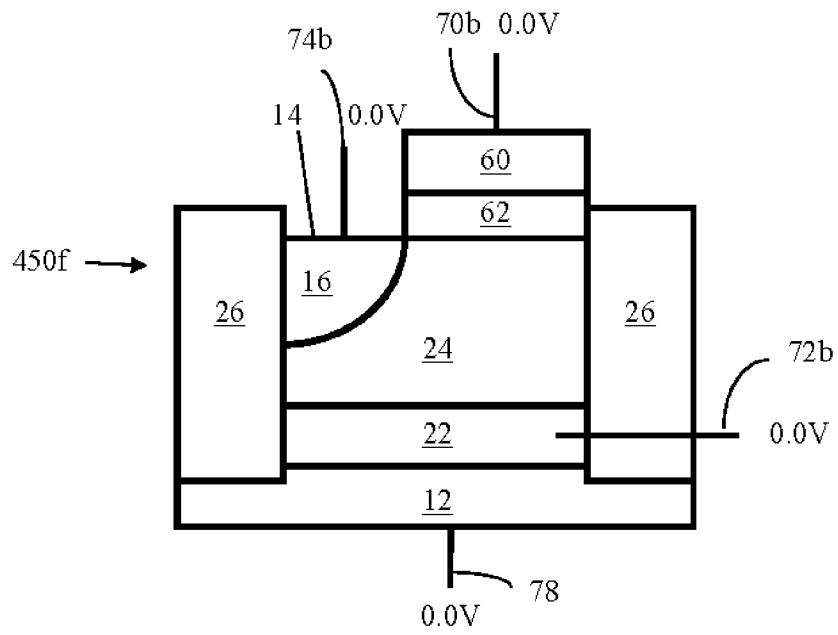


FIG. 64K

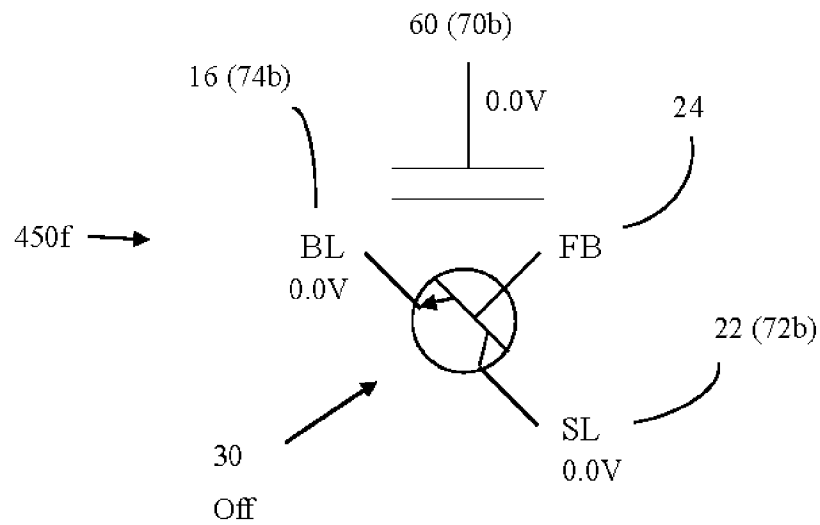


FIG. 64L

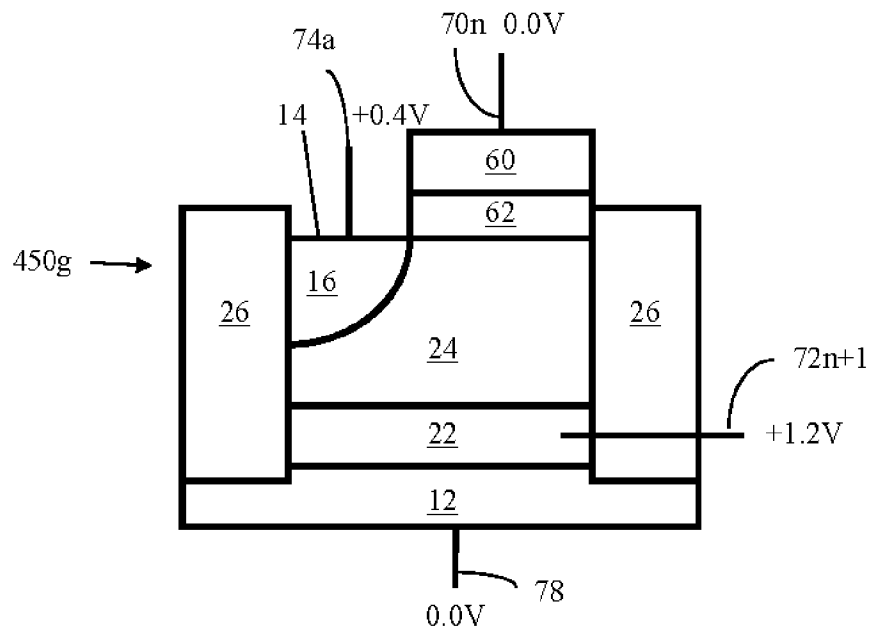


FIG. 64M

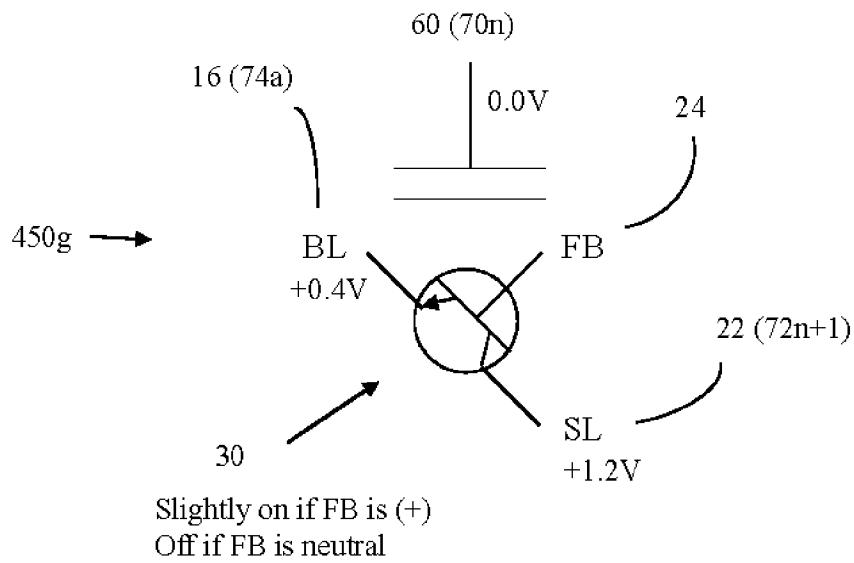


FIG. 64N

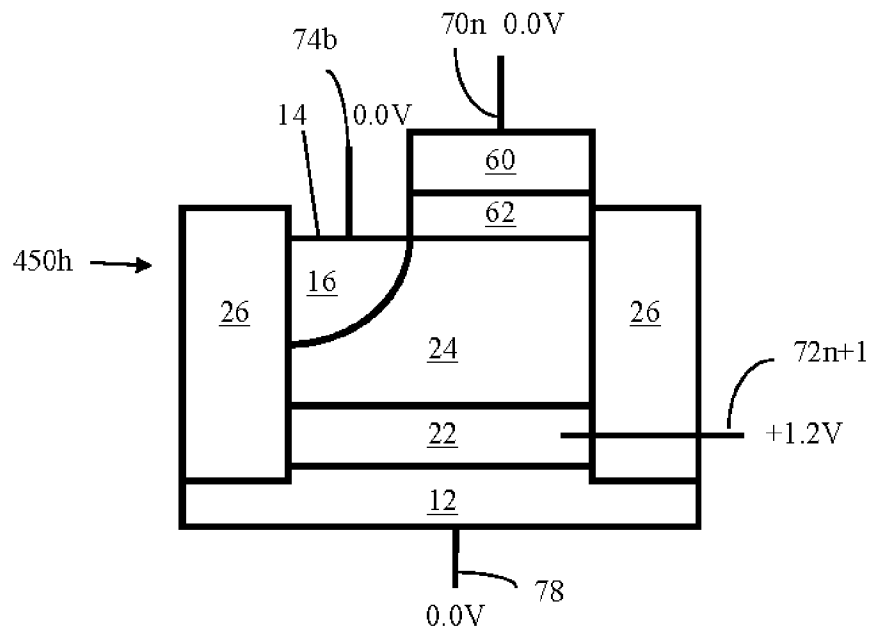


FIG. 64O

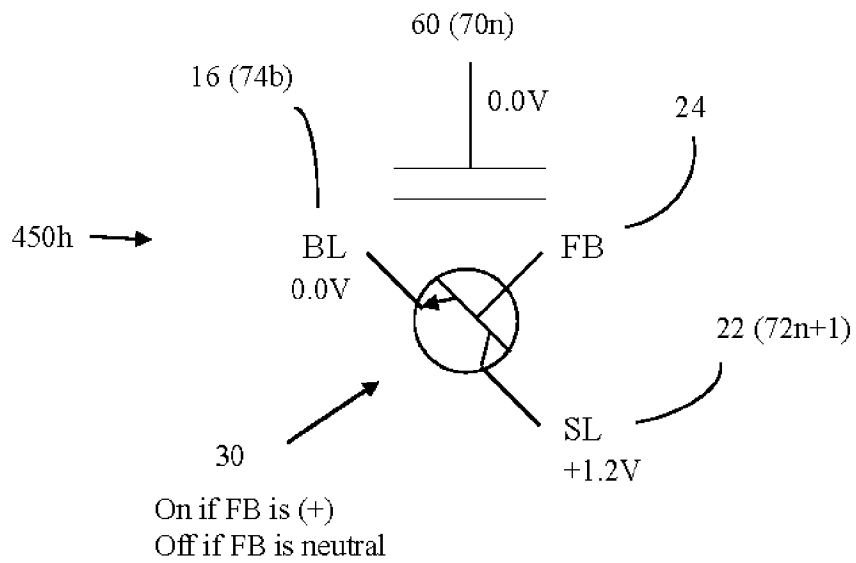
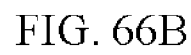
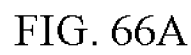


FIG. 64P

480





Single Column Write Logic-0 Operation (Memory Cells 450a, 450b, 450c and 450g)

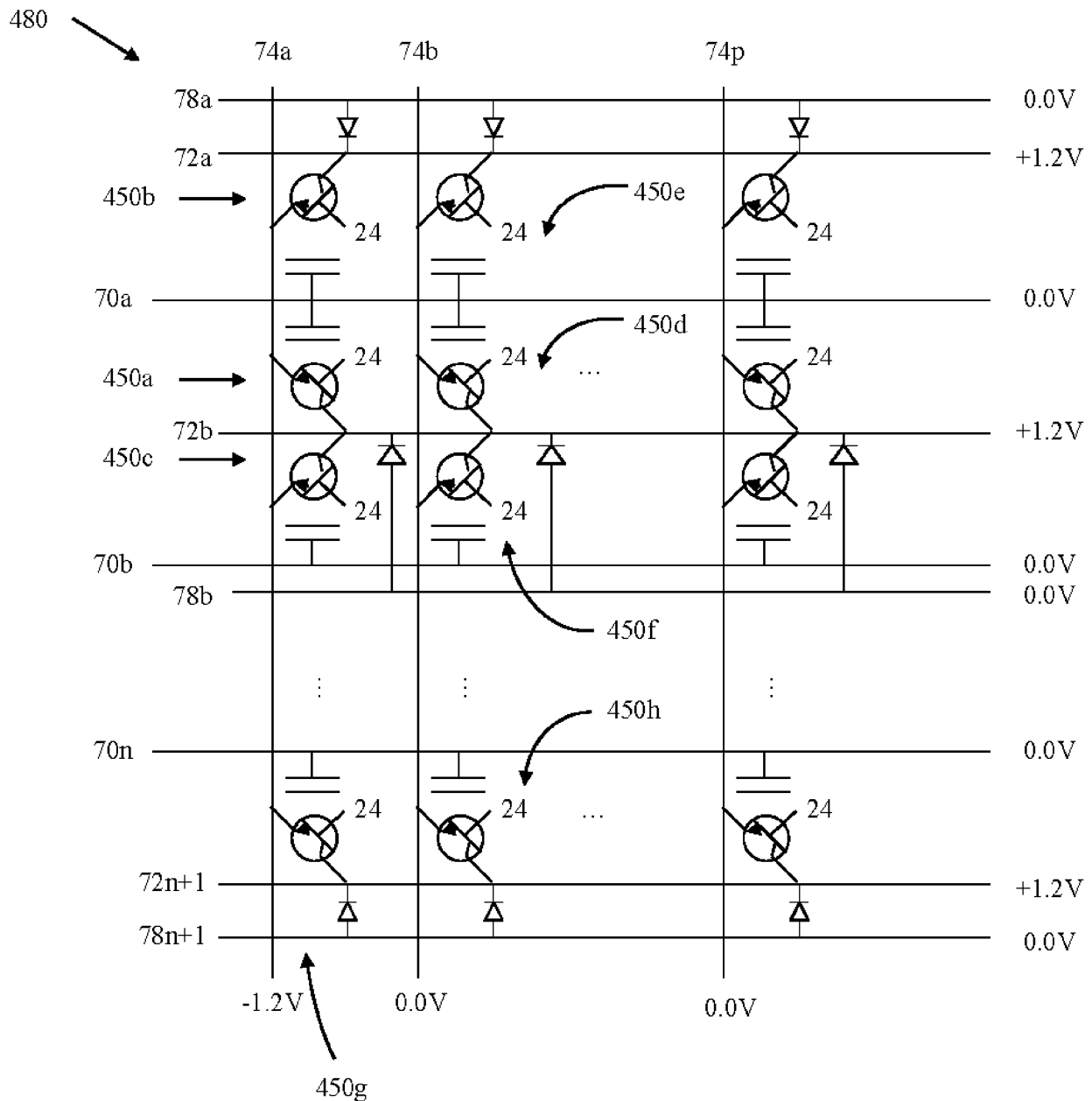


FIG. 67

Write Logic-0 Operation (Single Memory Cell 450a)

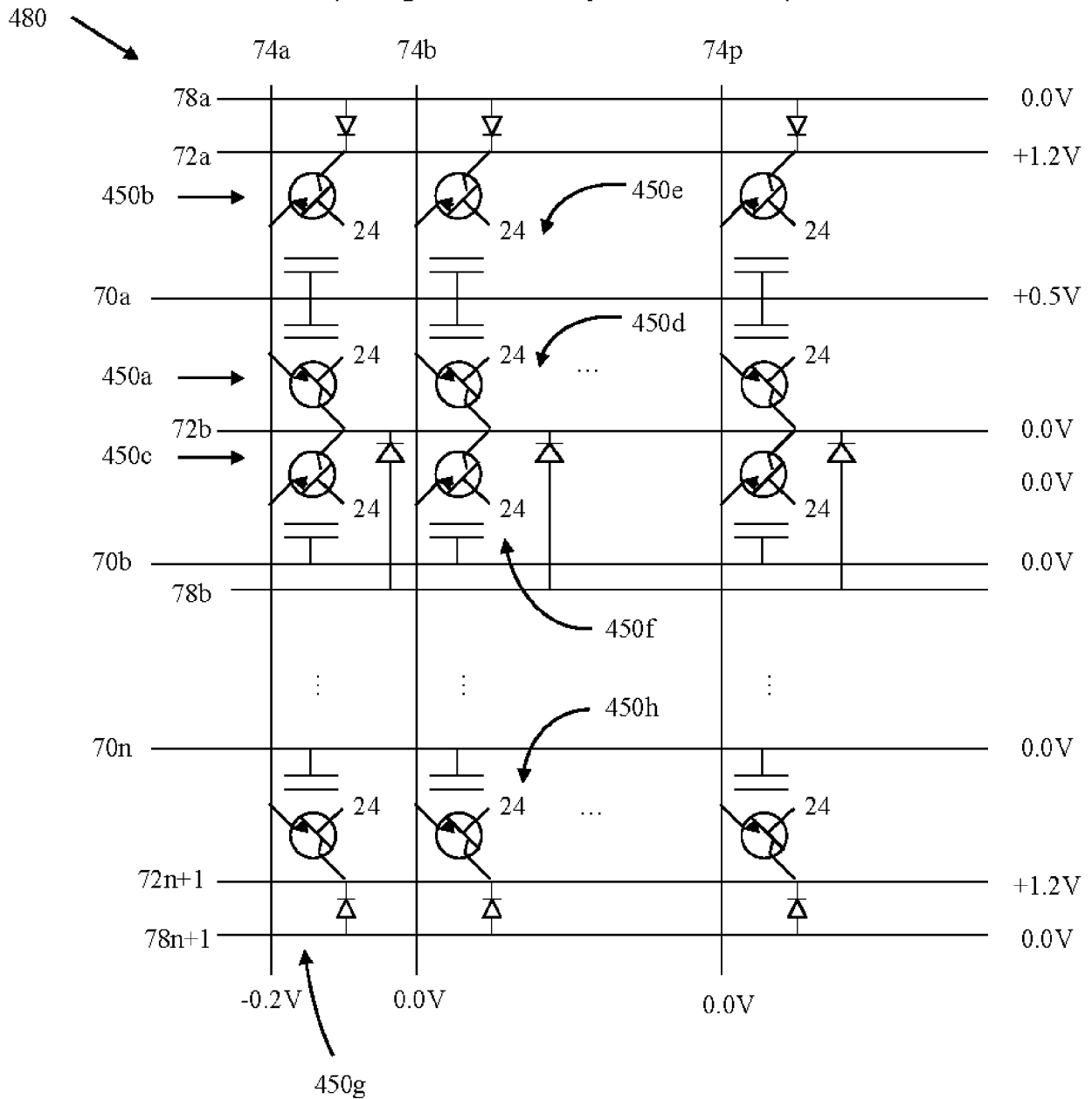


FIG. 68

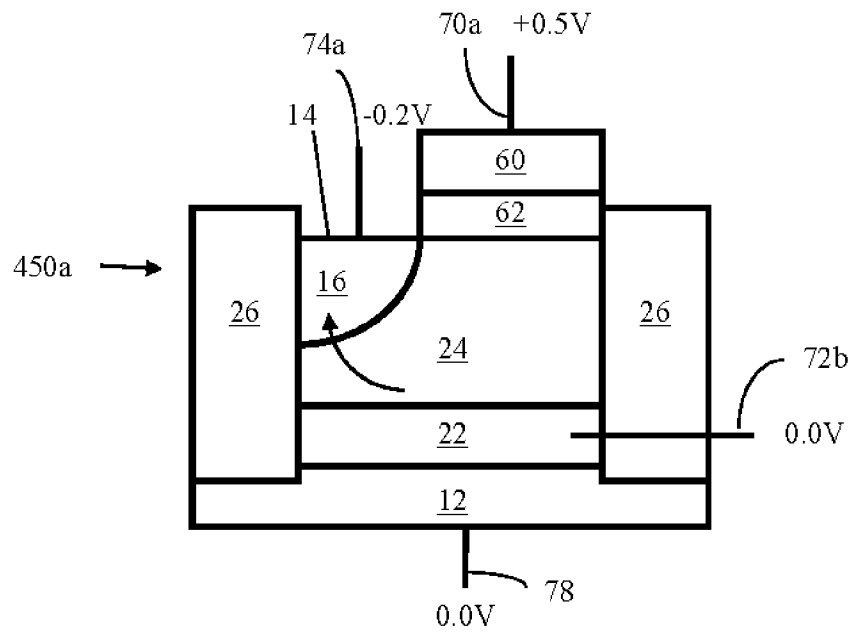


FIG. 69A

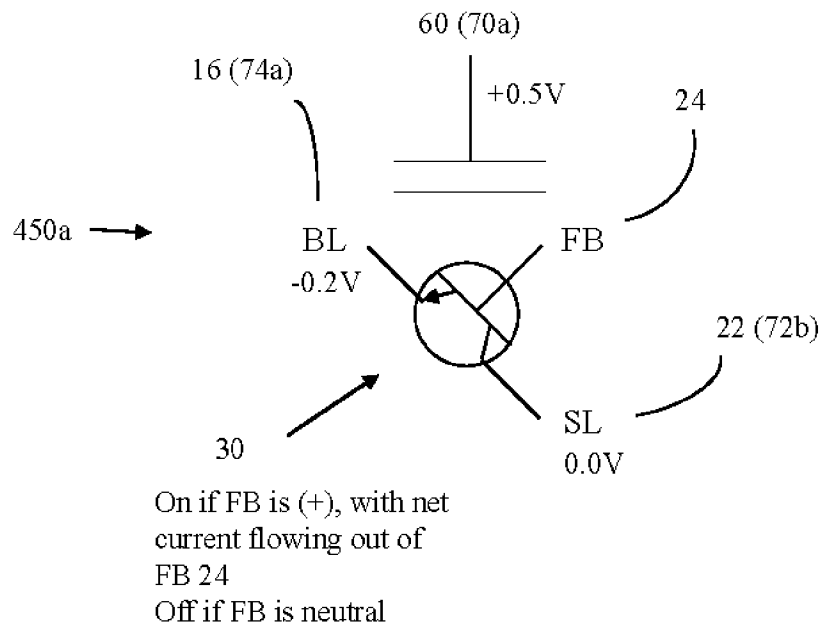


FIG. 69B

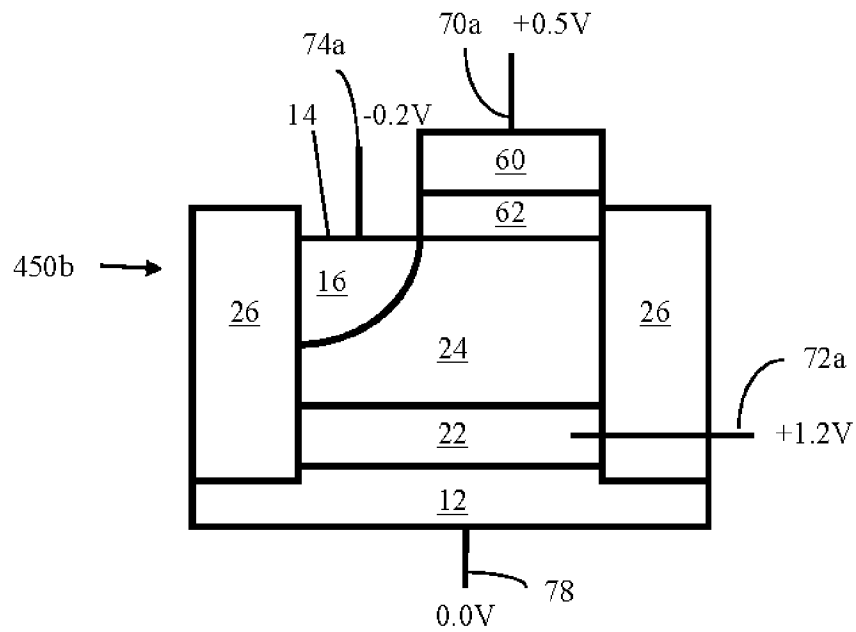
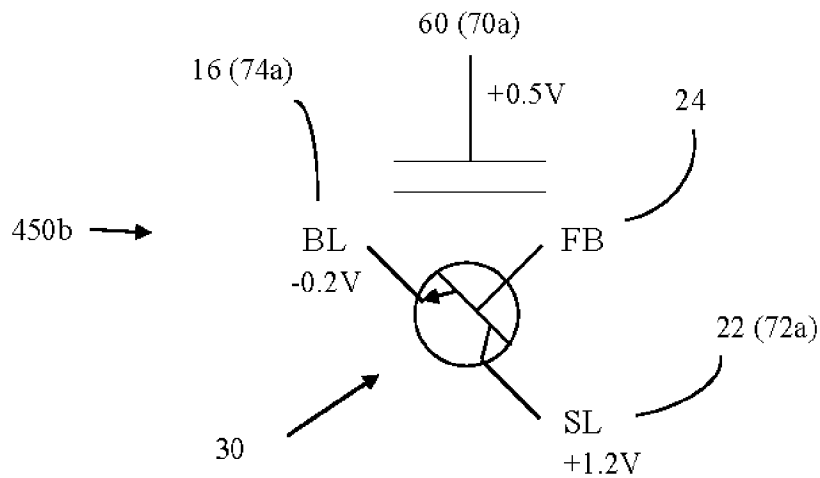


FIG. 69C



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 69D

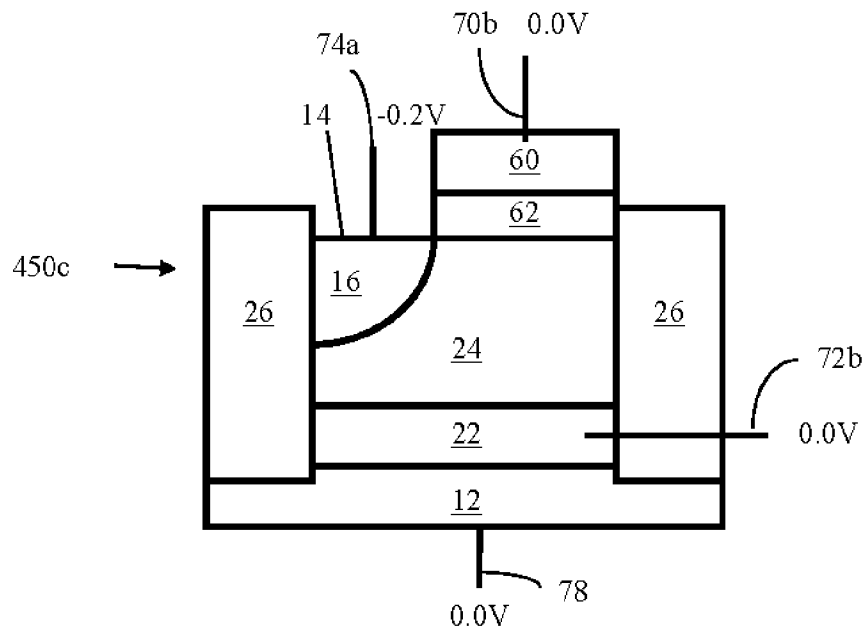


FIG. 69E

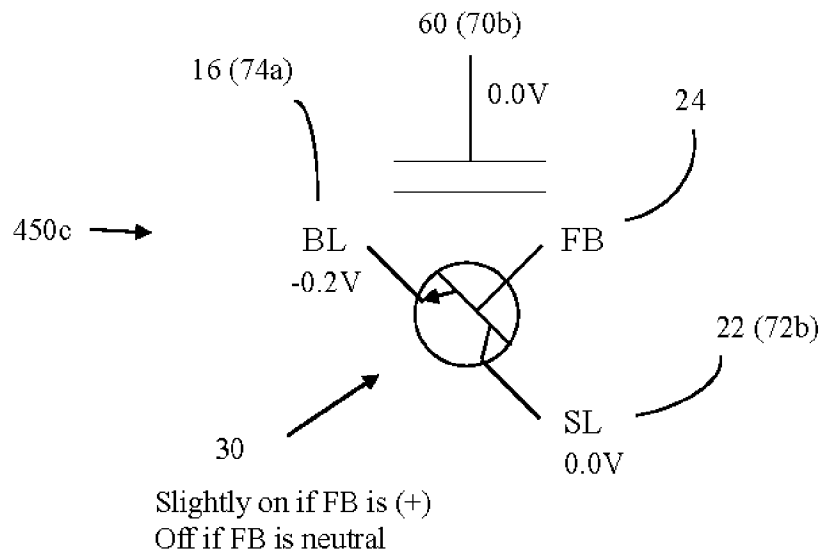


FIG. 69F

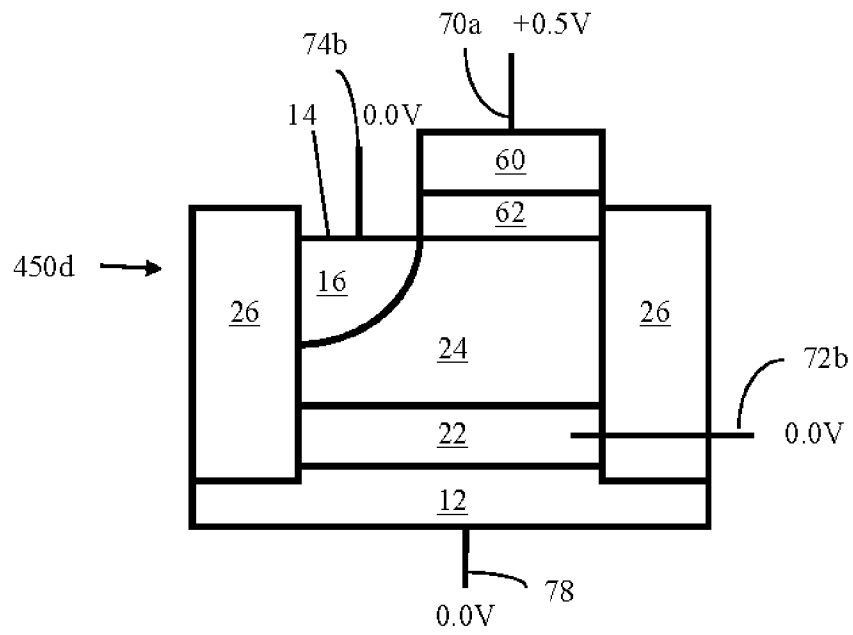


FIG. 69G

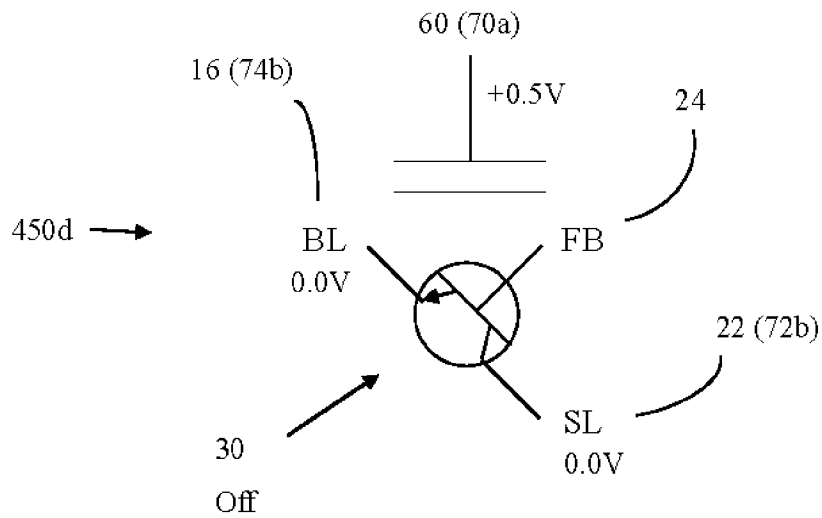


FIG. 69H

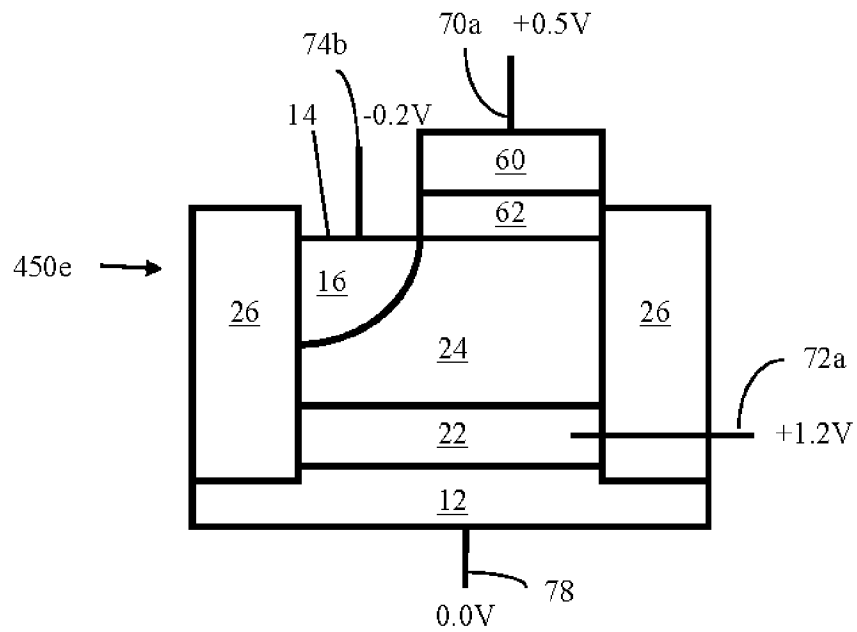
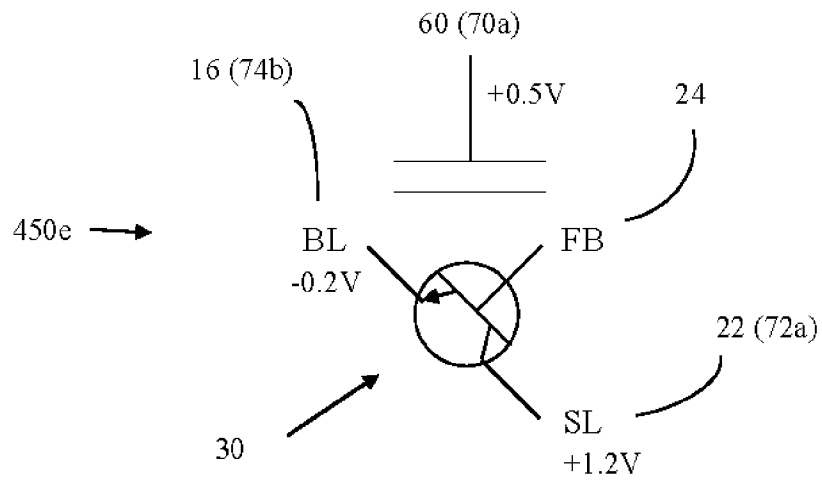


FIG. 69I



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 69J

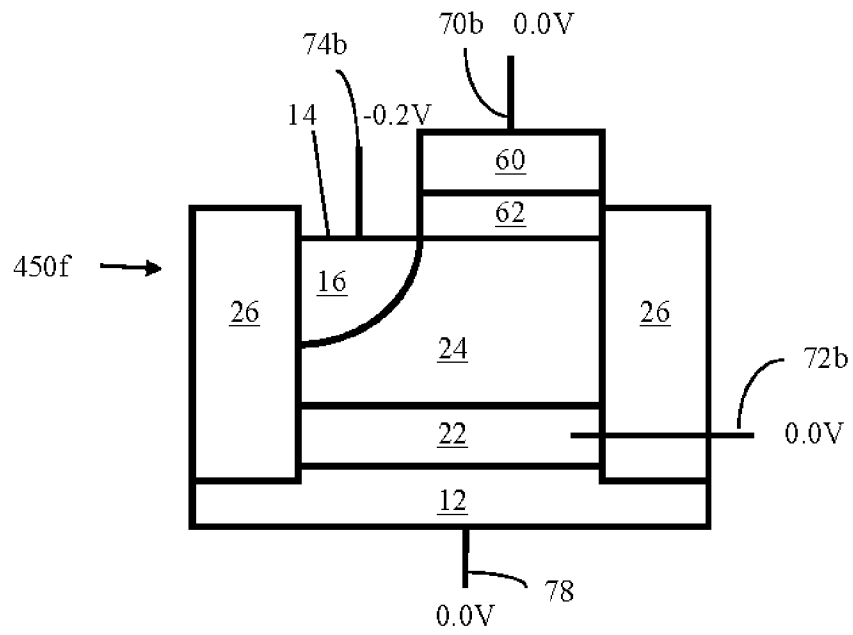


FIG. 69K

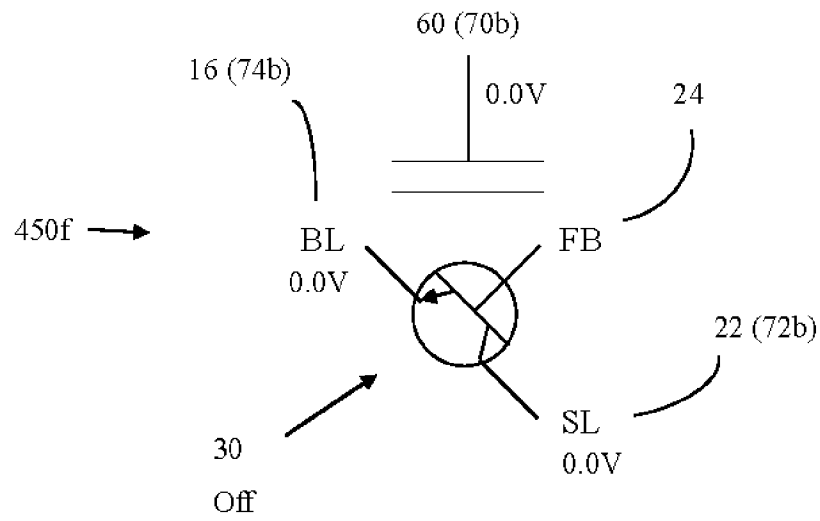


FIG. 69L

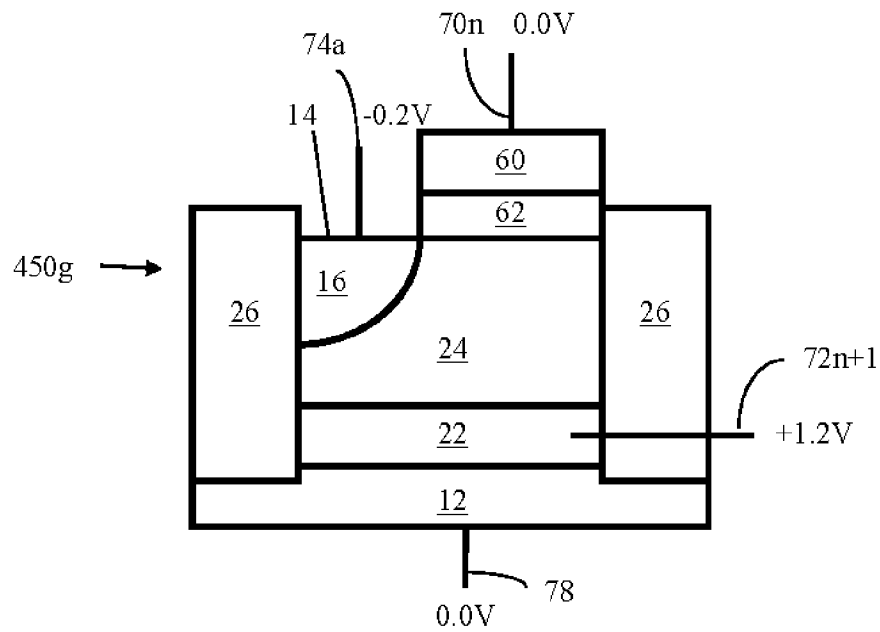
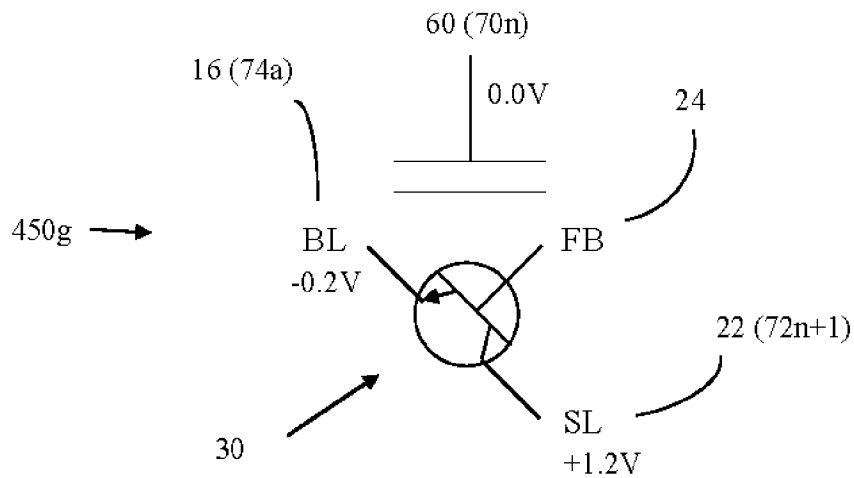


FIG. 69M



On if FB is (+); forward
bias current is balanced
by higher bipolar base
current
Off if FB is neutral

FIG. 69N

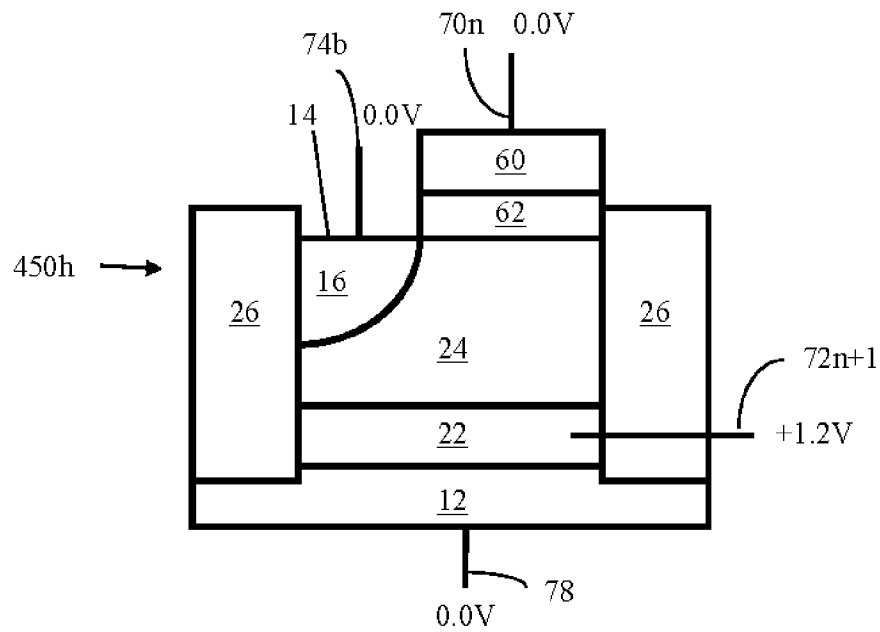


FIG. 69O

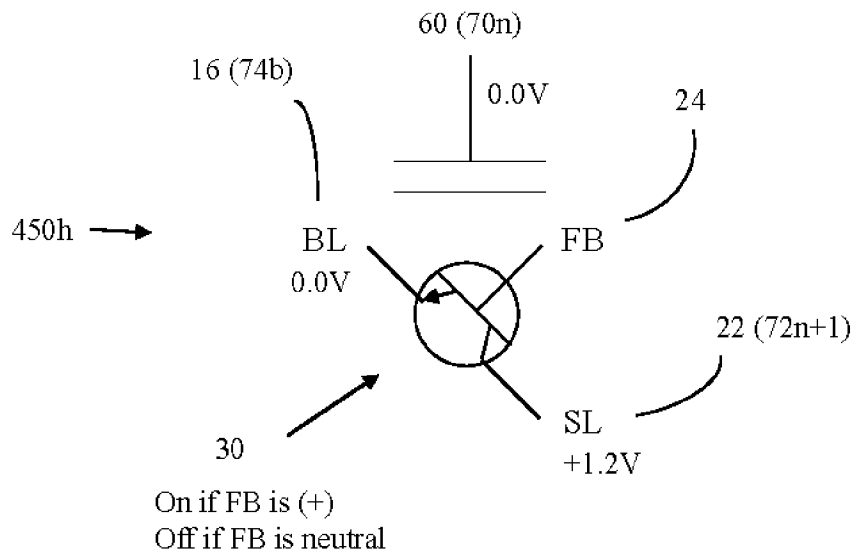


FIG. 69P

Write Logic-1 Operation – GIDL (Single Memory Cell 450a)

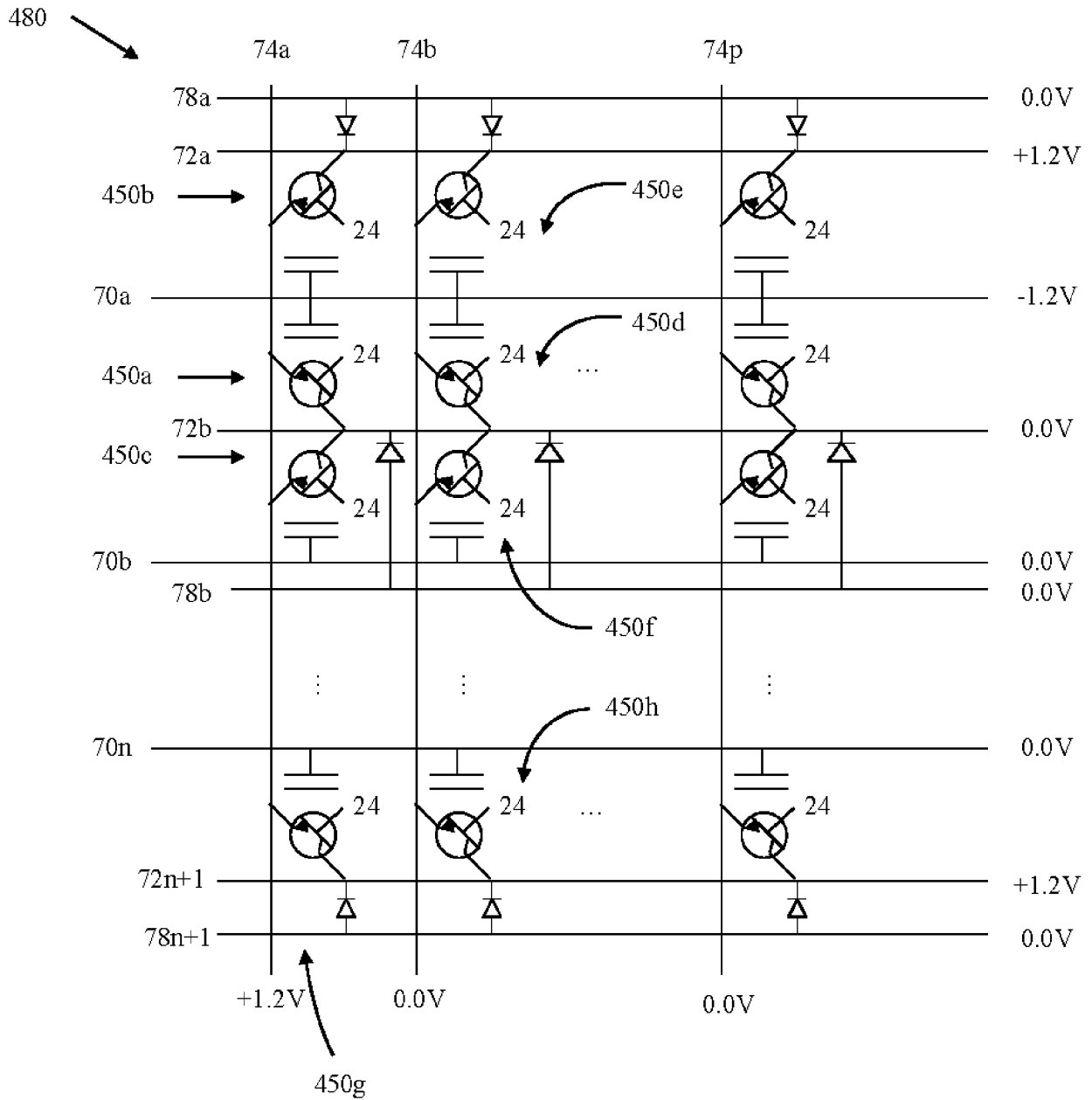


FIG. 70

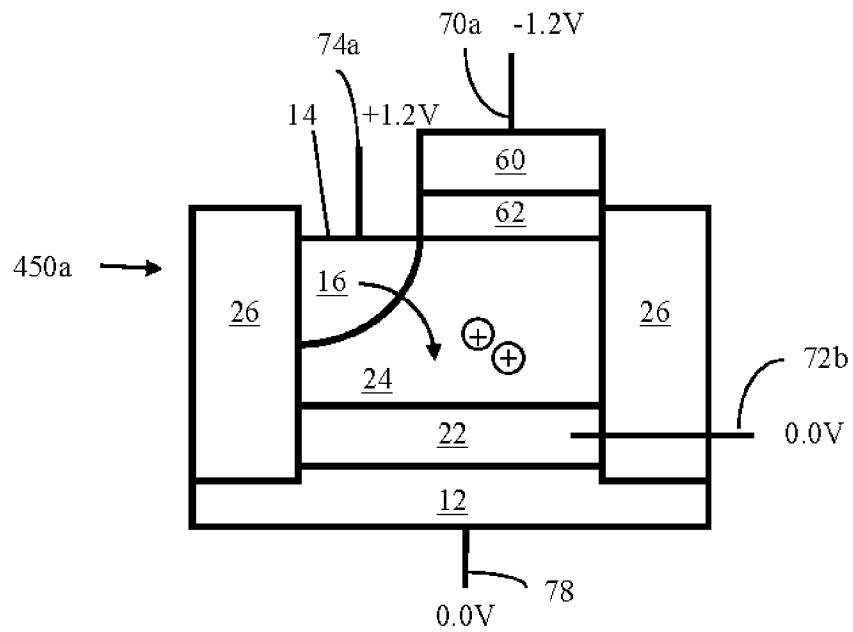


FIG. 71A

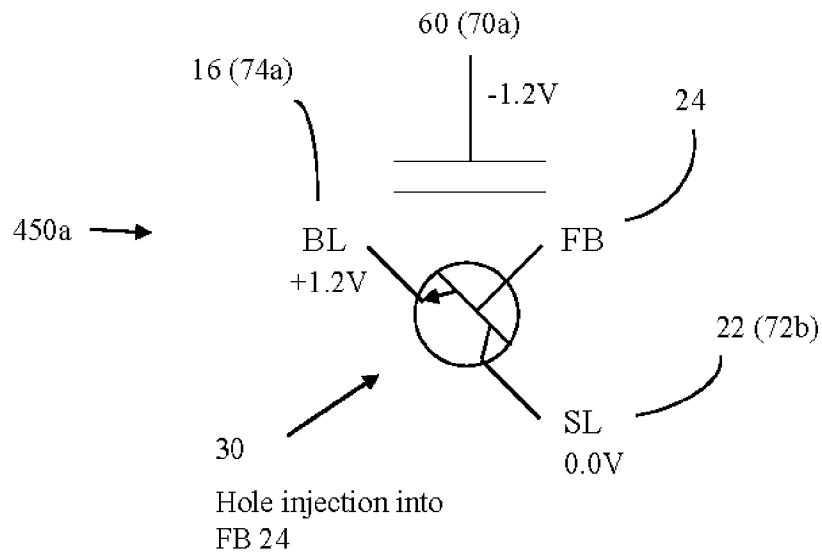


FIG. 71B

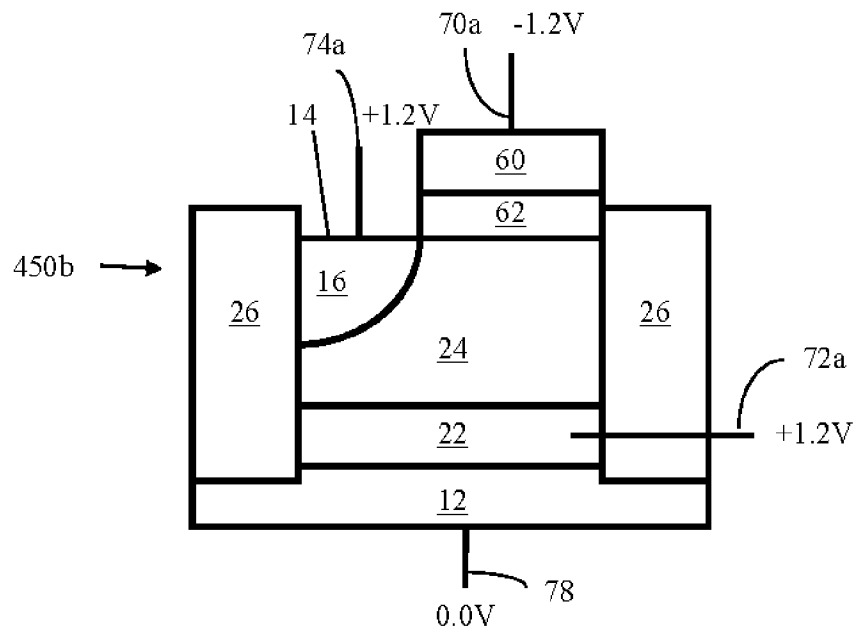


FIG. 71C

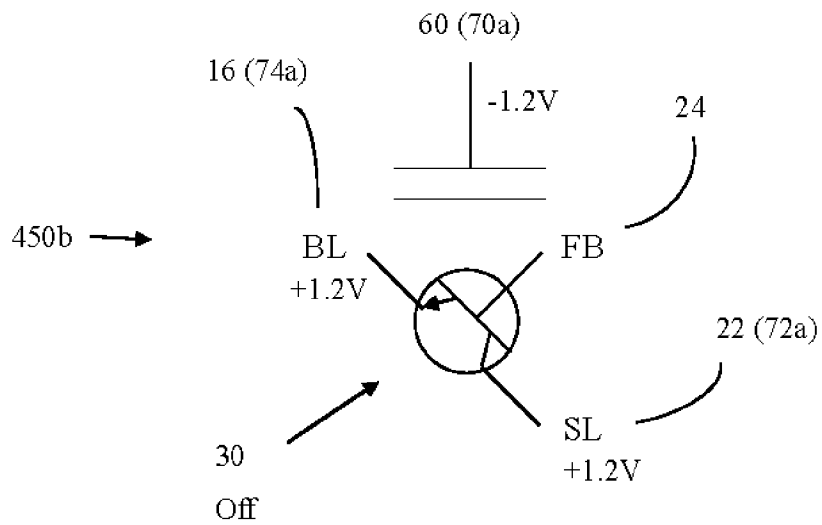


FIG. 71D

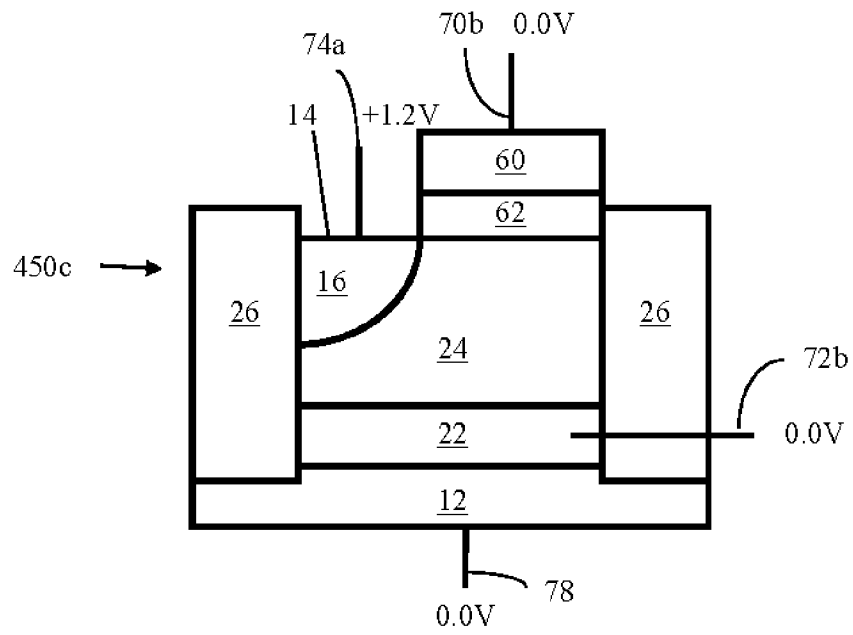


FIG. 71E

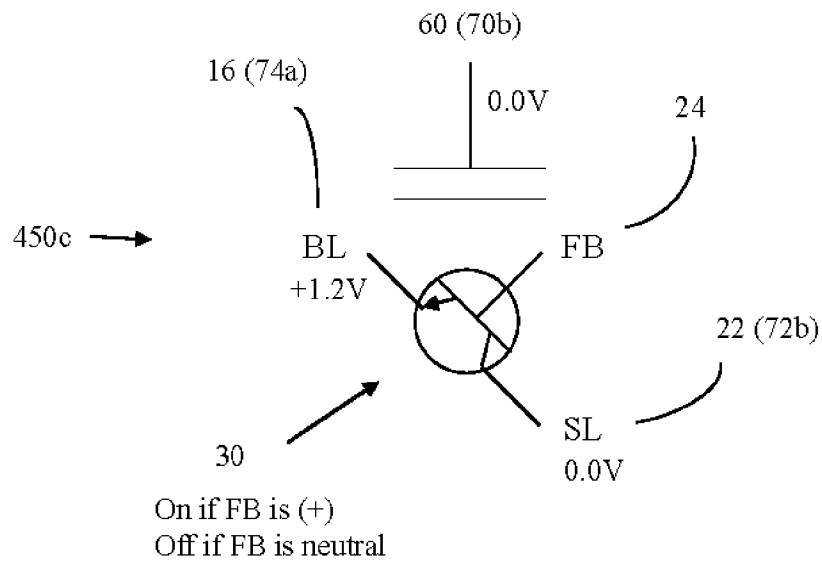


FIG. 71F

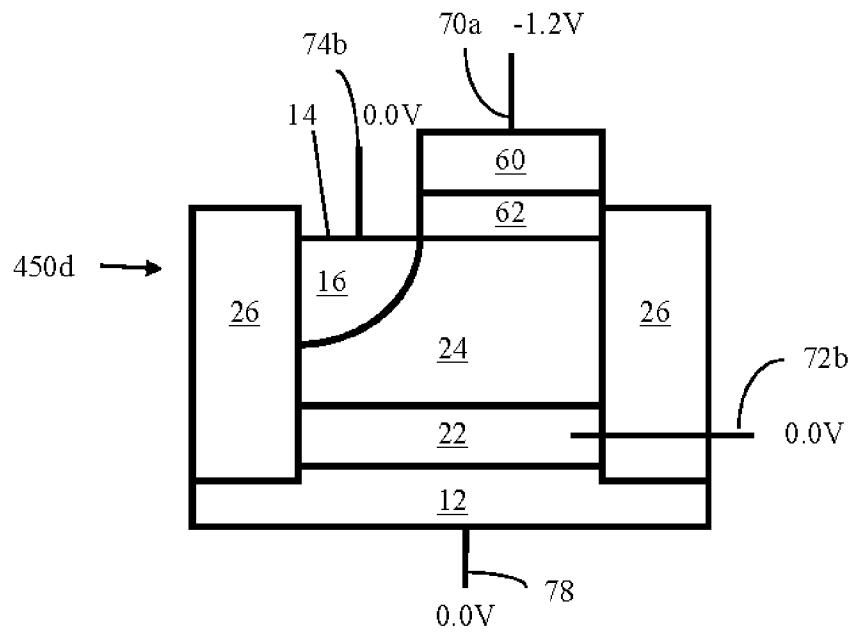


FIG. 71G

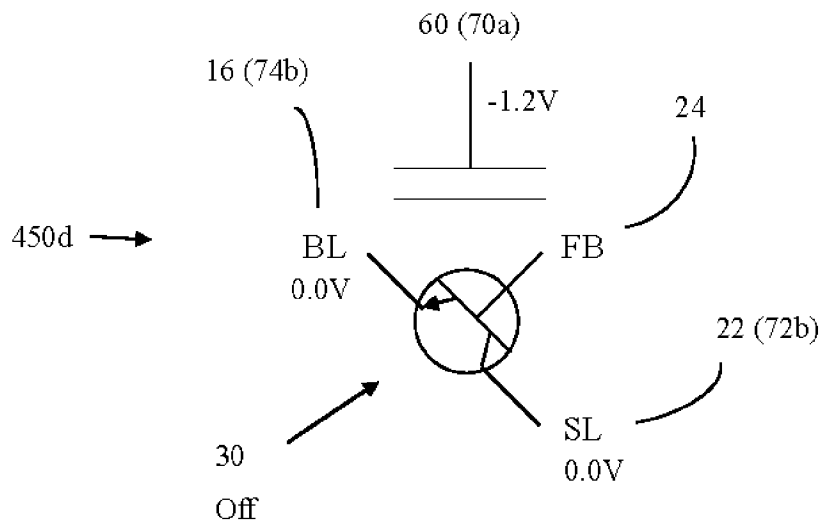


FIG. 71H

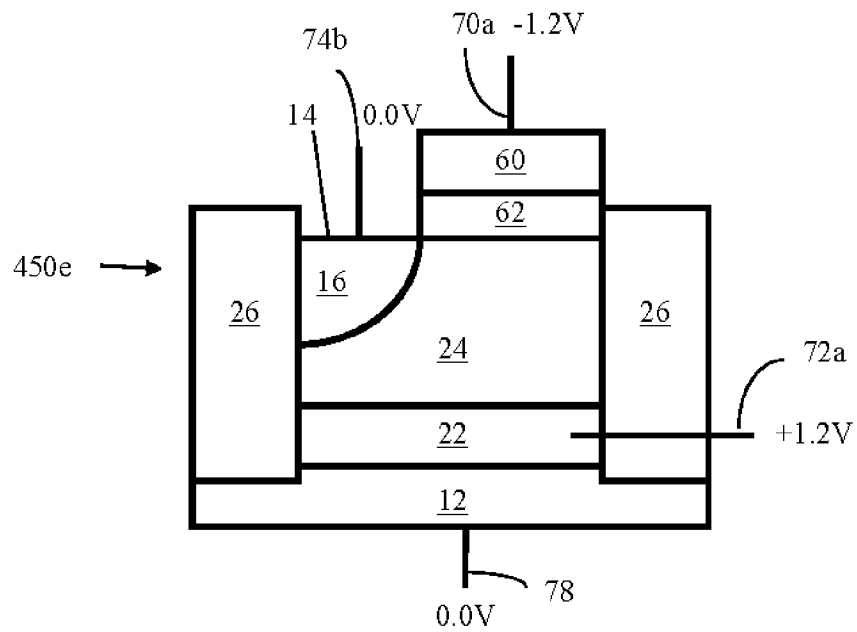


FIG. 71I

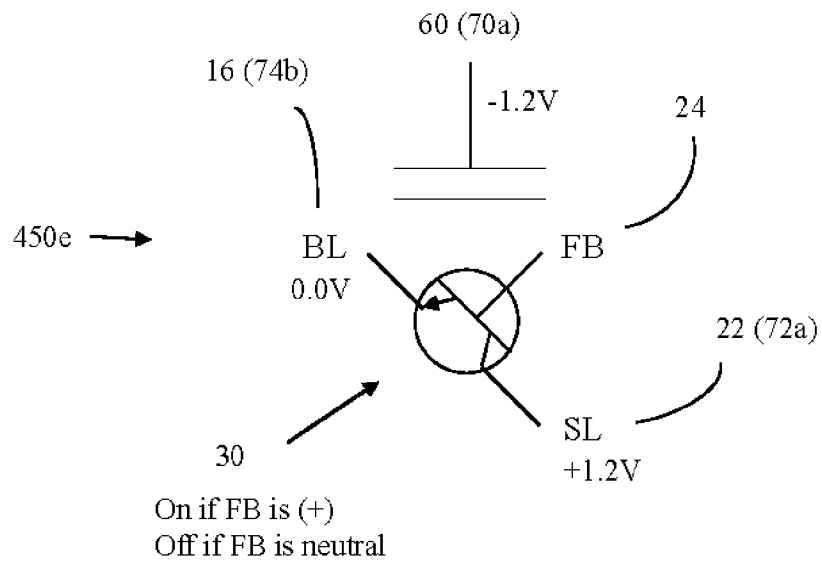


FIG. 71J

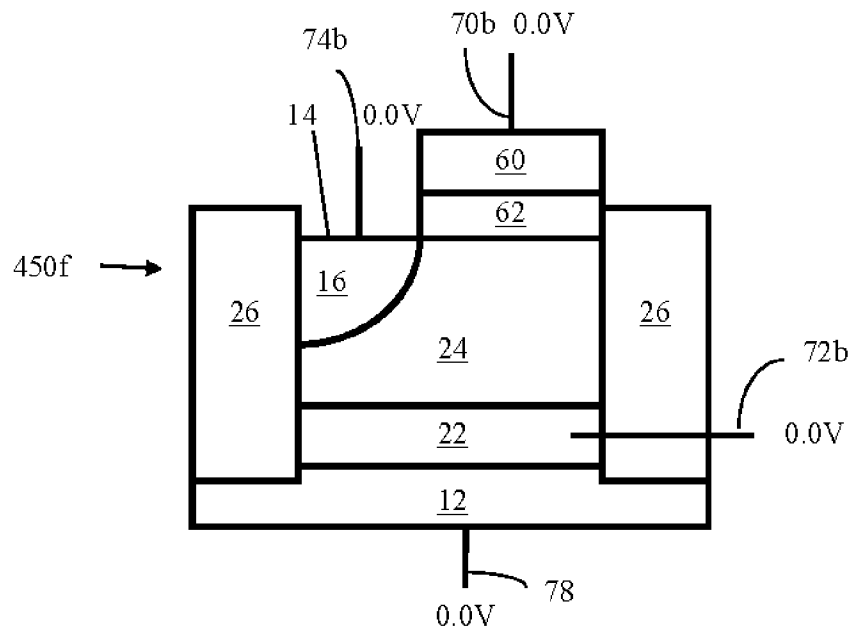


FIG. 71K

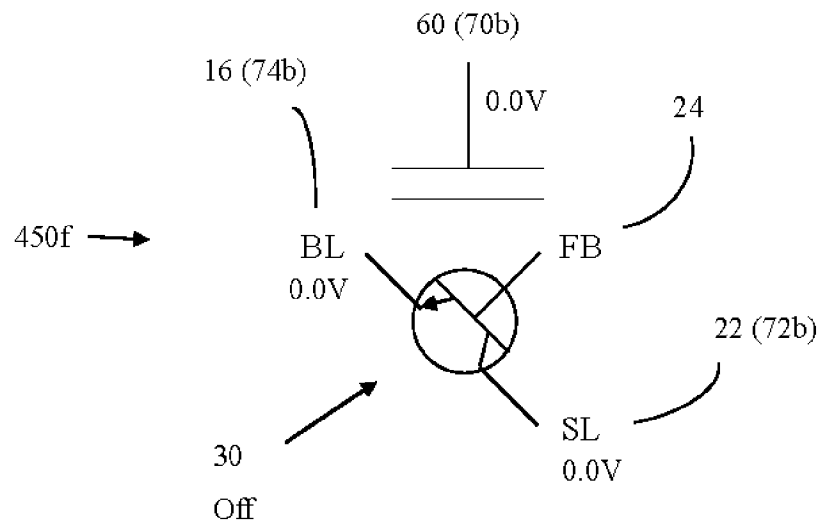


FIG. 71L

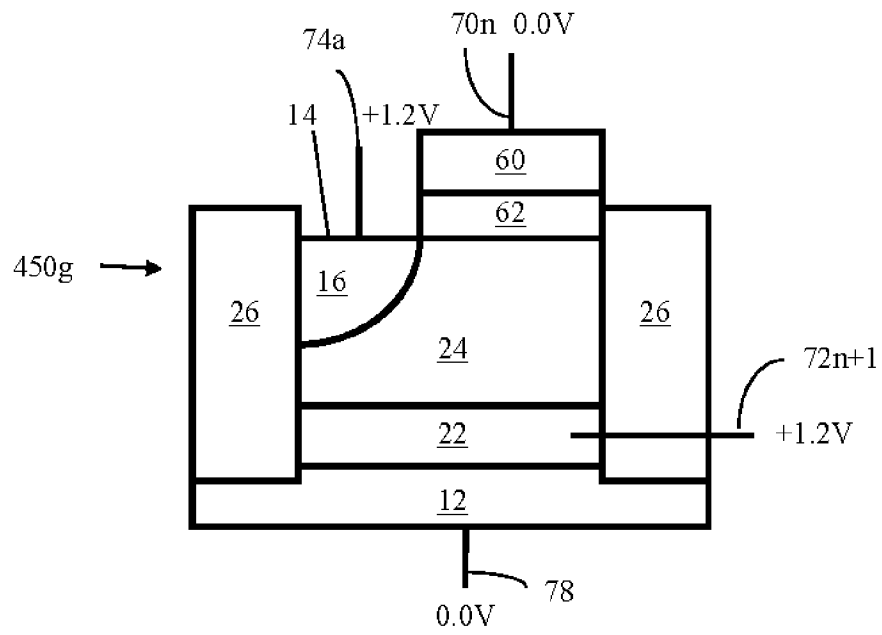


FIG. 71M

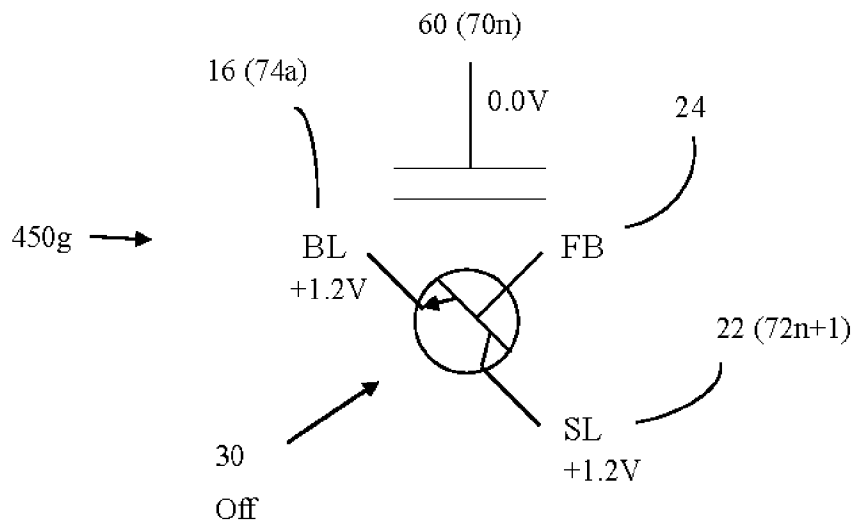


FIG. 71N

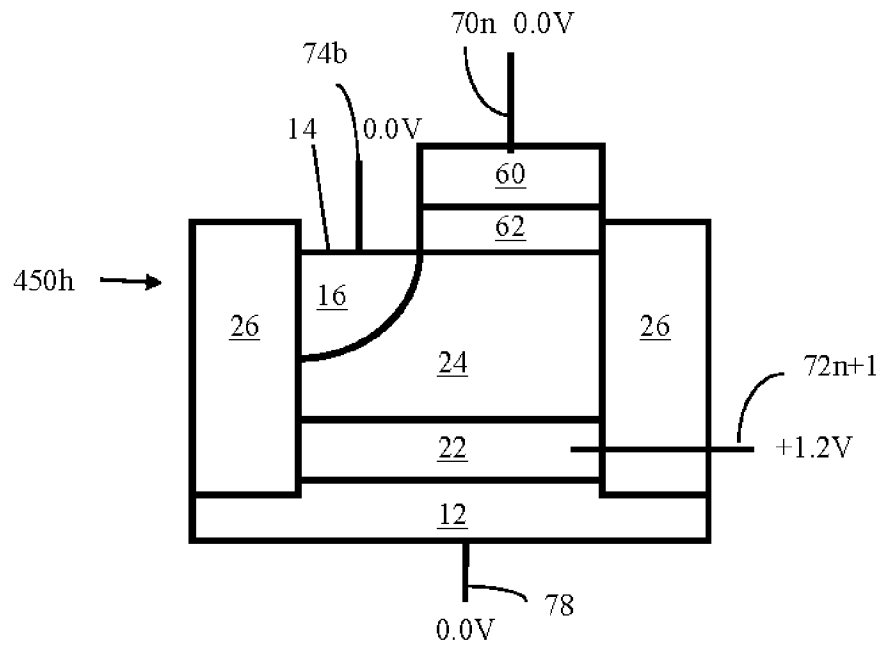


FIG. 71O

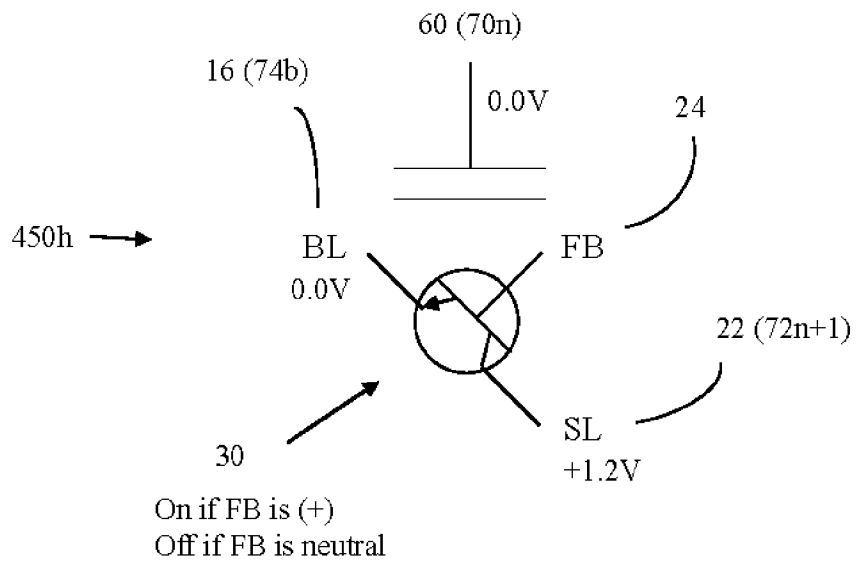


FIG. 71P

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 450a)

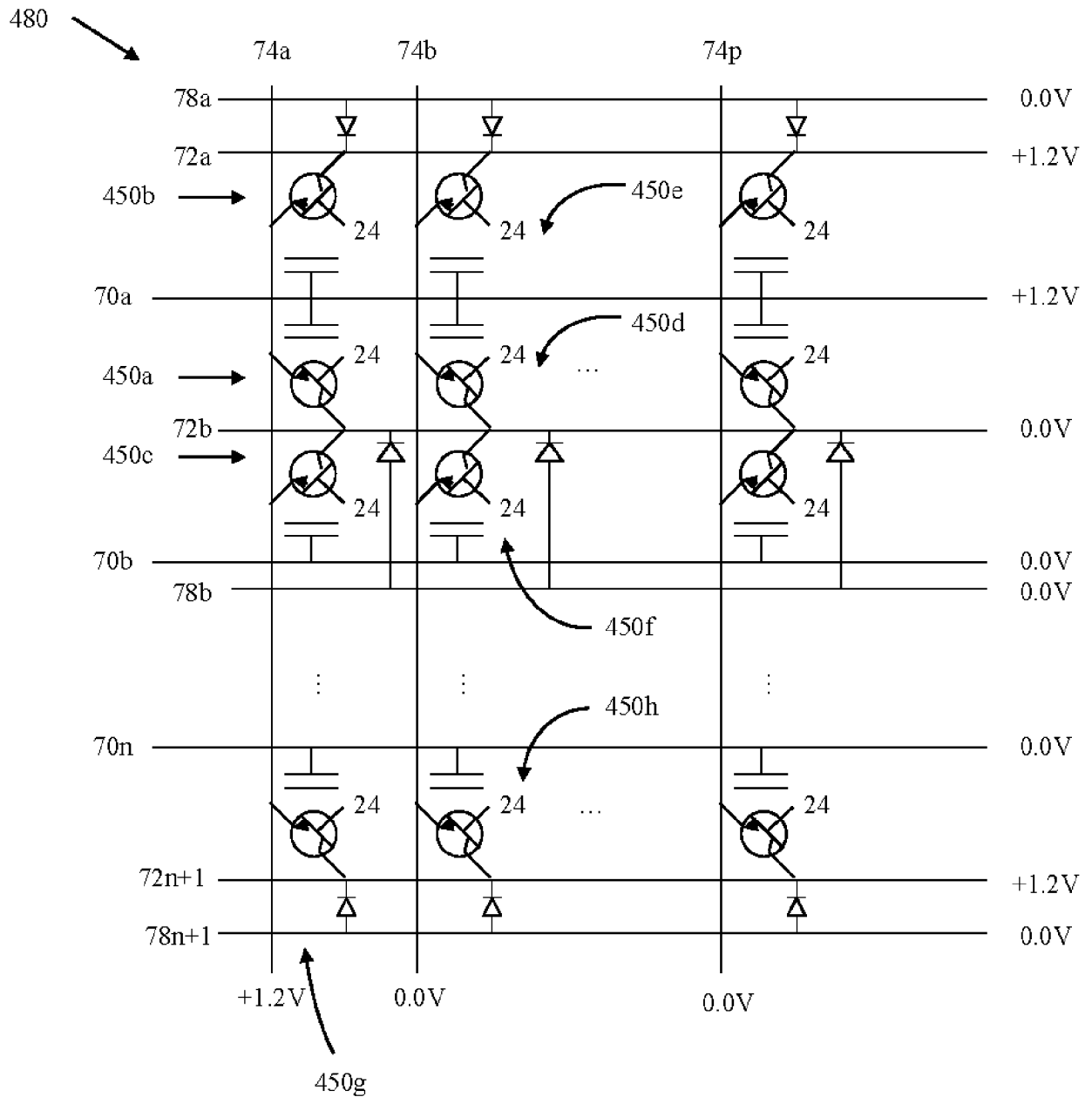


FIG. 72

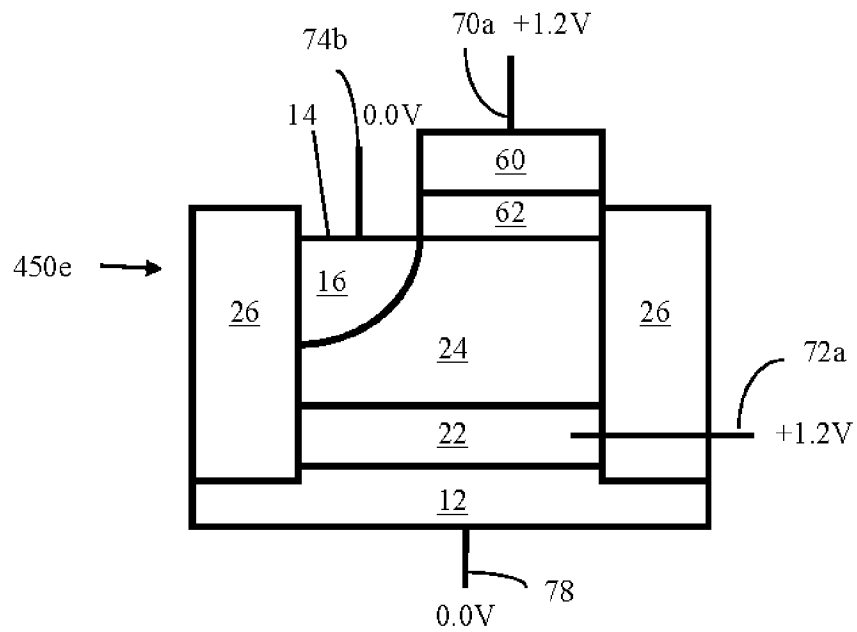


FIG. 73A

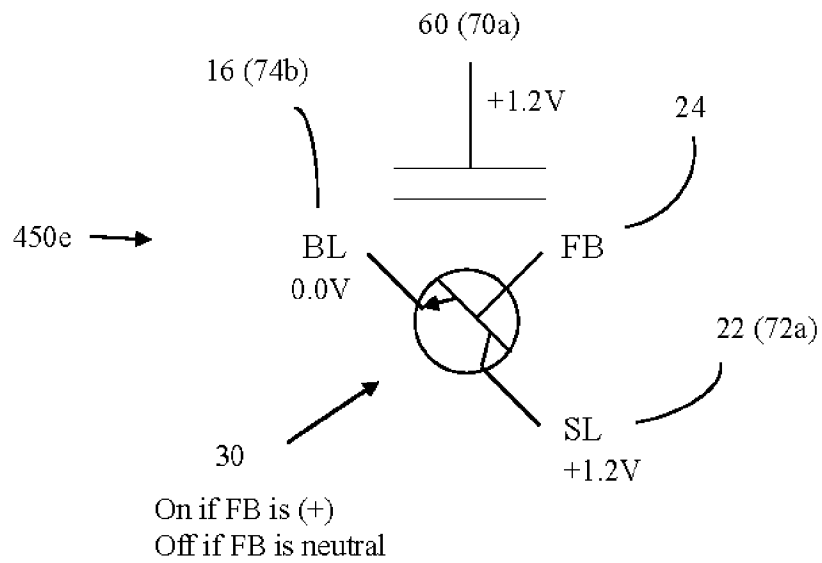


FIG. 73B

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 450a)

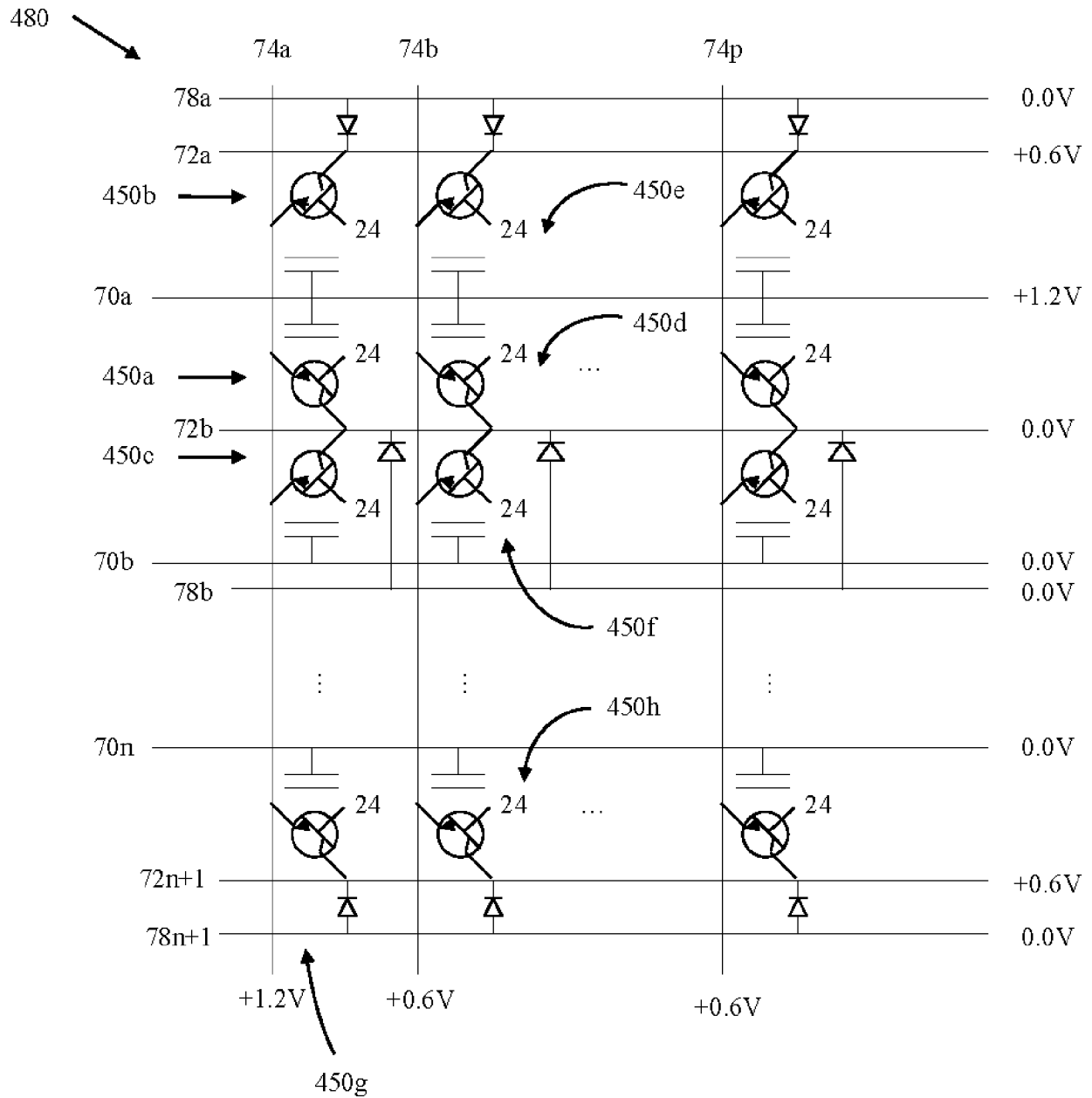


FIG. 74

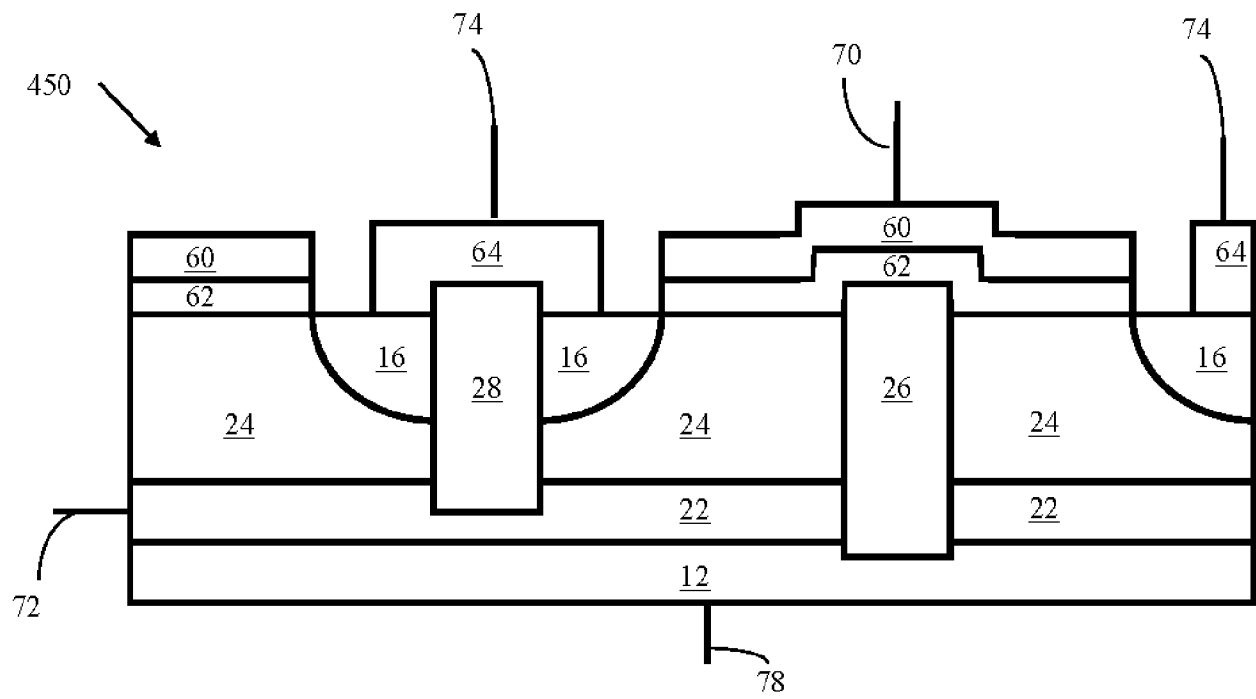


FIG. 75A

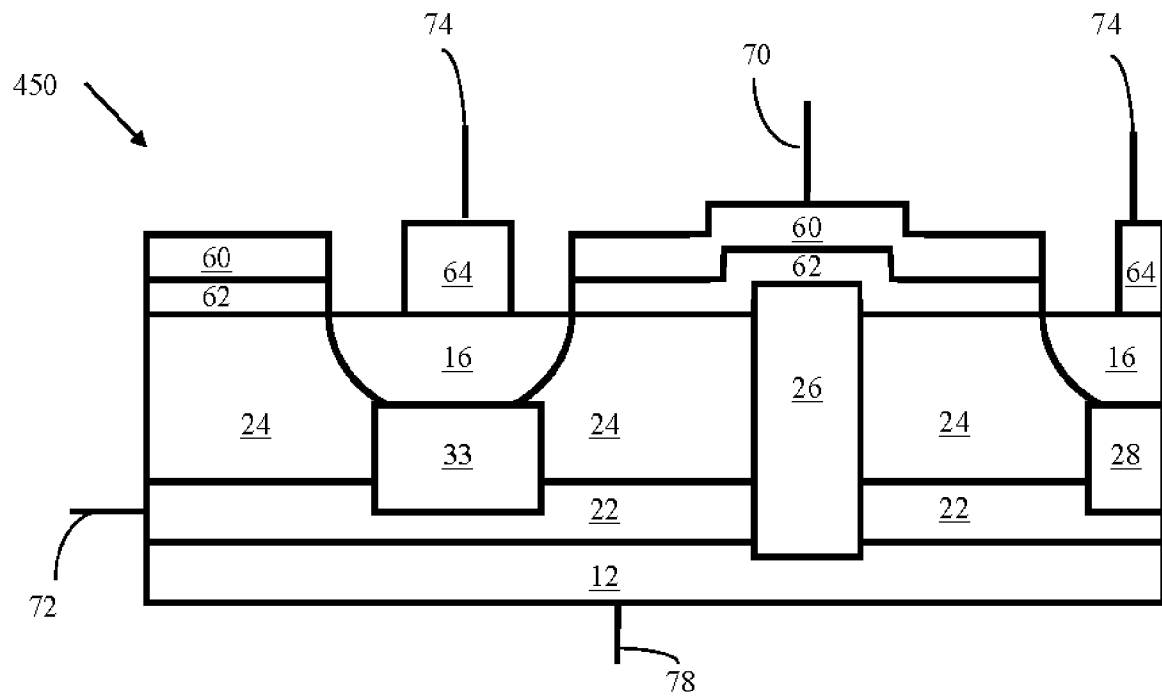


FIG. 75B

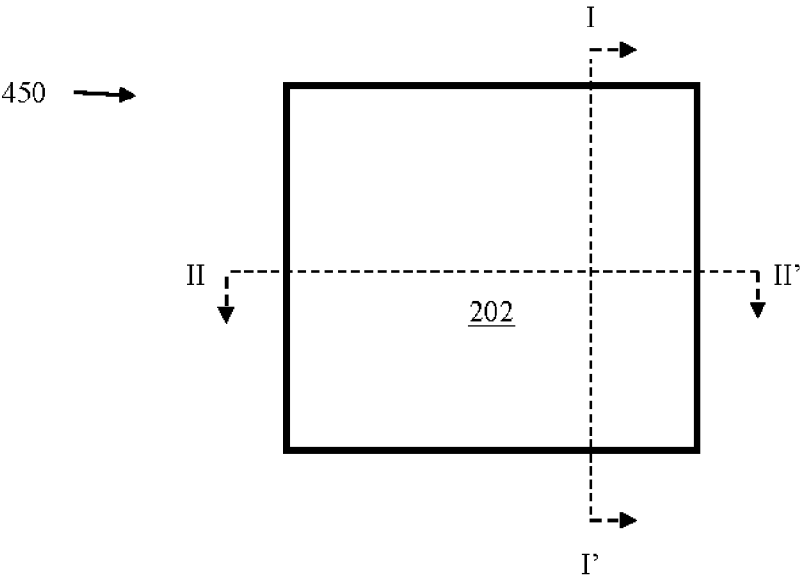


FIG. 76A

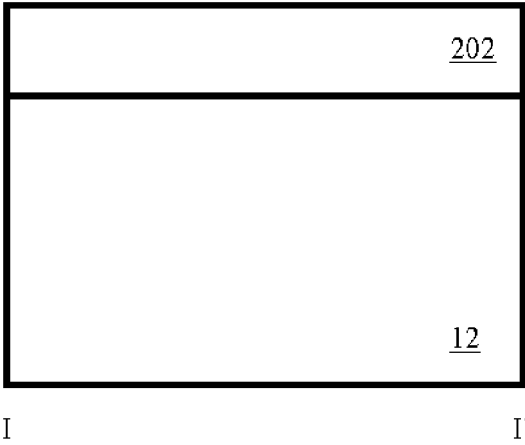


FIG. 76B

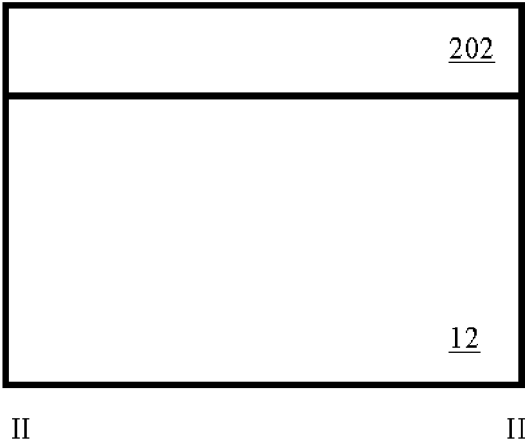


FIG. 76C

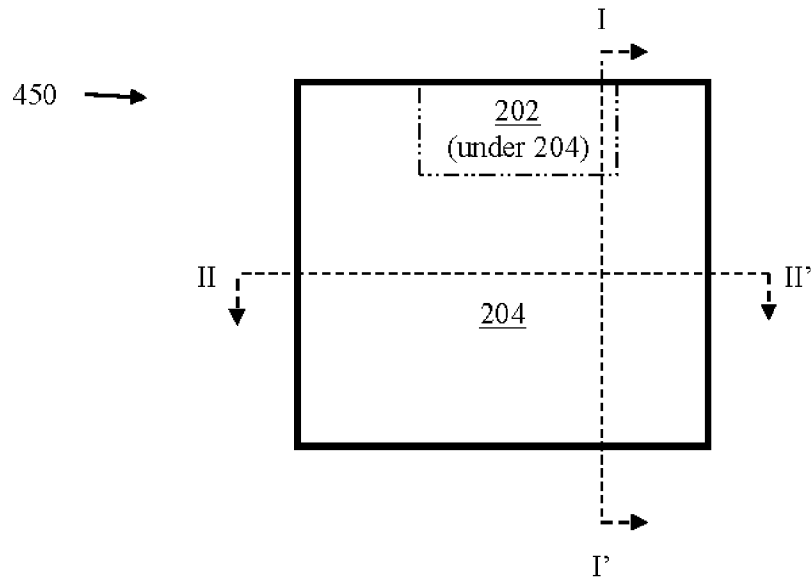


FIG. 76D

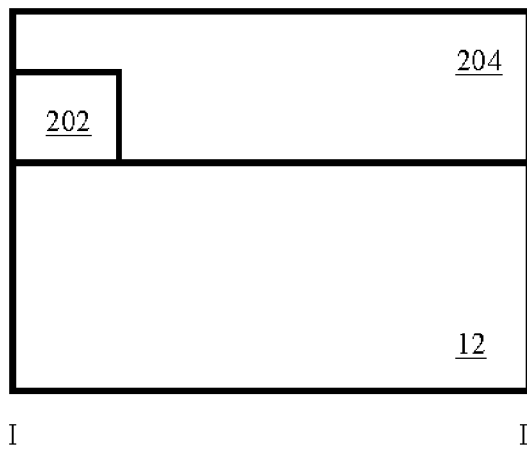


FIG. 76E

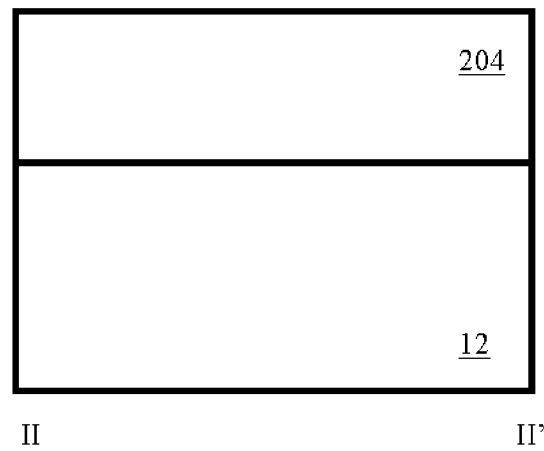


FIG. 76F

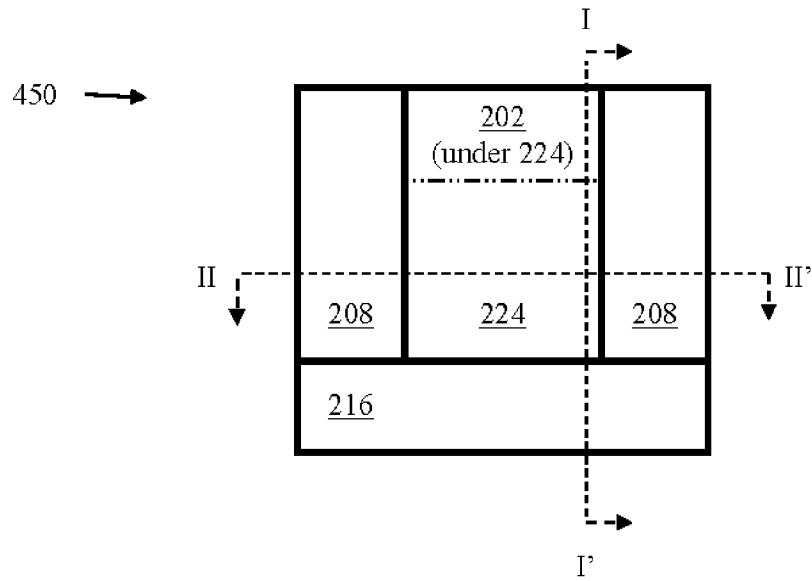


FIG. 76G

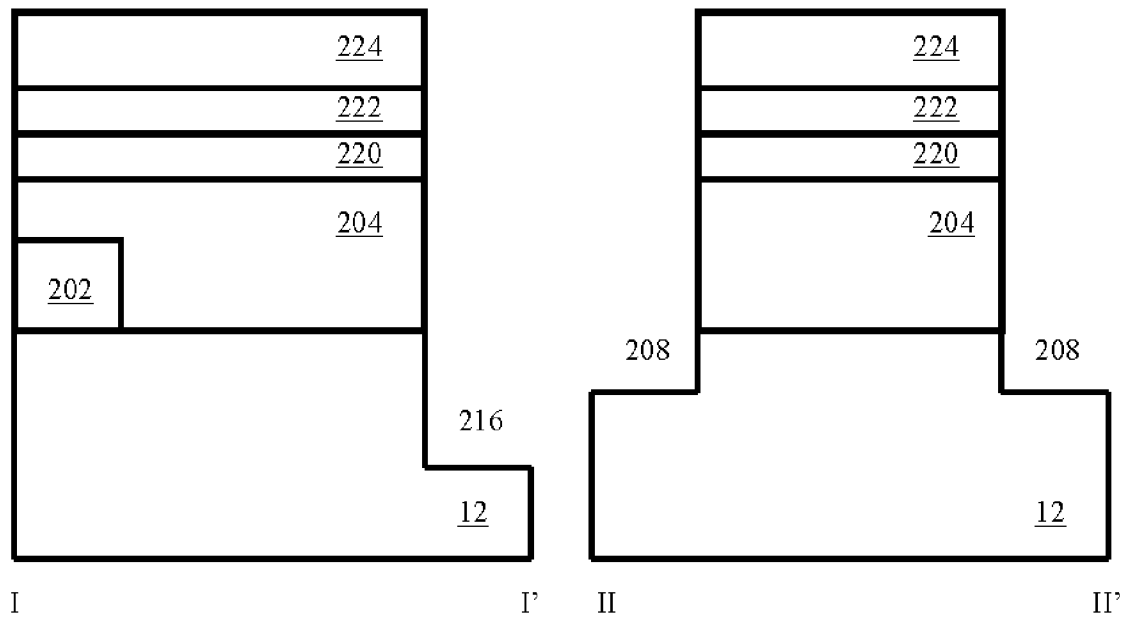


FIG. 76H

FIG. 76I

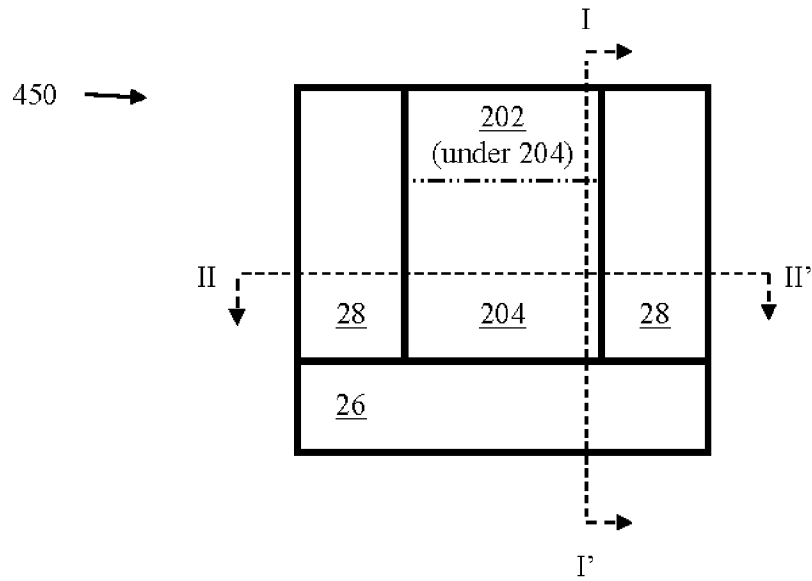


FIG. 76J

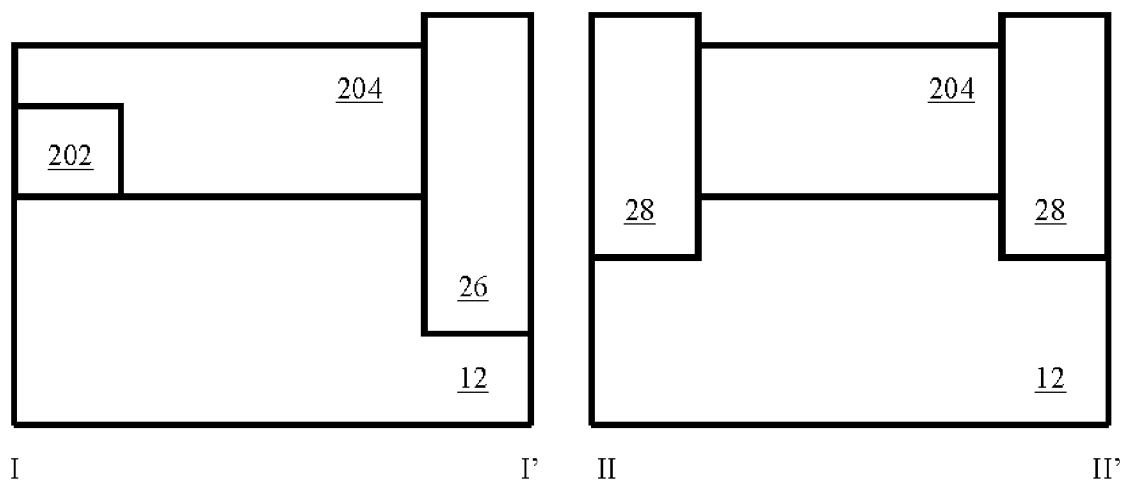


FIG. 76K

FIG. 76L

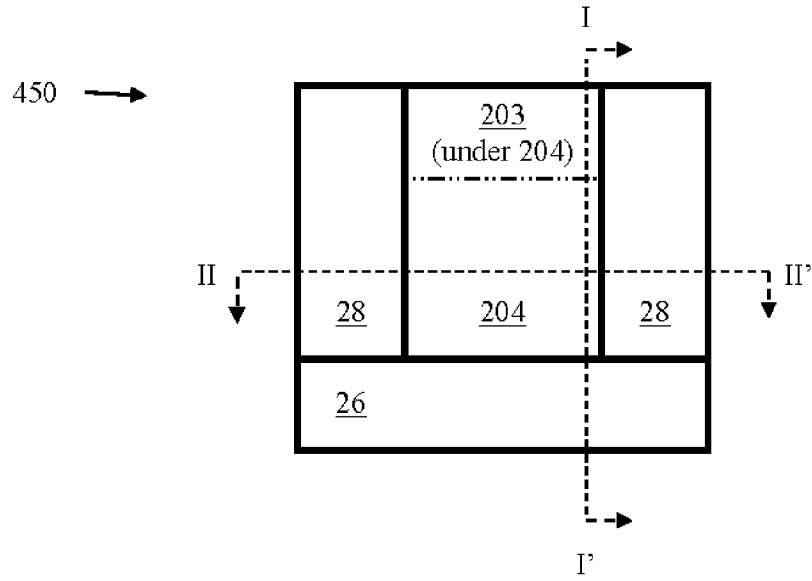


FIG. 76M

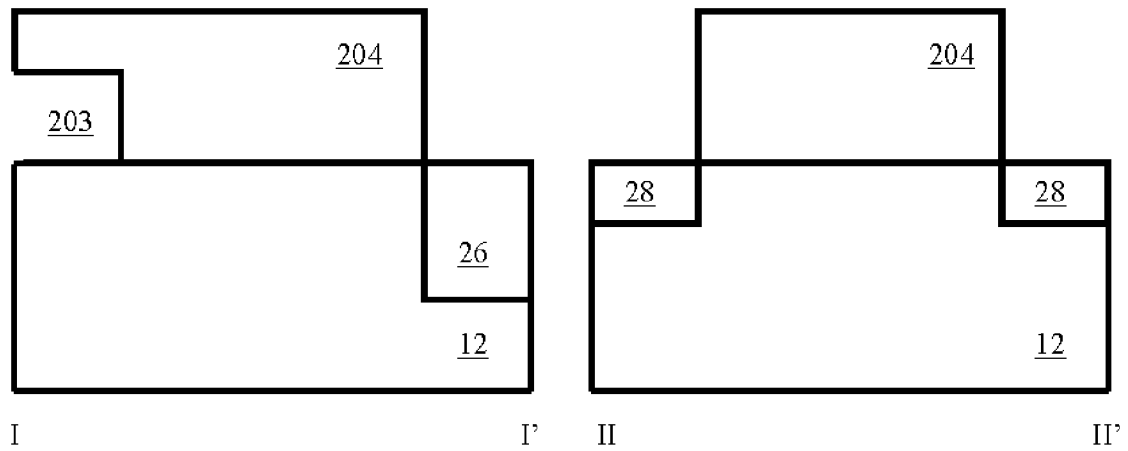


FIG. 76N

FIG. 76O

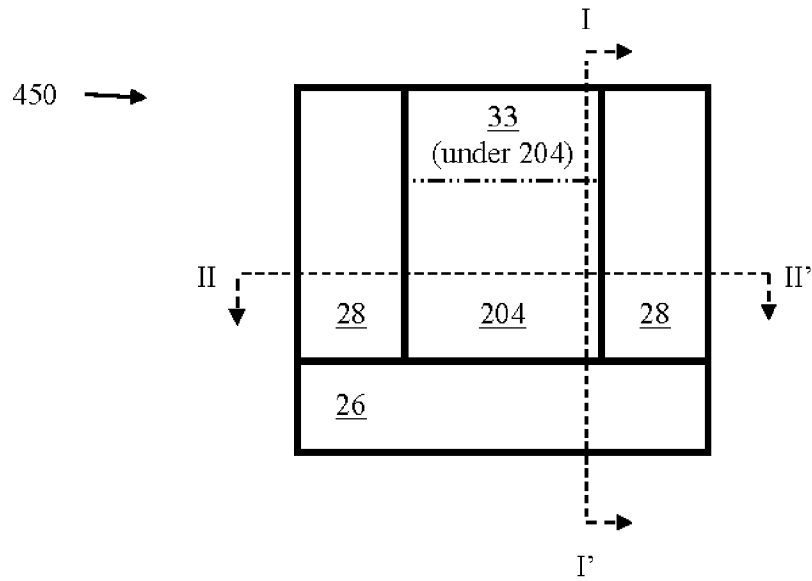


FIG. 76P

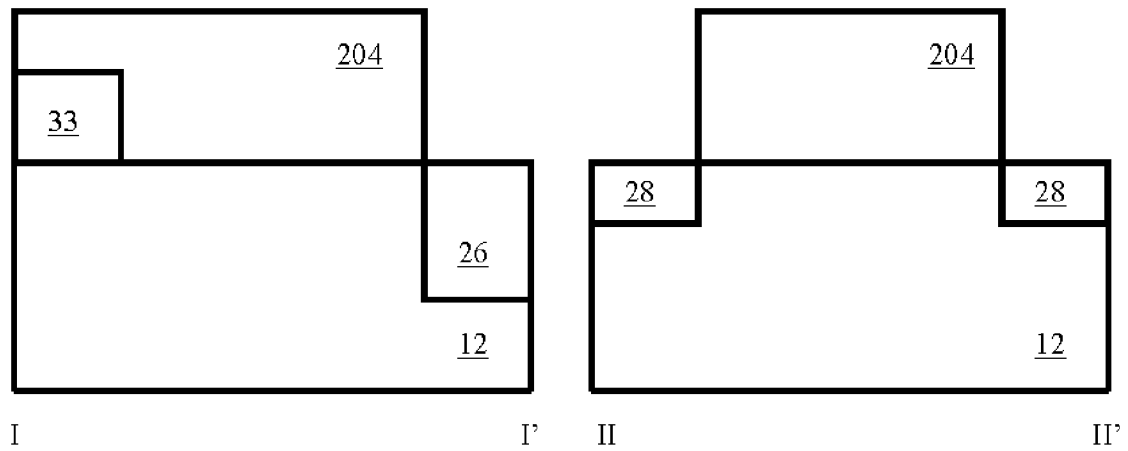


FIG. 76Q

FIG. 76R

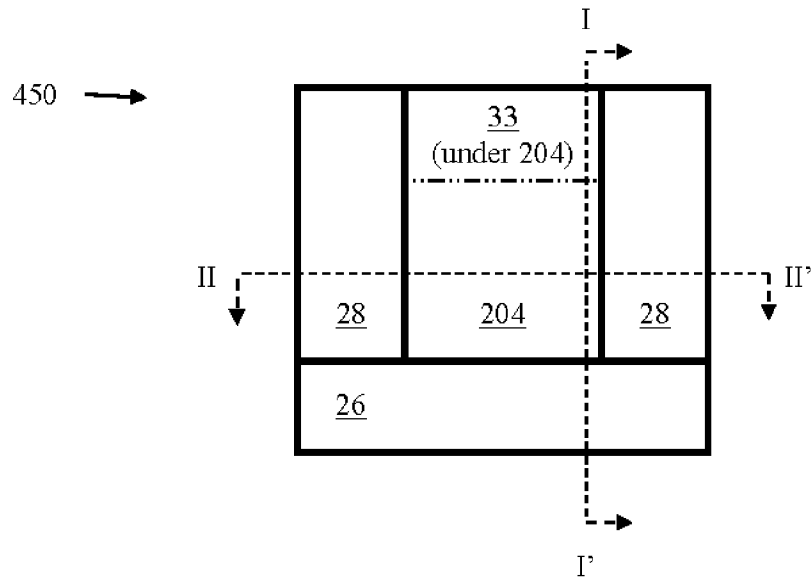


FIG. 76S

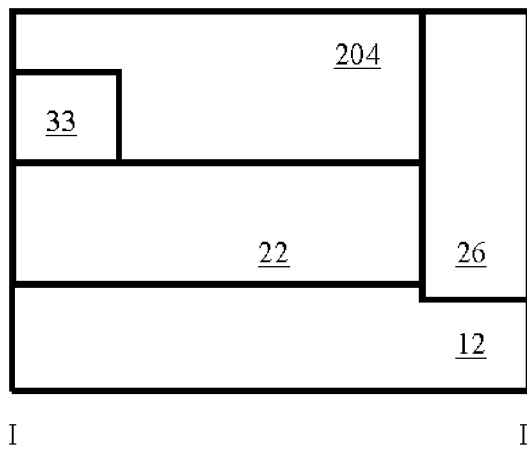


FIG. 76T

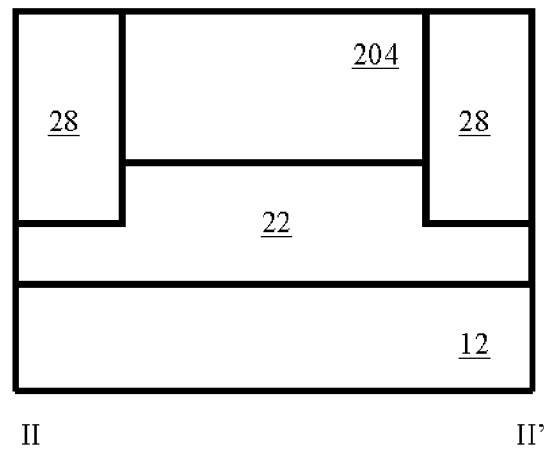


FIG. 76U

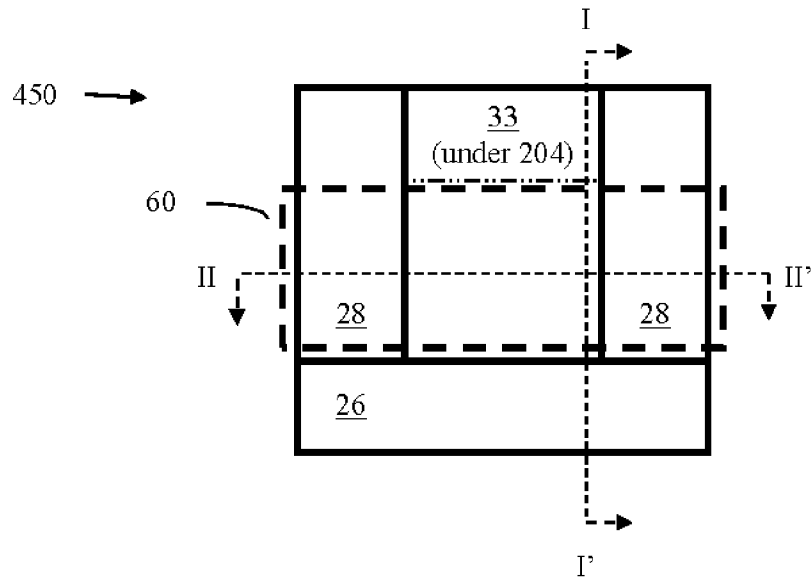


FIG. 76V

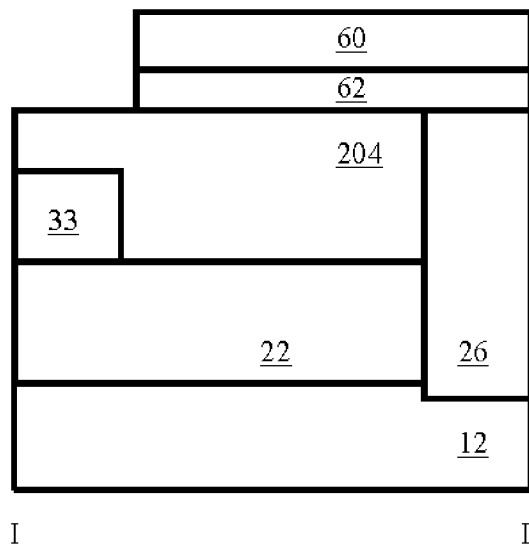


FIG. 76W

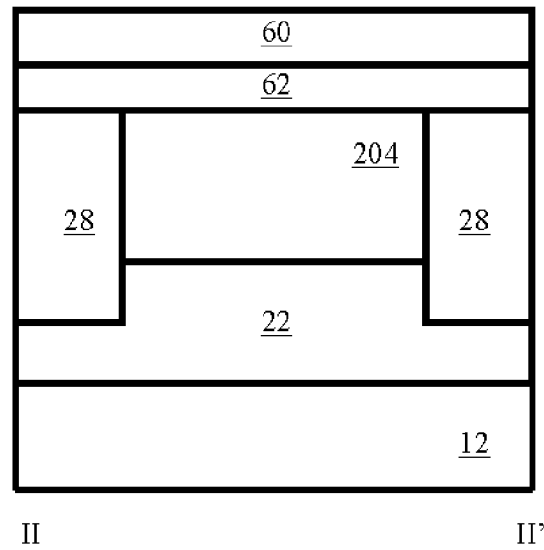


FIG. 76X

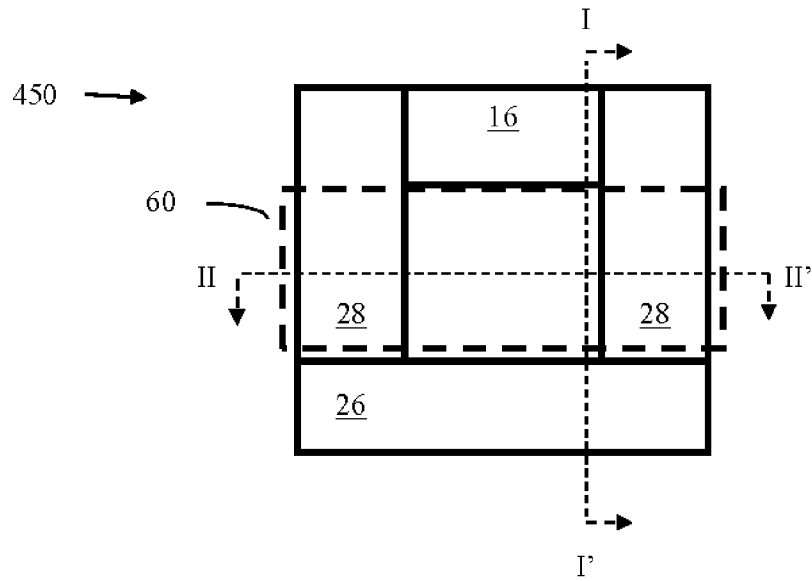
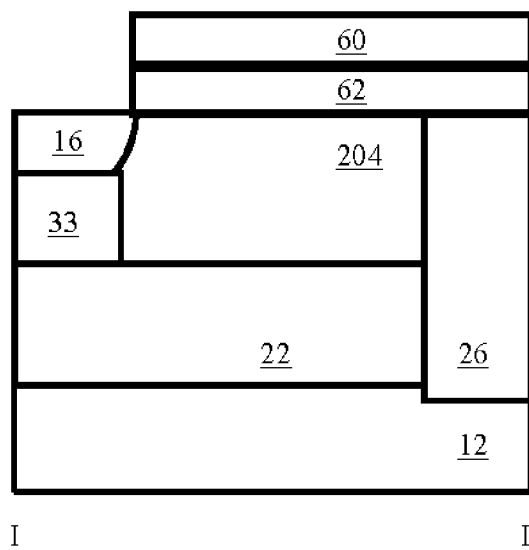


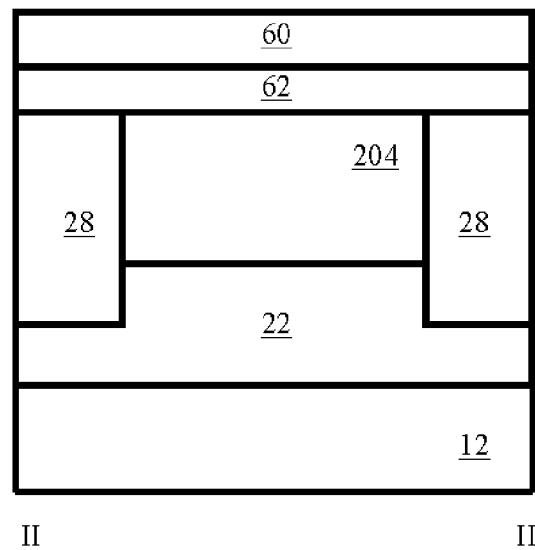
FIG. 76Y



I

I'

FIG. 76Z



II

II'

FIG. 76AA

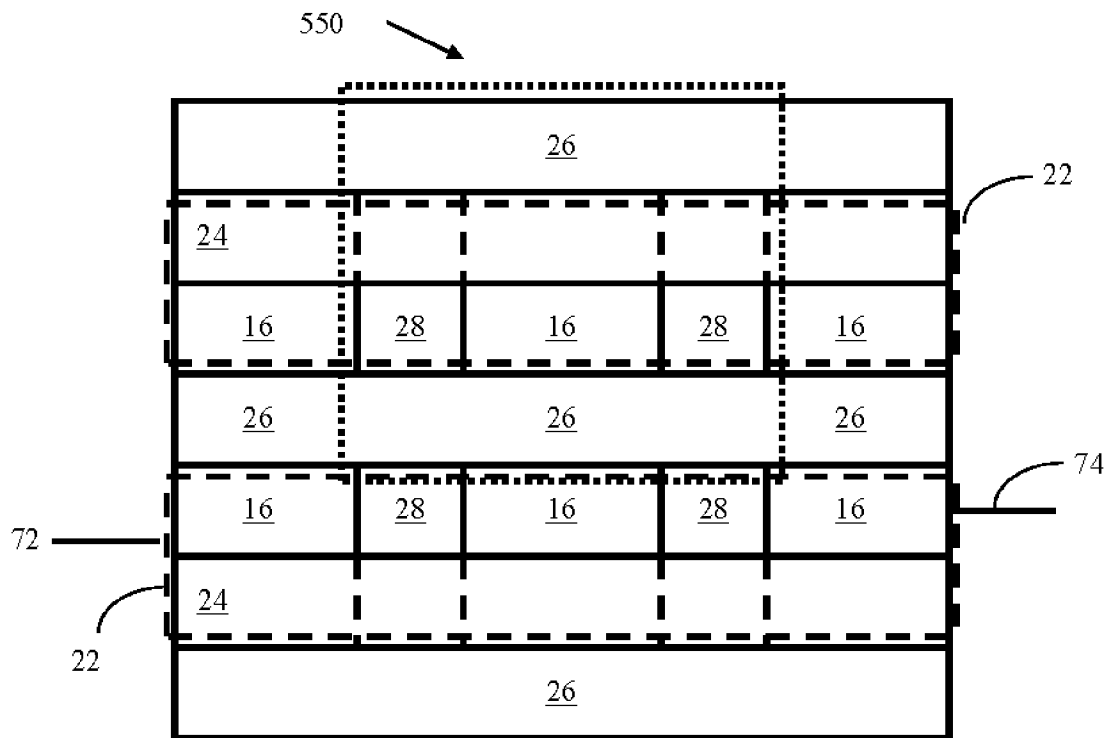


FIG. 77A

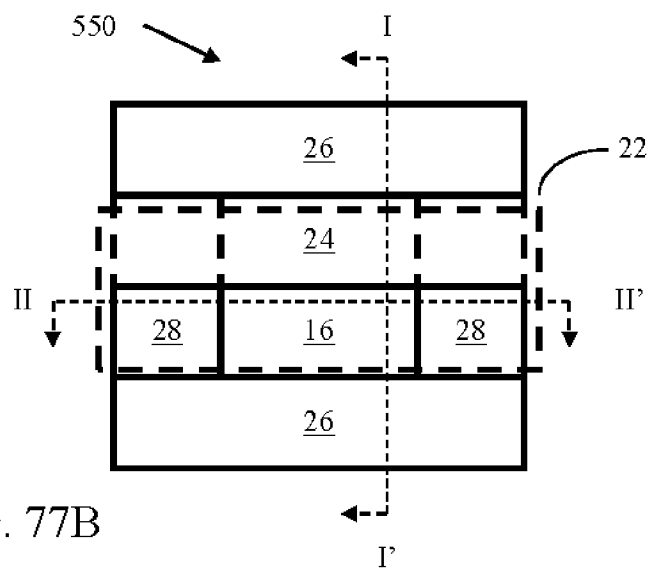


FIG. 77B

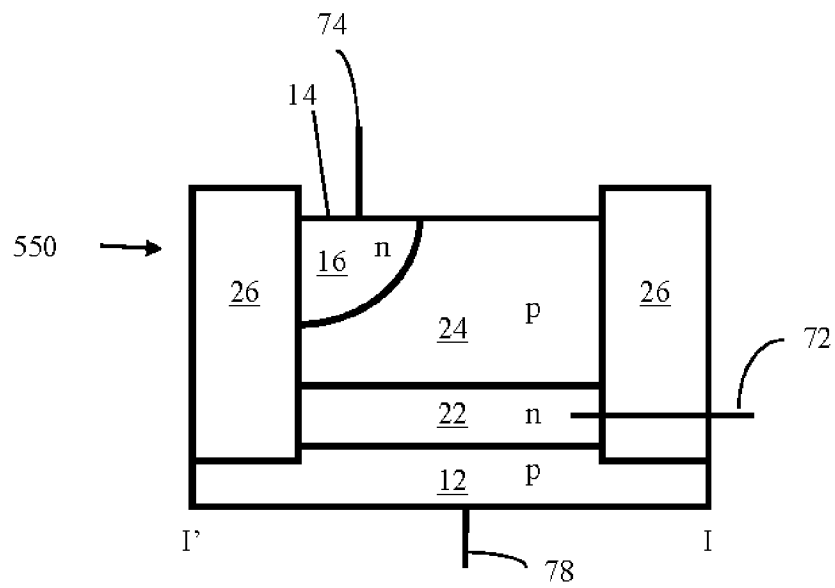


FIG. 77C

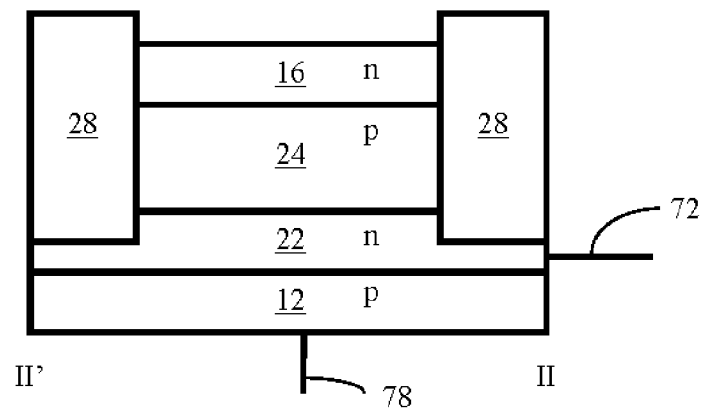


FIG. 77D

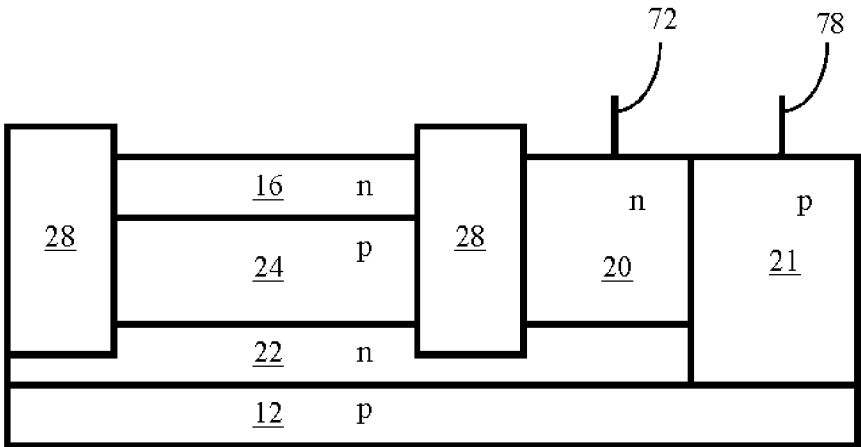


FIG. 77E

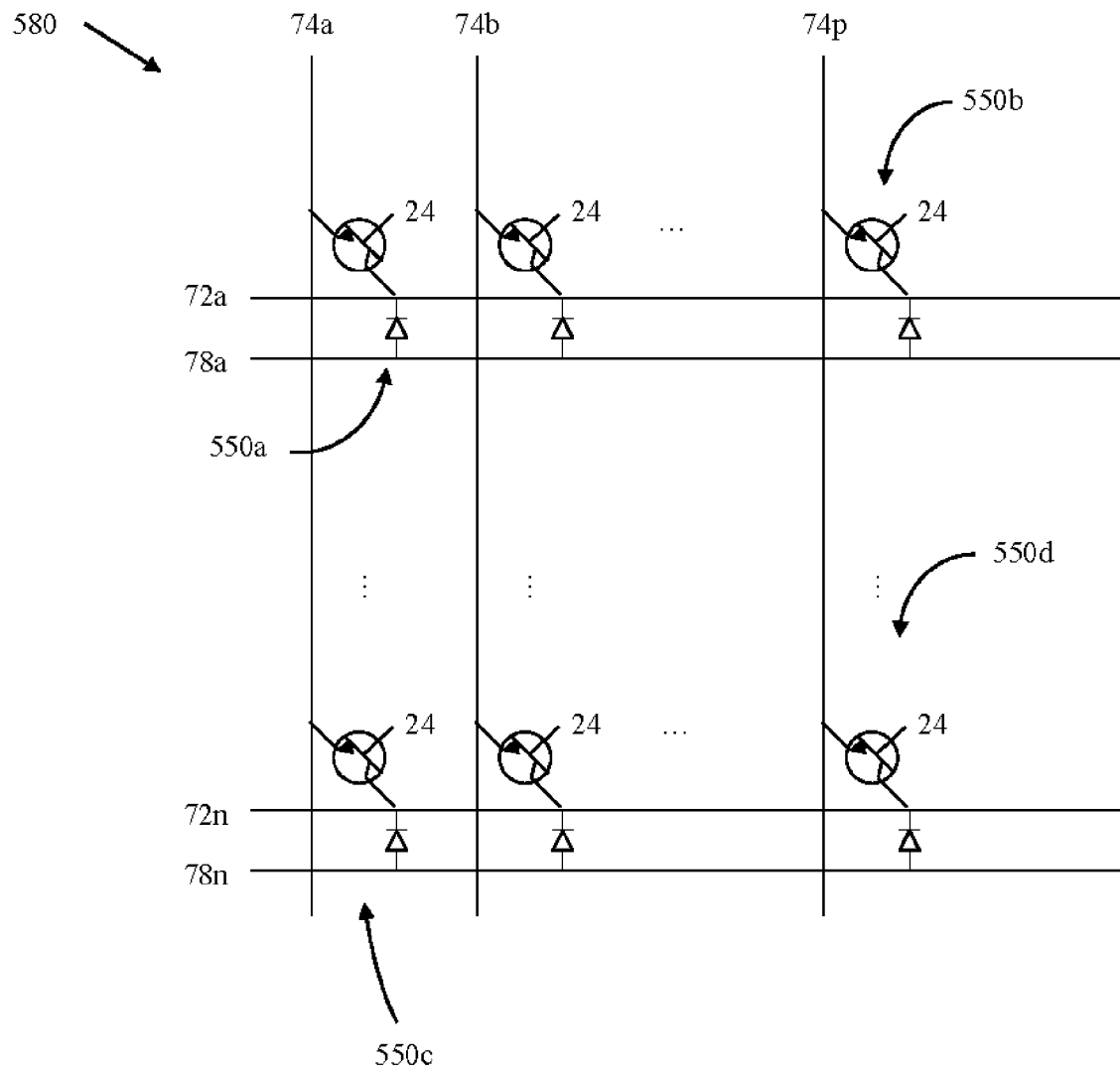


FIG. 77F

Array Hold Operation
(Memory Cells 550a, 550b, 550c and 550d)

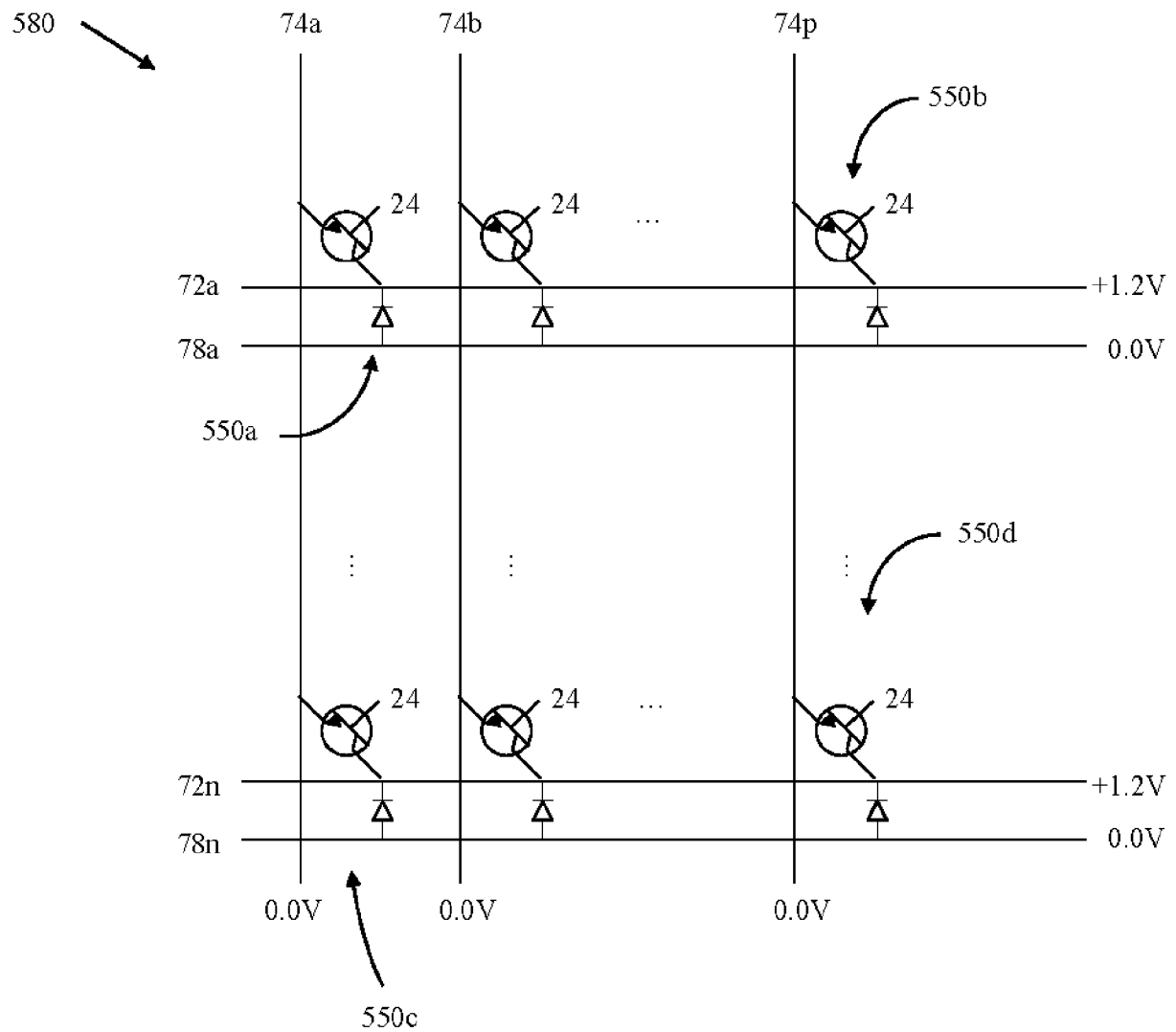


FIG. 78A

Row Hold Operation (Memory Cells 550a and 550b)

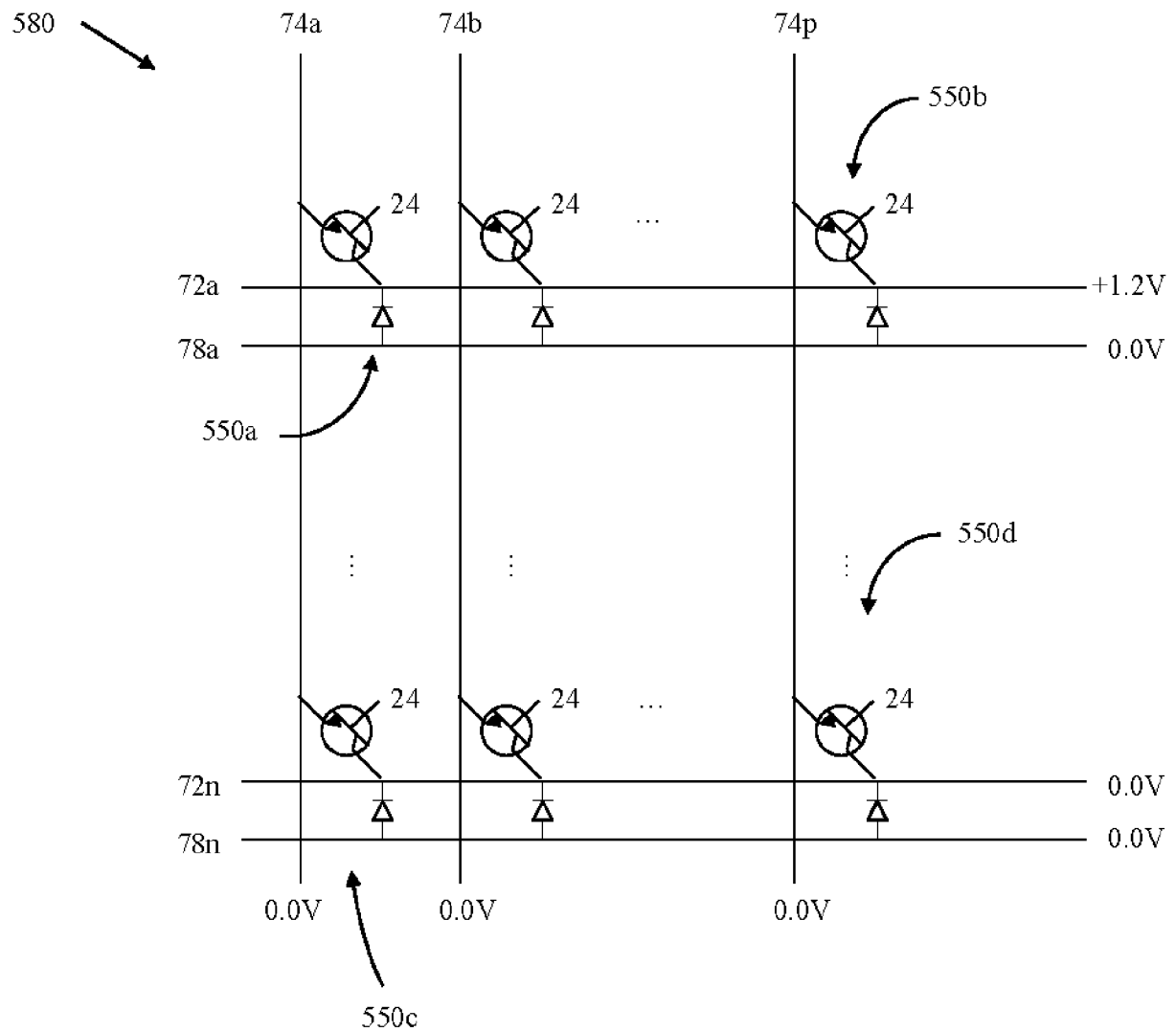


FIG. 78B

Read Operation (Single Memory Cell 550a)

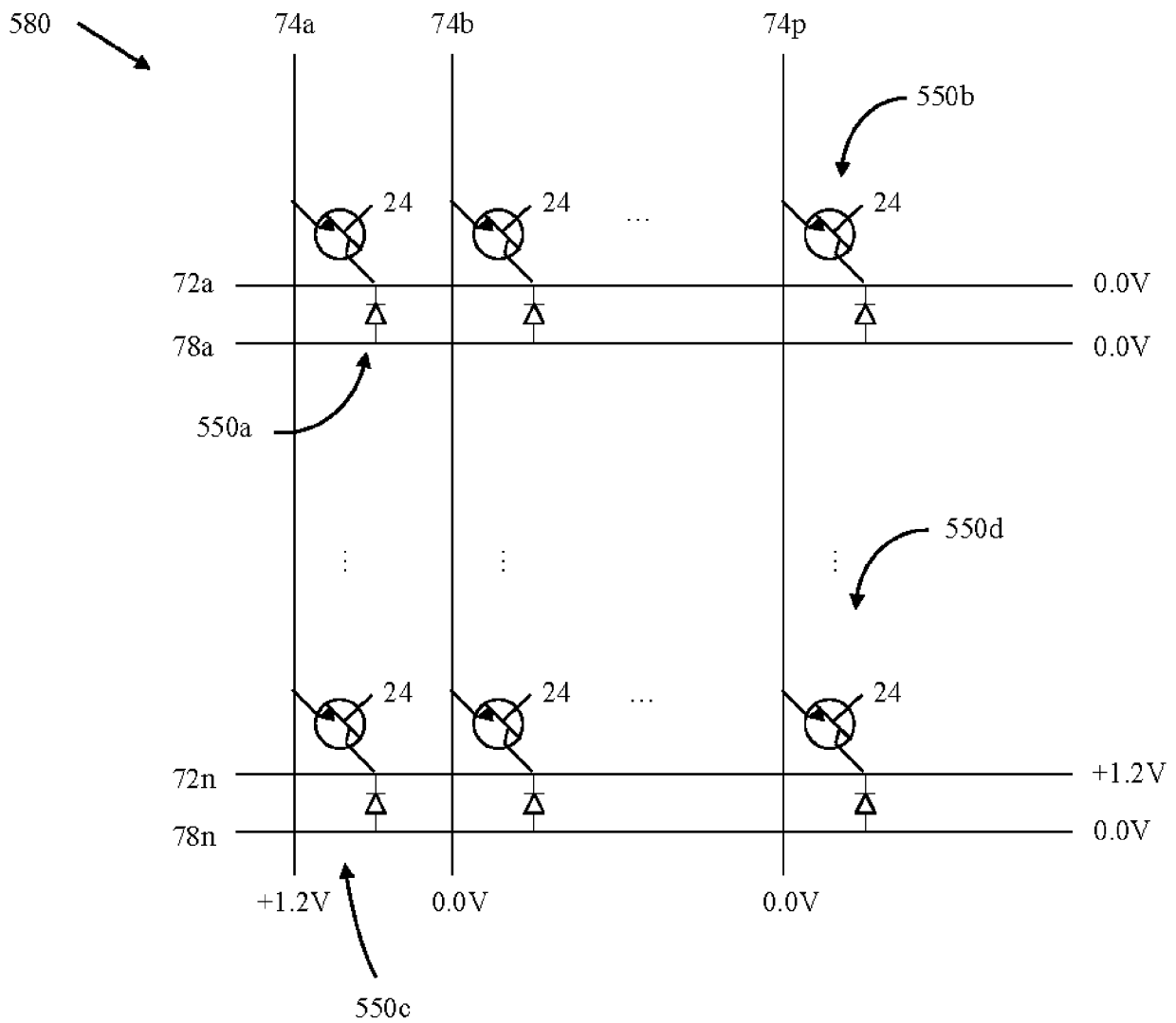


FIG. 79

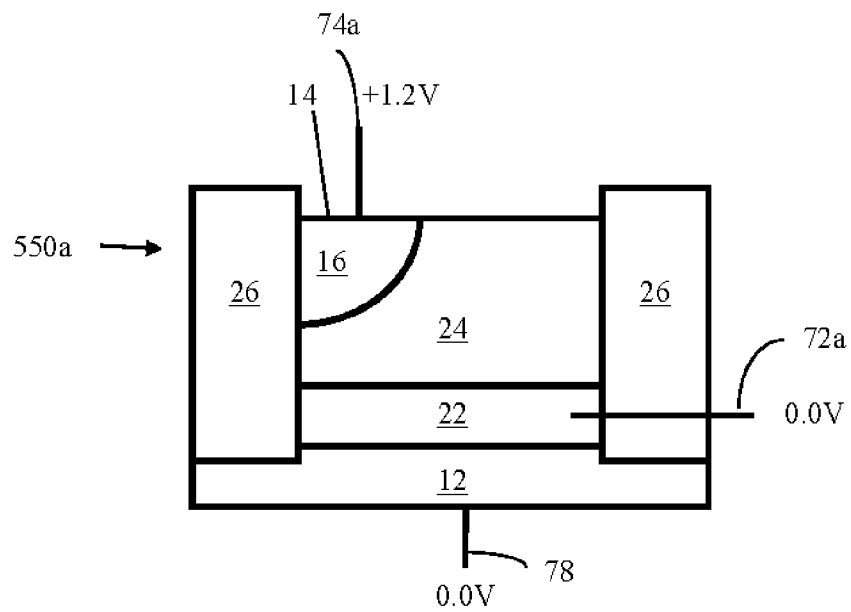


FIG. 80A

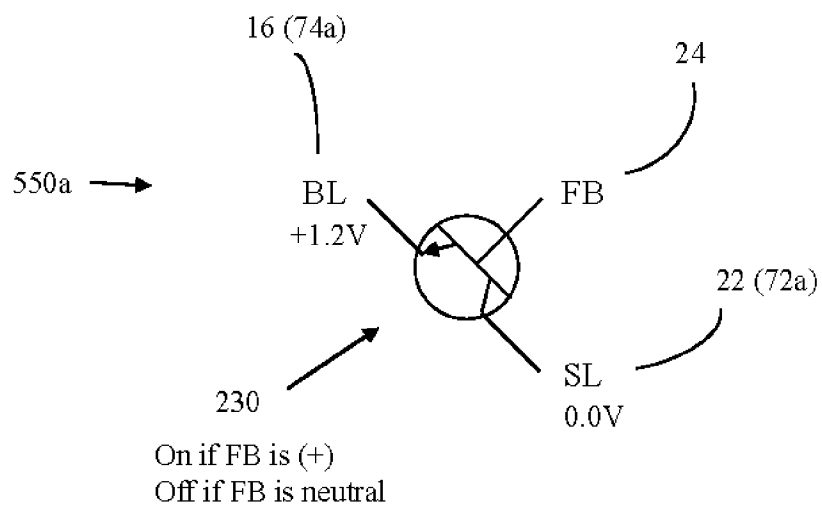


FIG. 80B

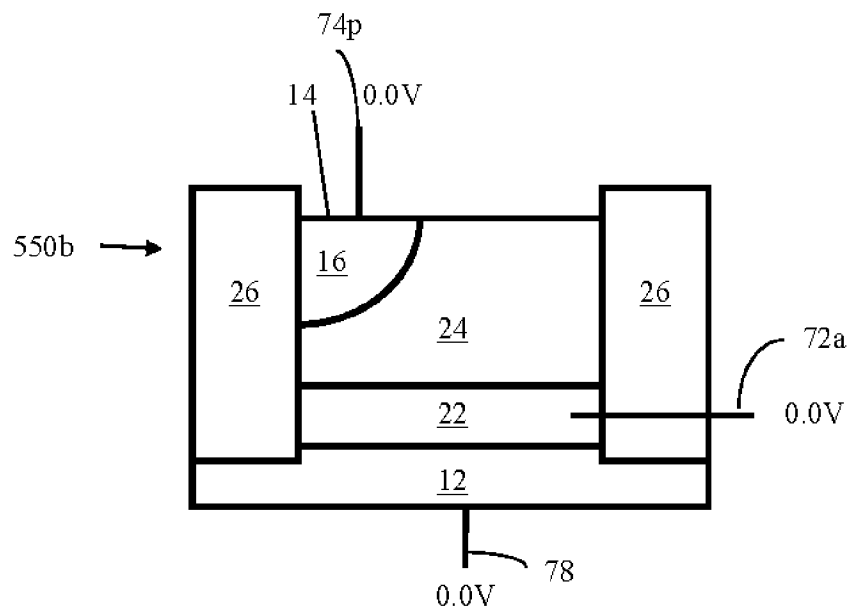


FIG. 80C

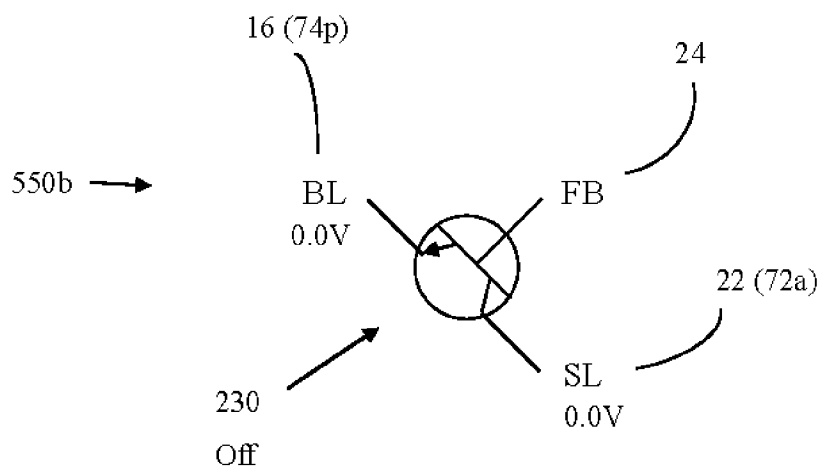


FIG. 80D

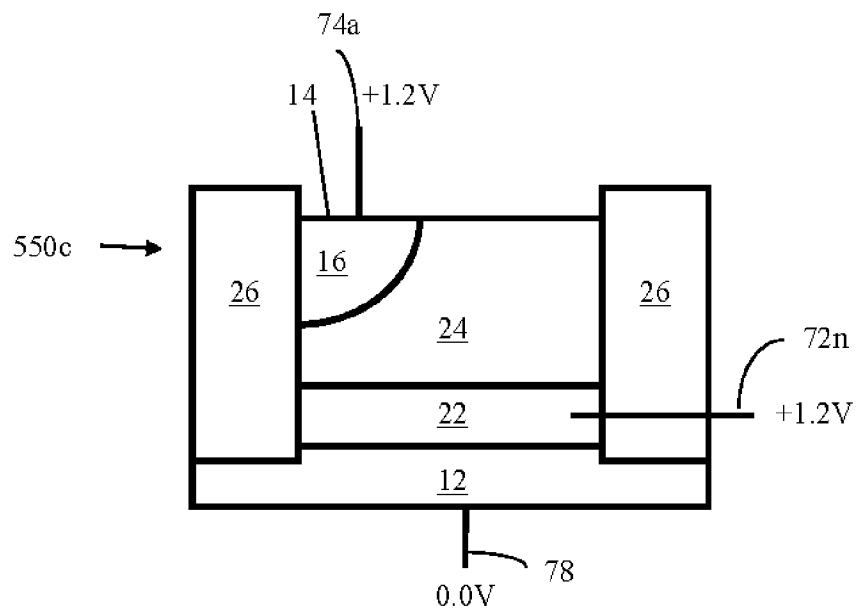


FIG. 80E

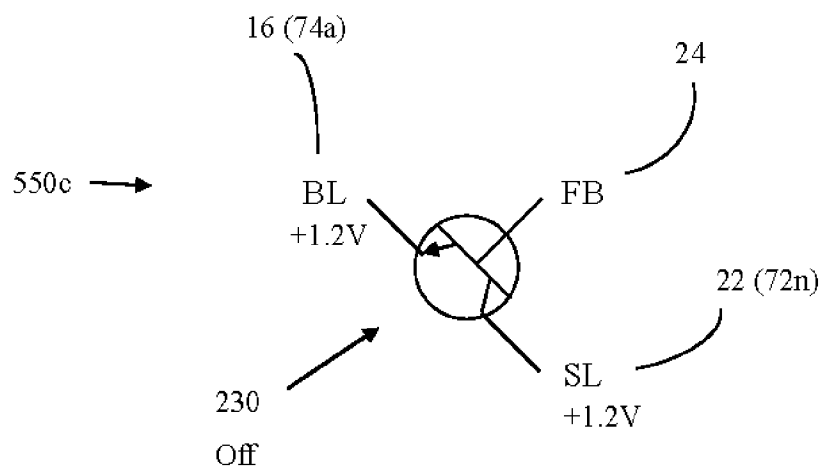


FIG. 80F

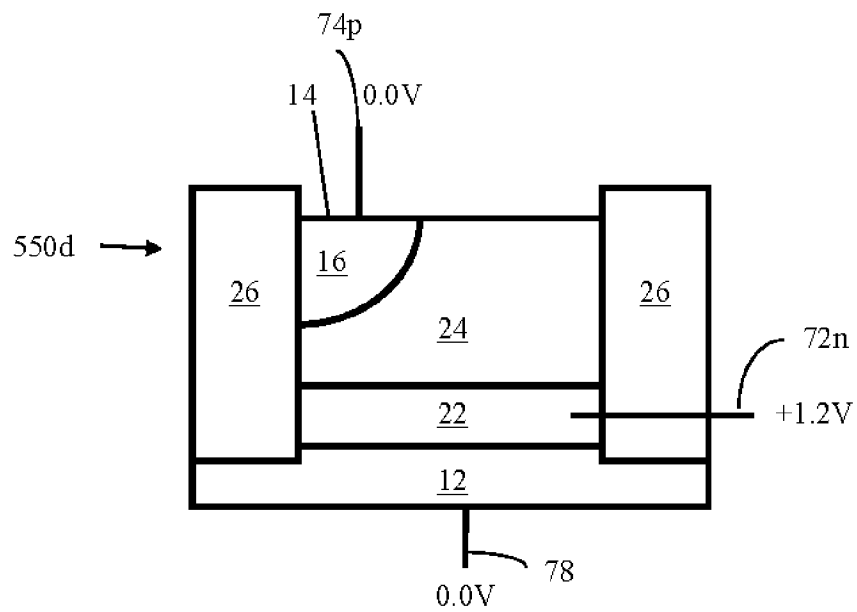


FIG. 80G

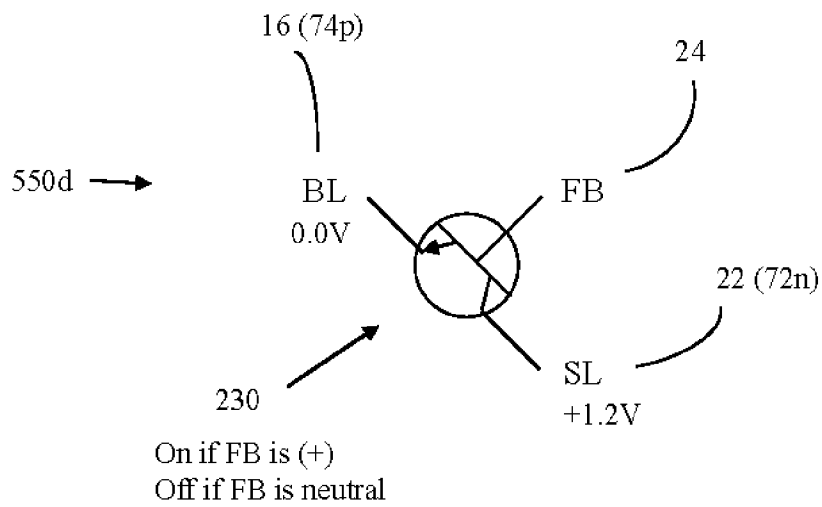


FIG. 80H

Singe Row Write Logic-0 Operation (Memory Cells 550a and 550b)

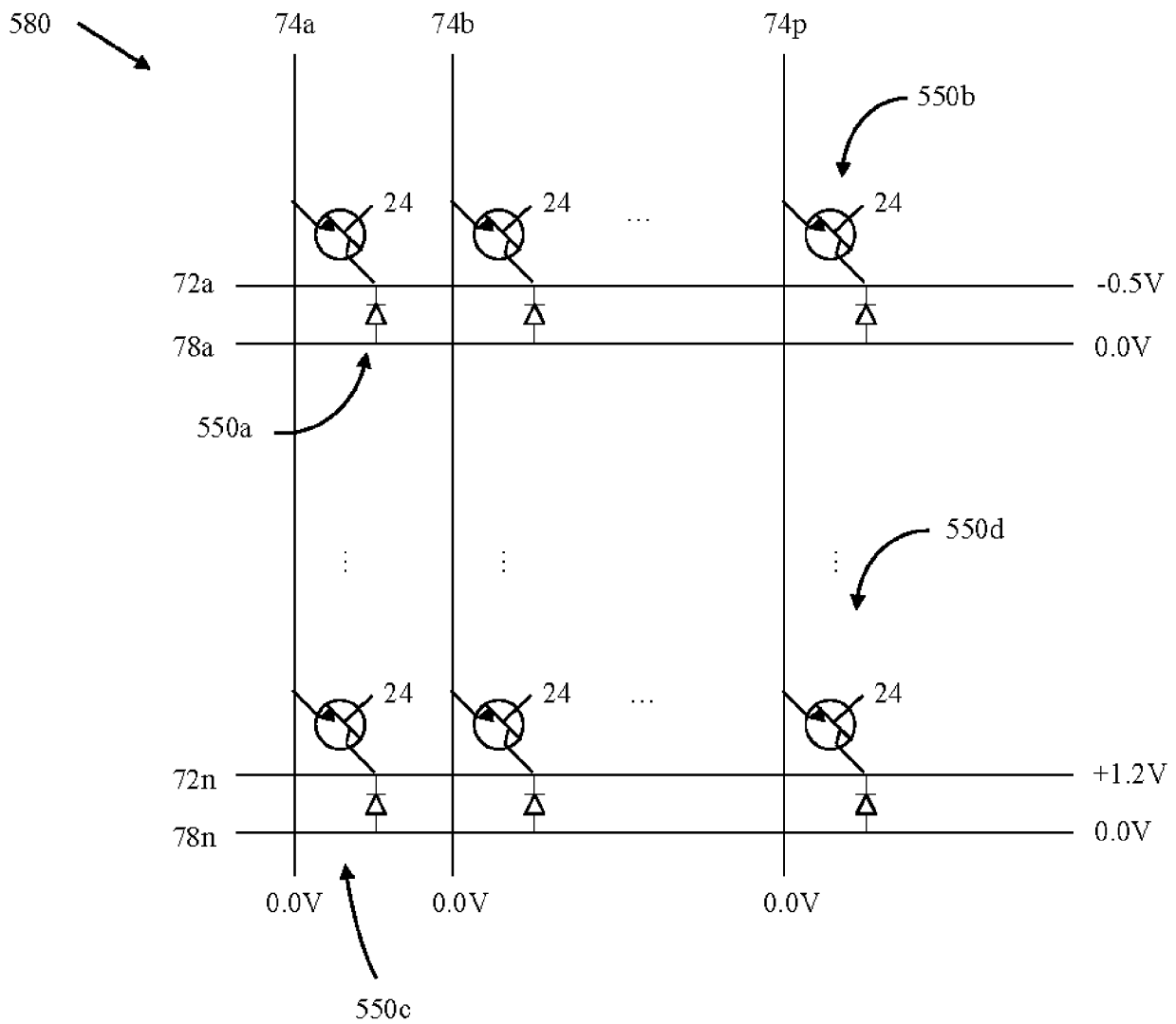


FIG. 81

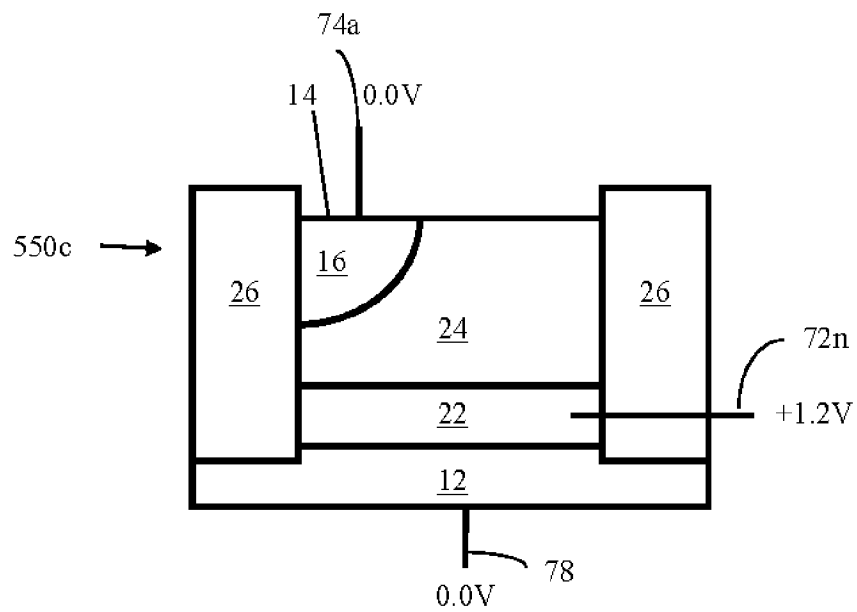


FIG. 82A

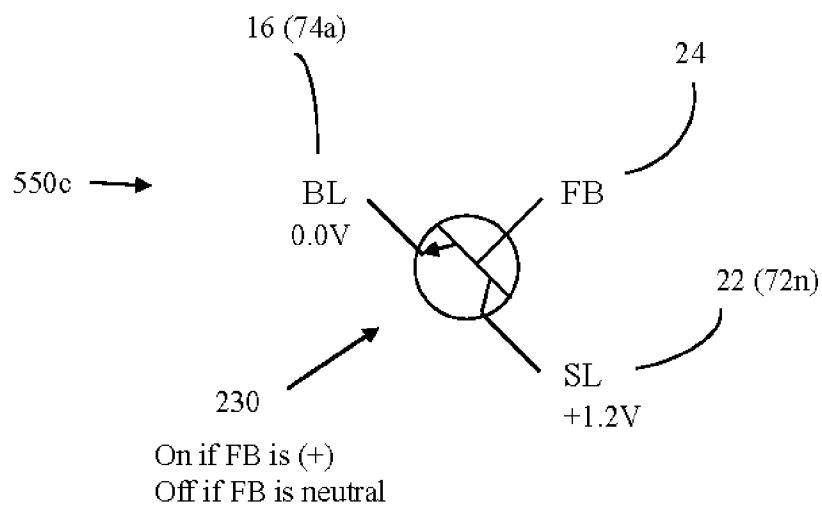


FIG. 82B

Write Logic-1 Operation – Impact Ionization (Single Memory Cell 550a)

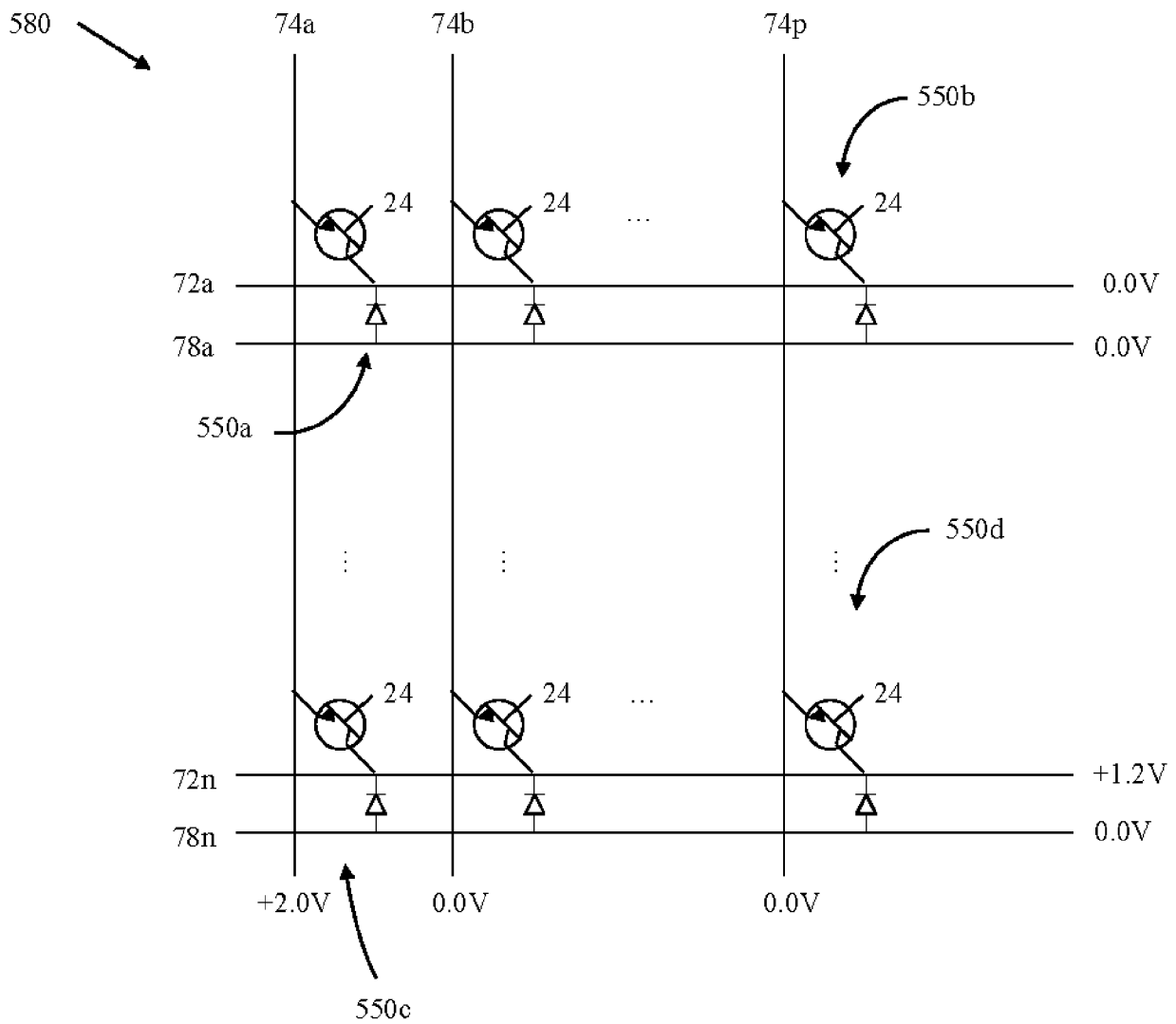


FIG. 83

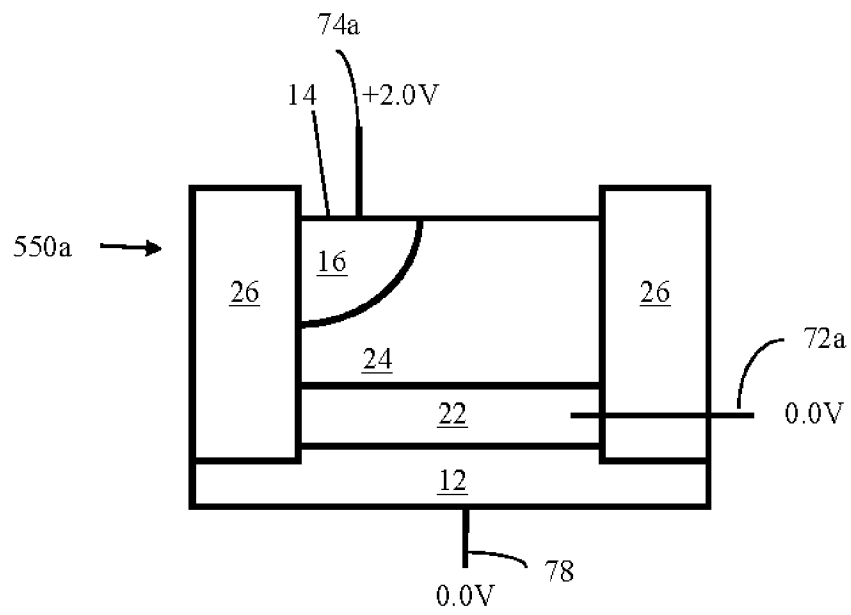


FIG. 84A

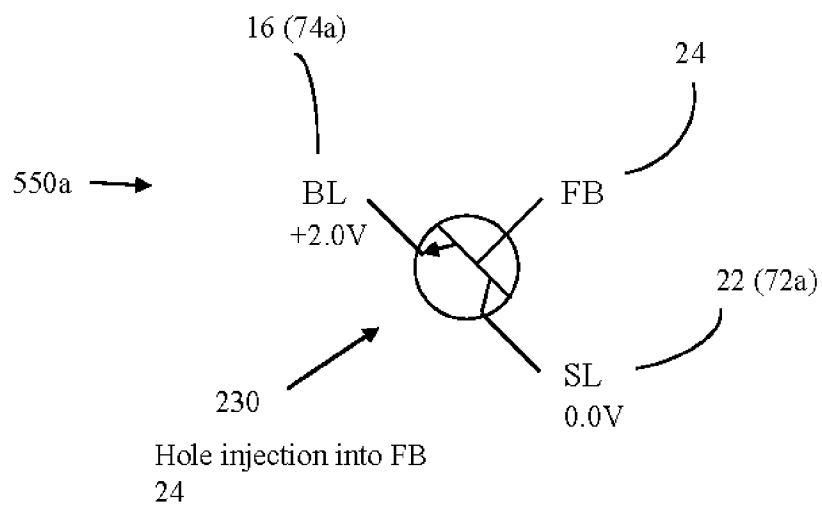


FIG. 84B

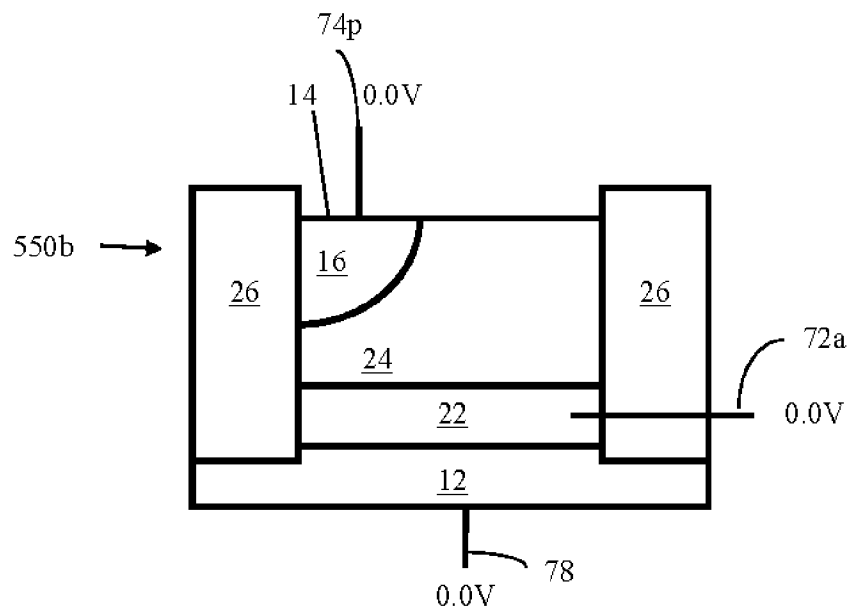


FIG. 84C

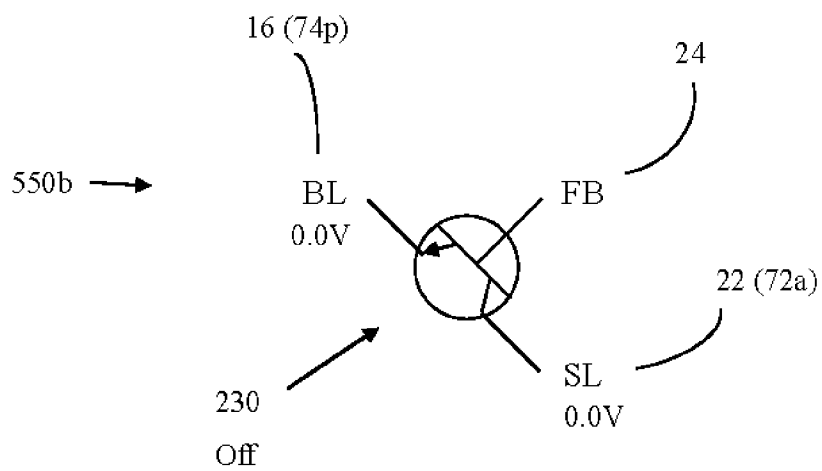


FIG. 84D

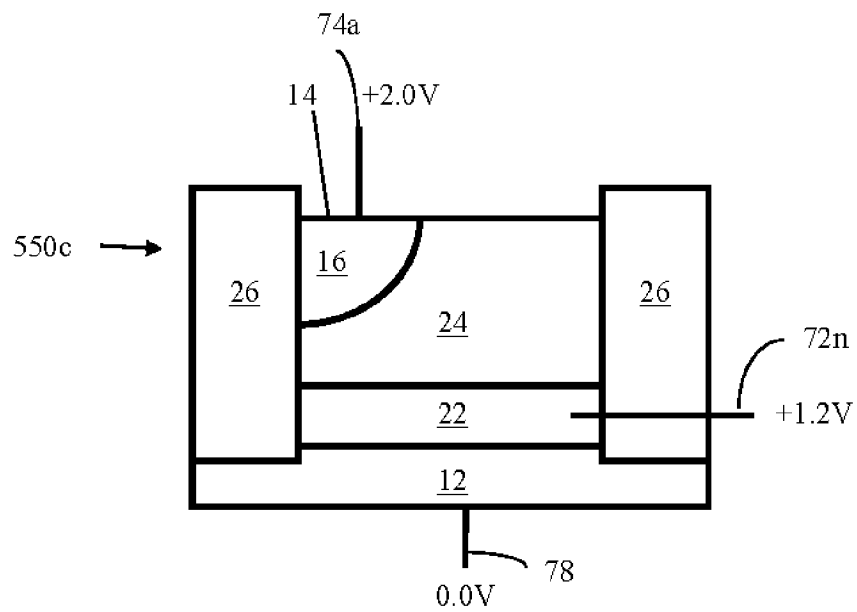


FIG. 84E

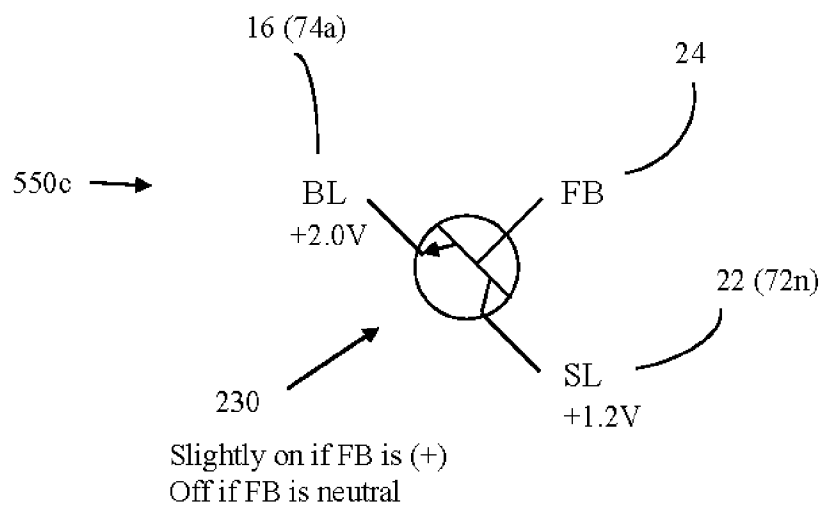


FIG. 84F

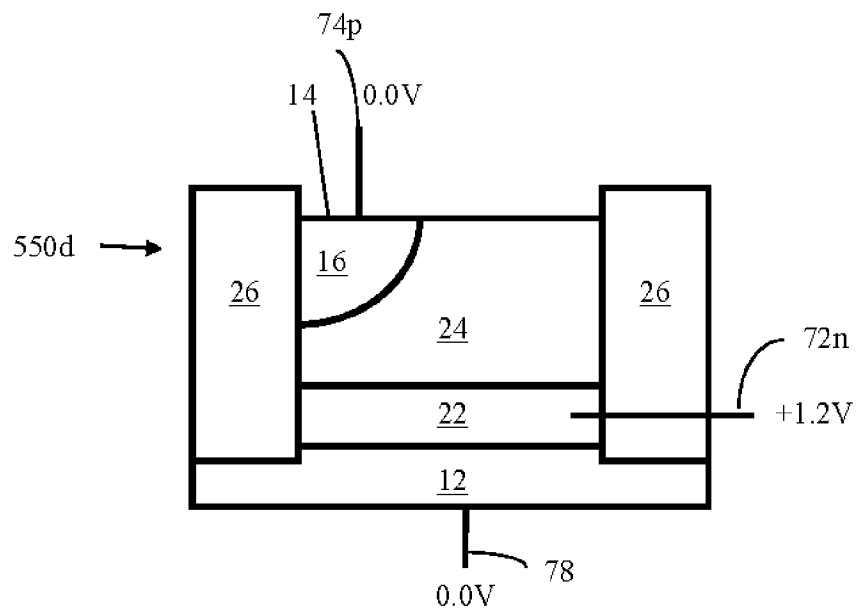


FIG. 84G

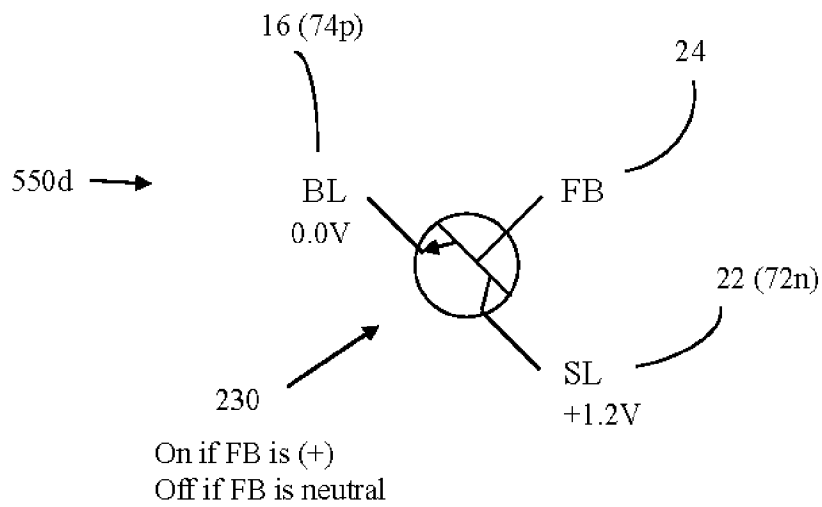


FIG. 84H

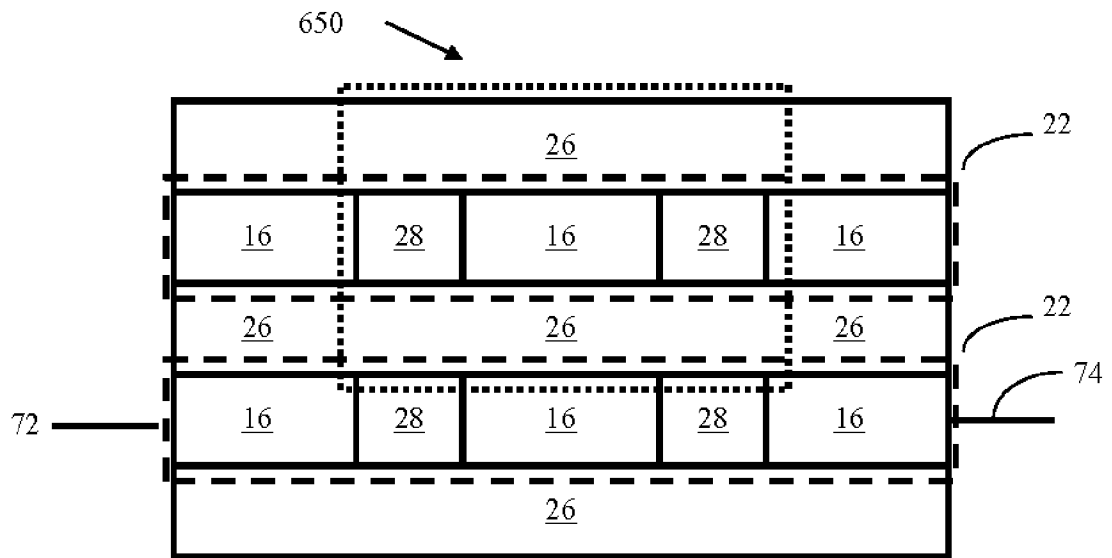


FIG. 85A

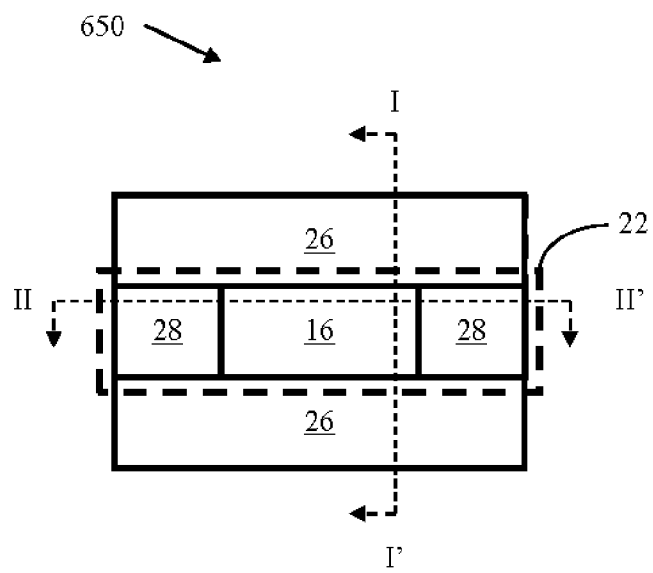


FIG. 85B

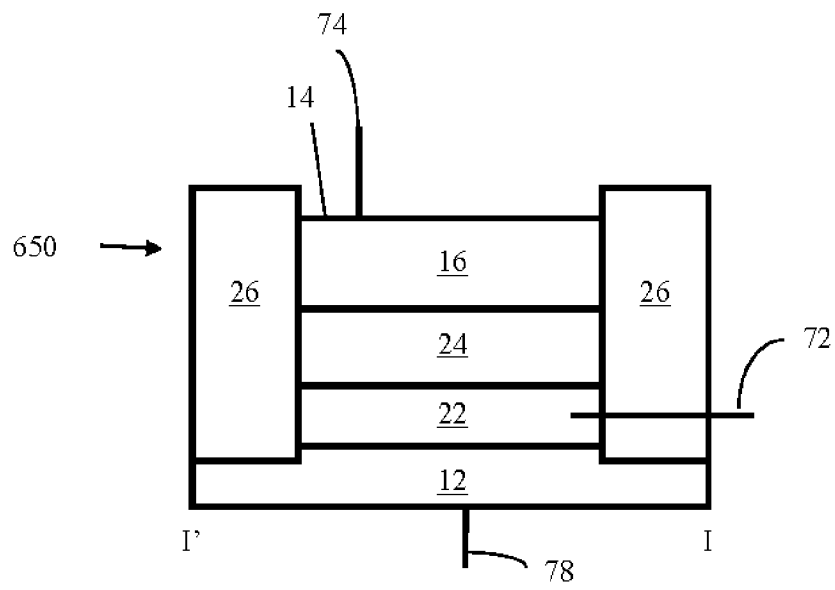


FIG. 85C

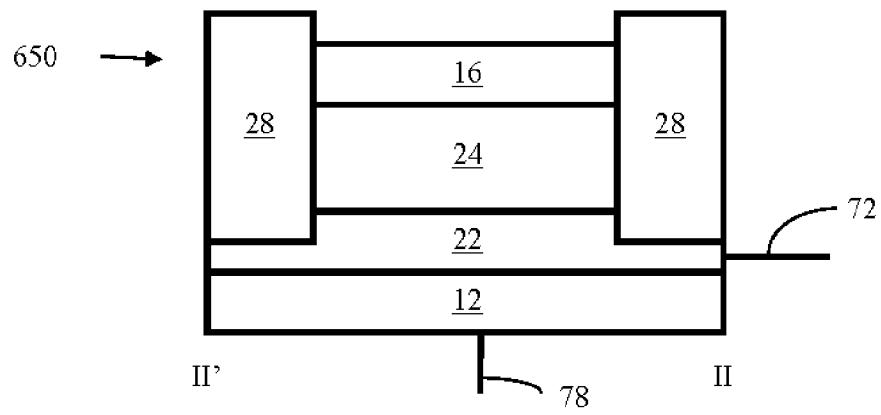


FIG. 85D

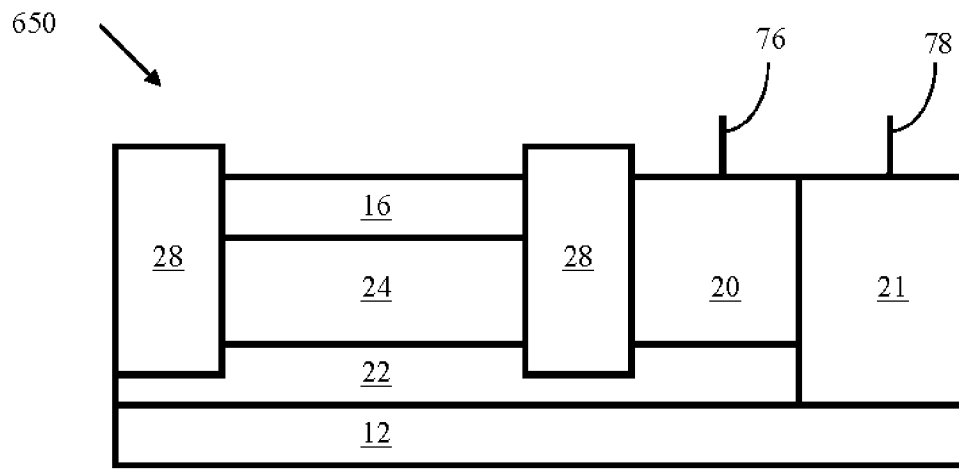


FIG. 85E

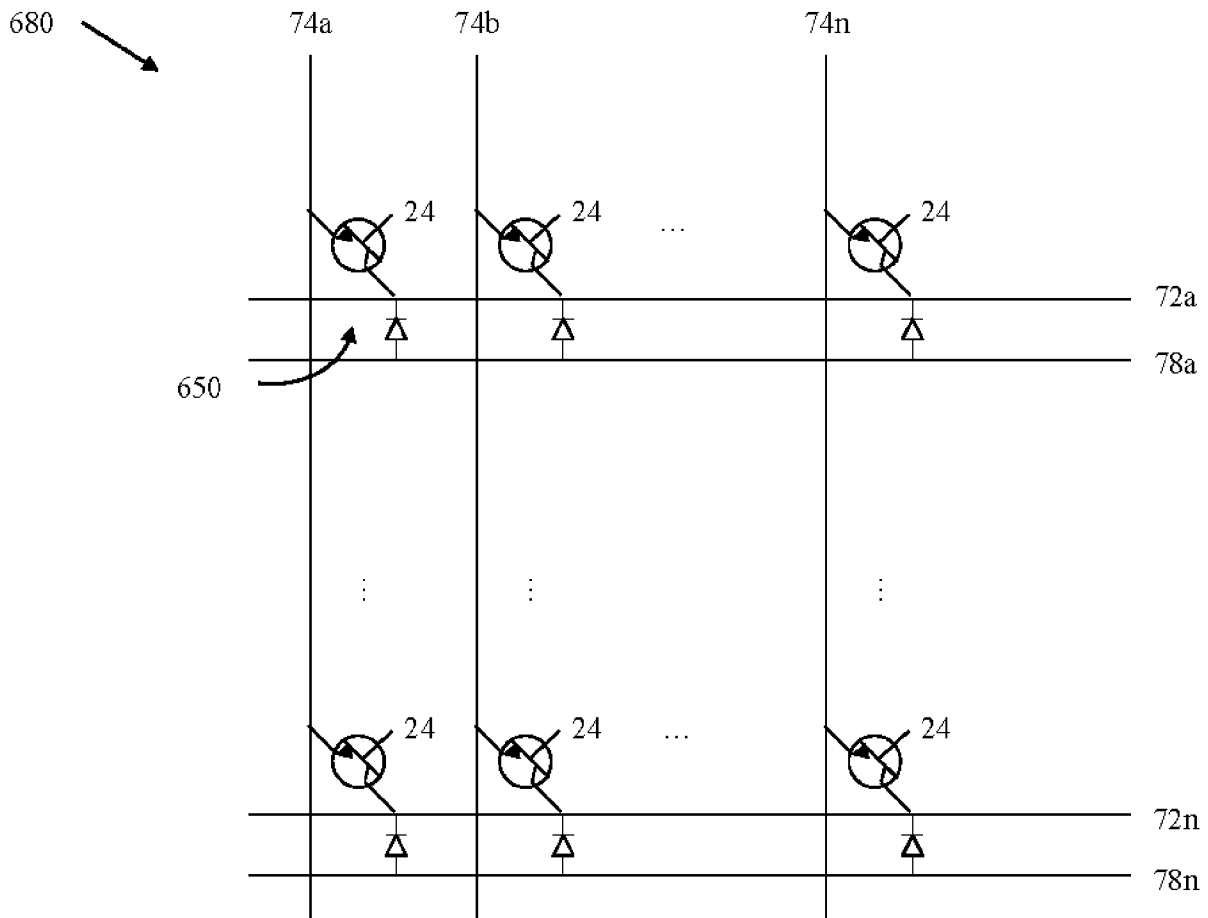


FIG. 85F

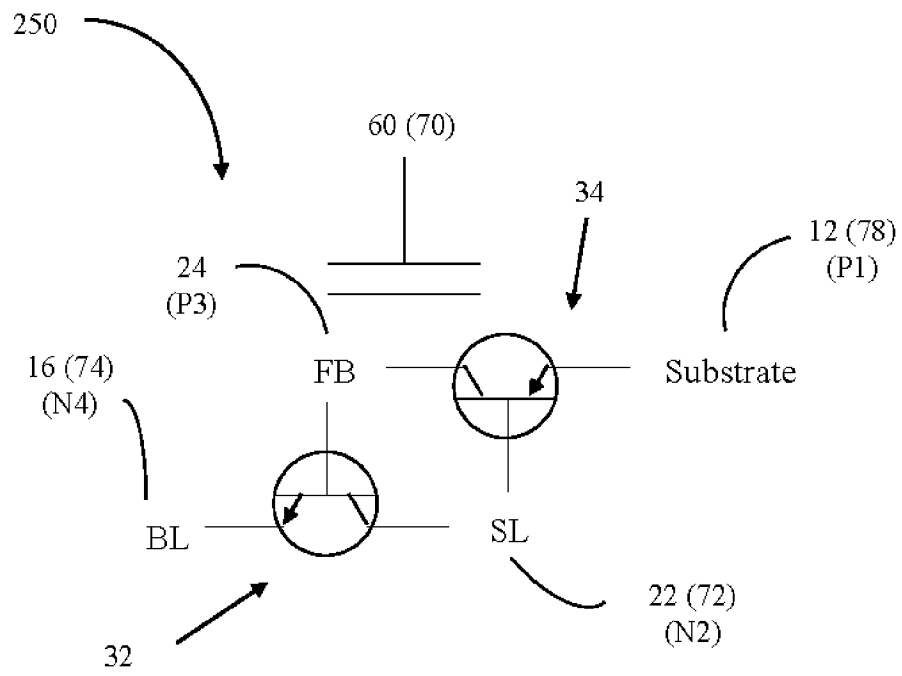


FIG. 86

Read Operation (Single Memory Cell 250a)

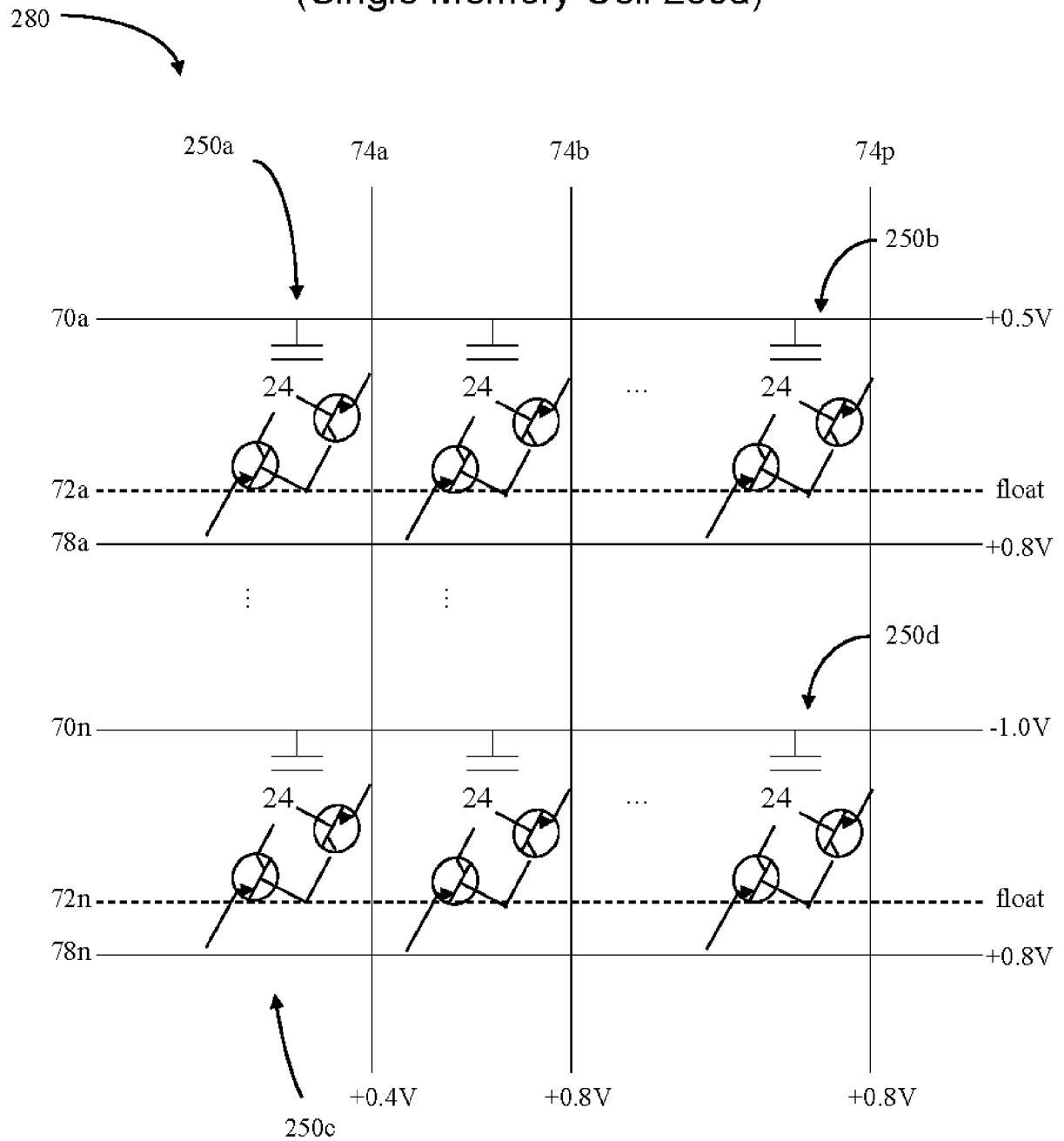


FIG. 87

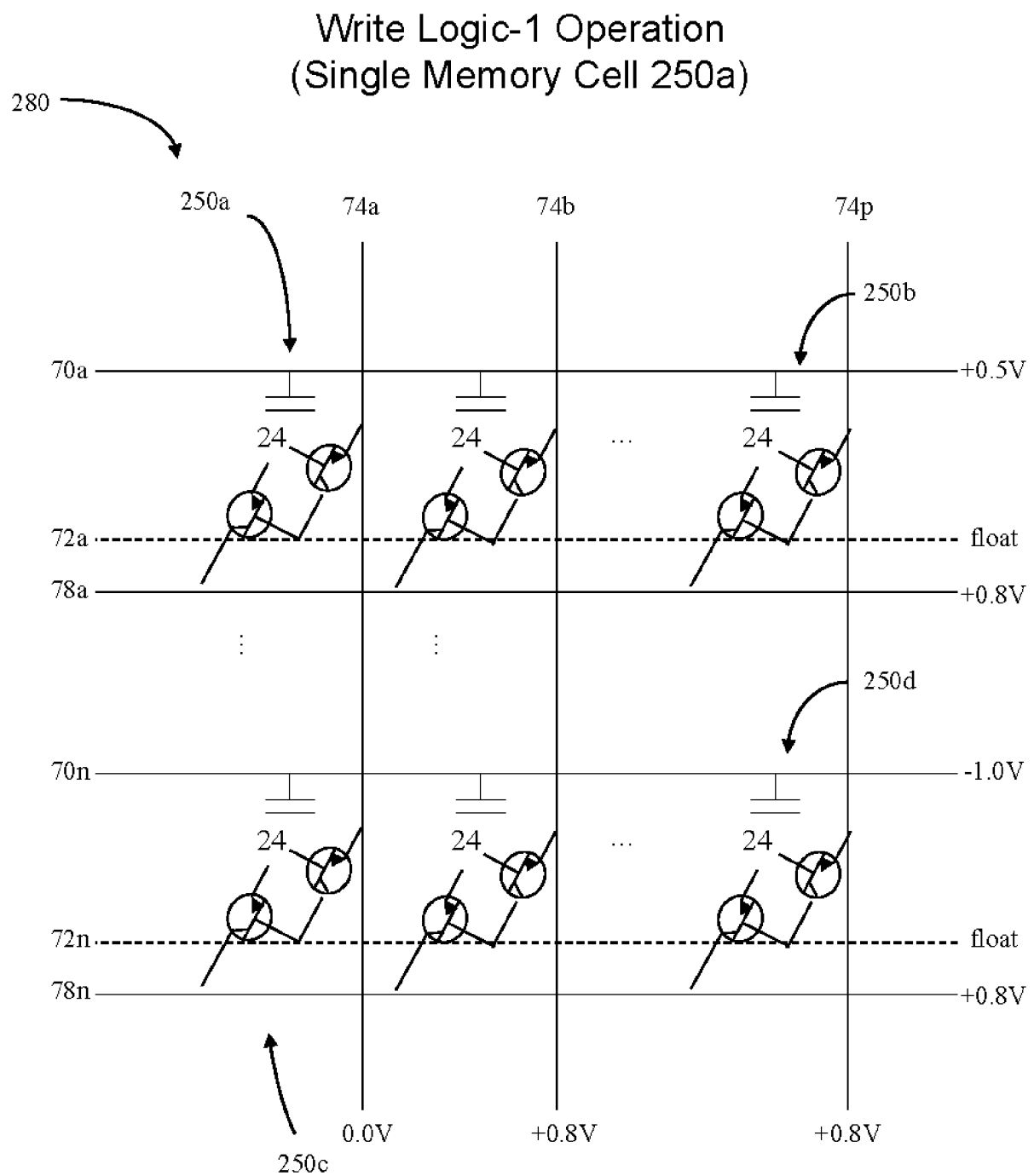


FIG. 88

Write Logic-0 Operation
(Single Memory Cell 250a)

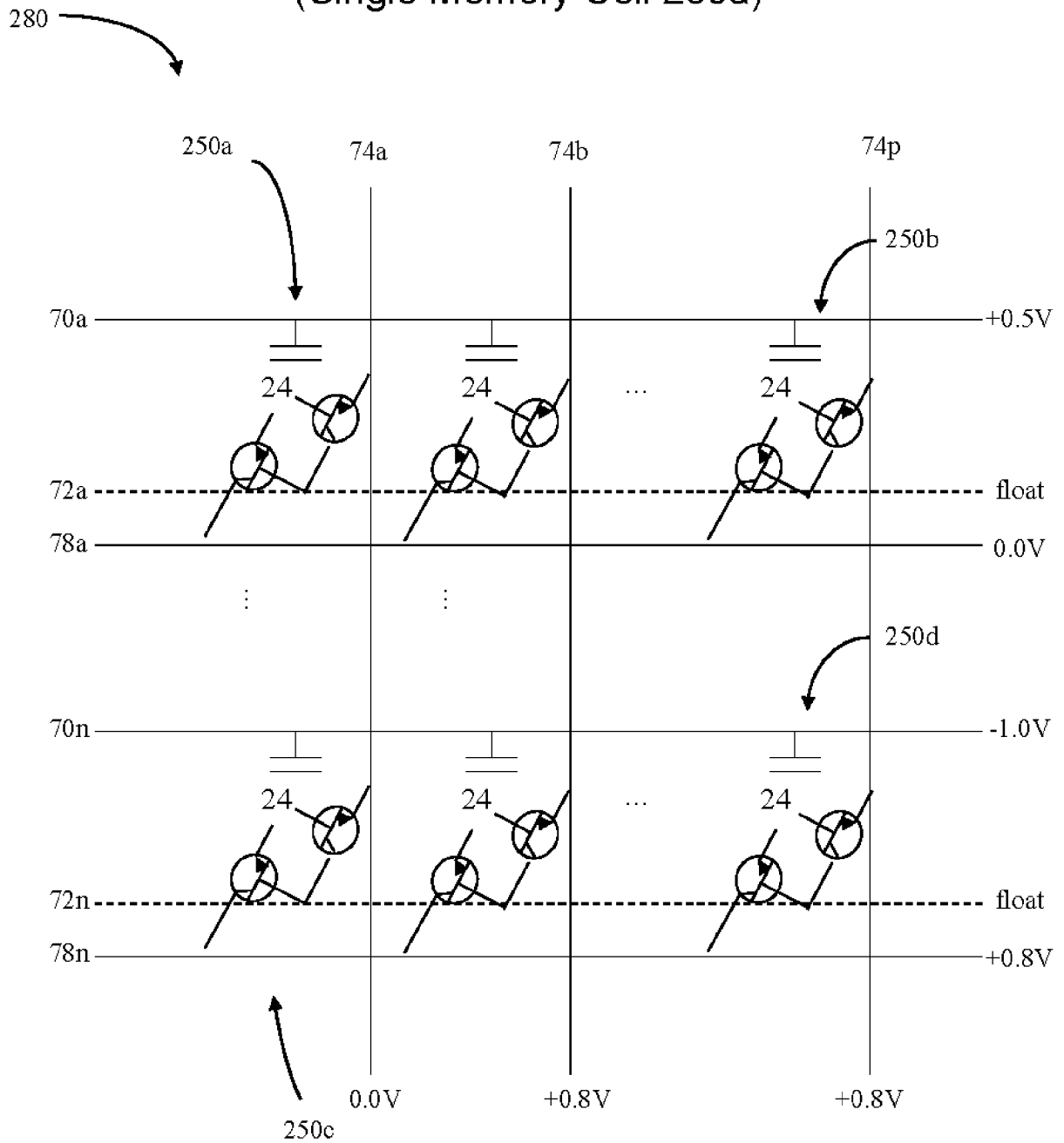


FIG. 89

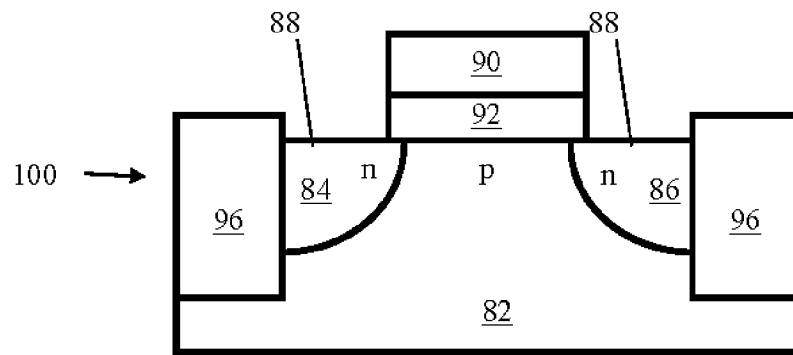


FIG. 90A (Prior Art)

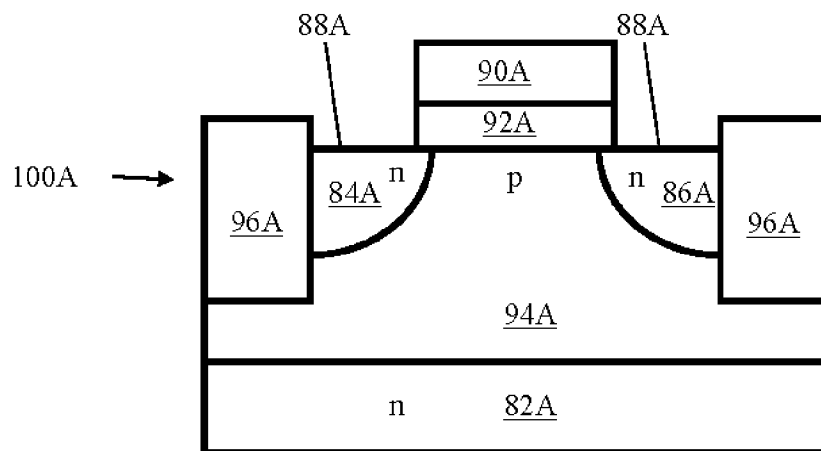


FIG. 90B (Prior Art)

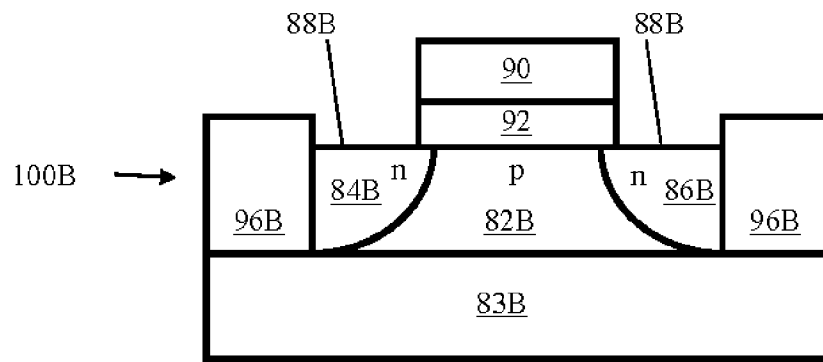


FIG. 90C (Prior Art)

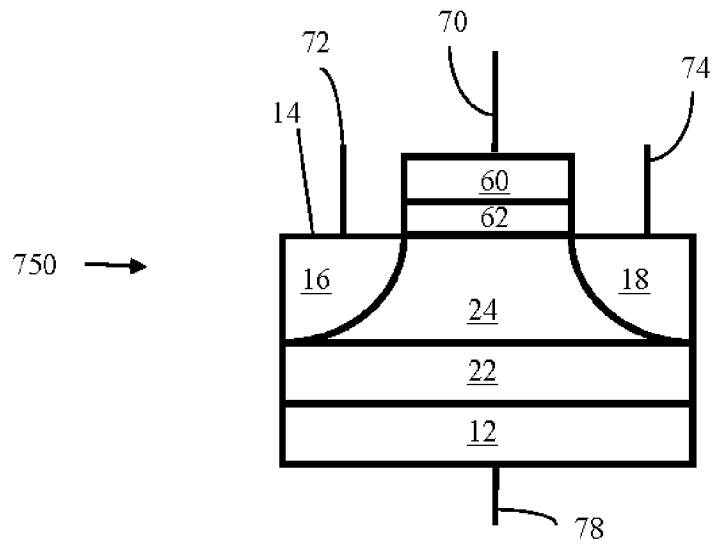


FIG. 91

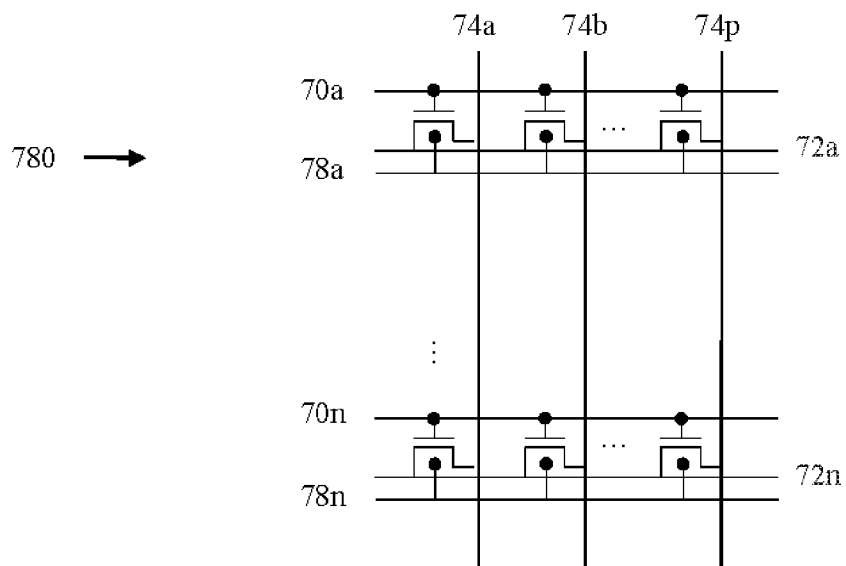


FIG. 92A

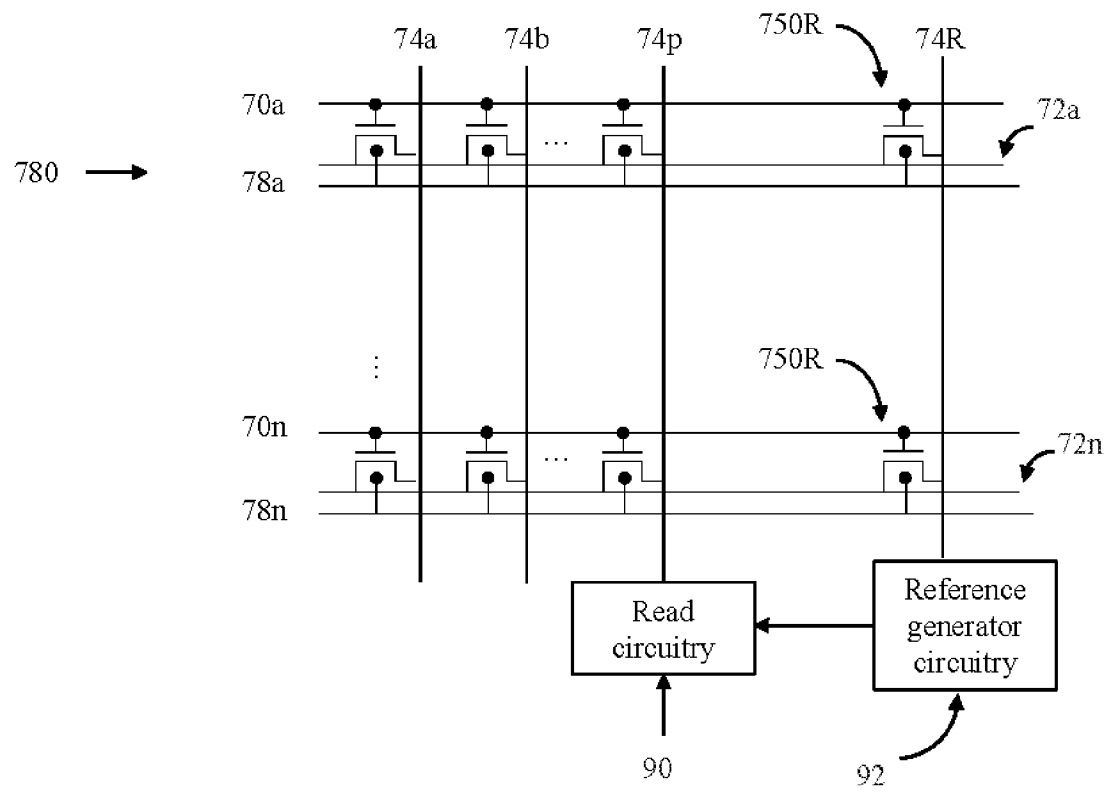


FIG. 92B

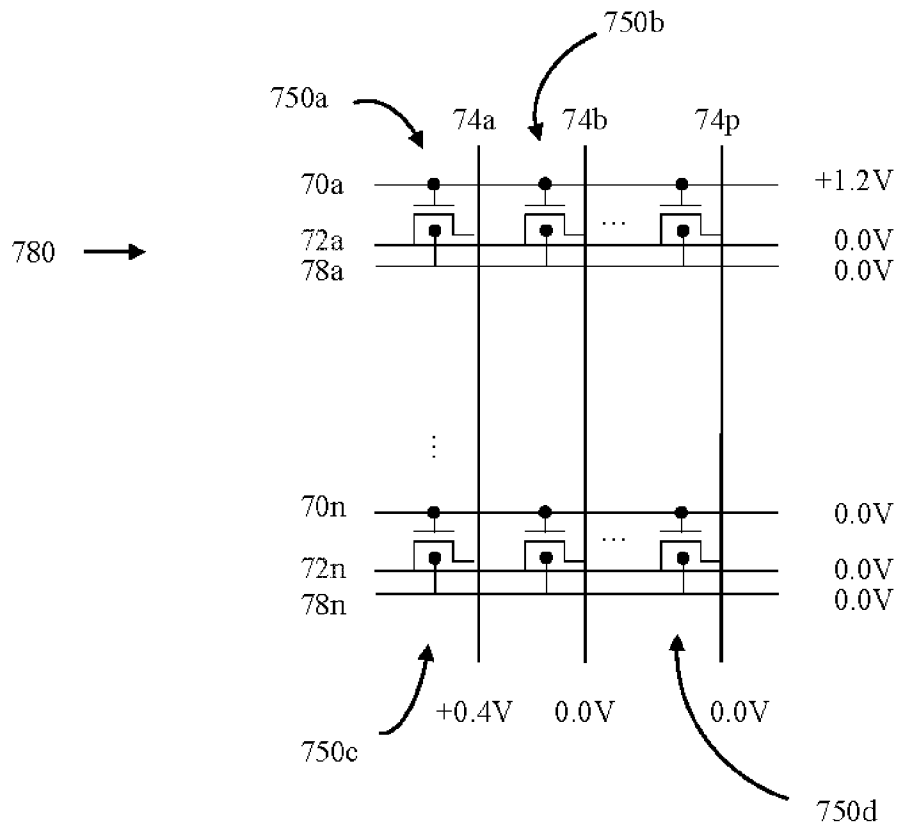


FIG. 93

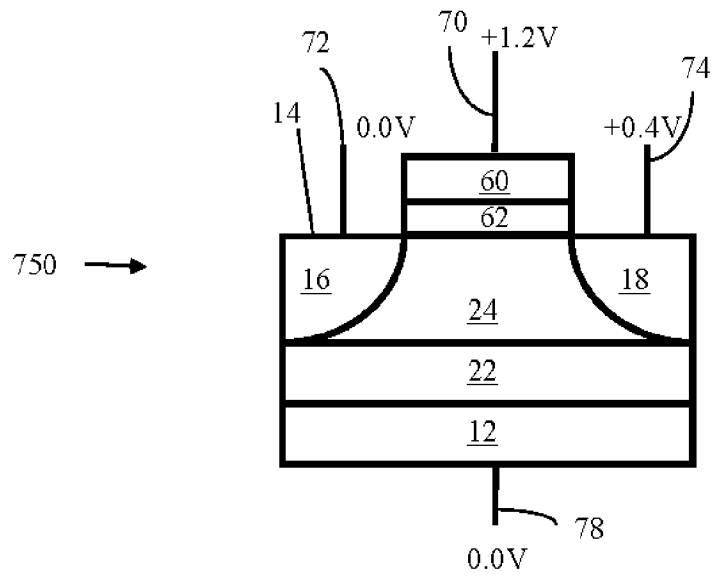


FIG. 94A

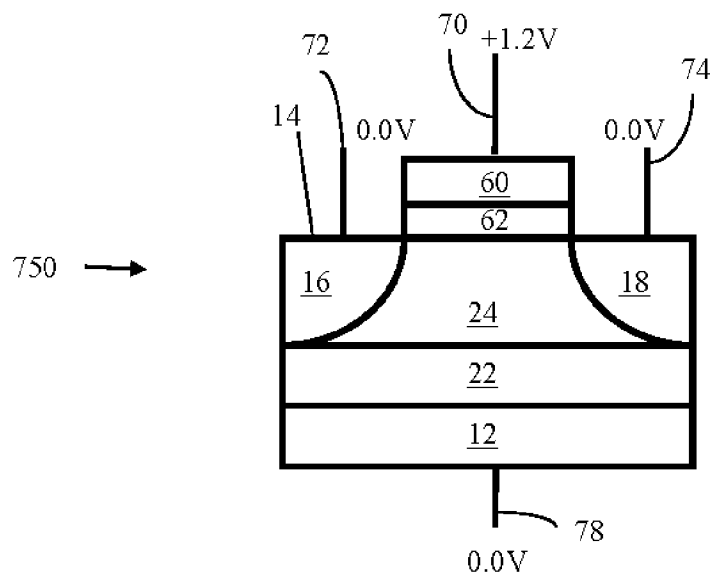


FIG. 94B

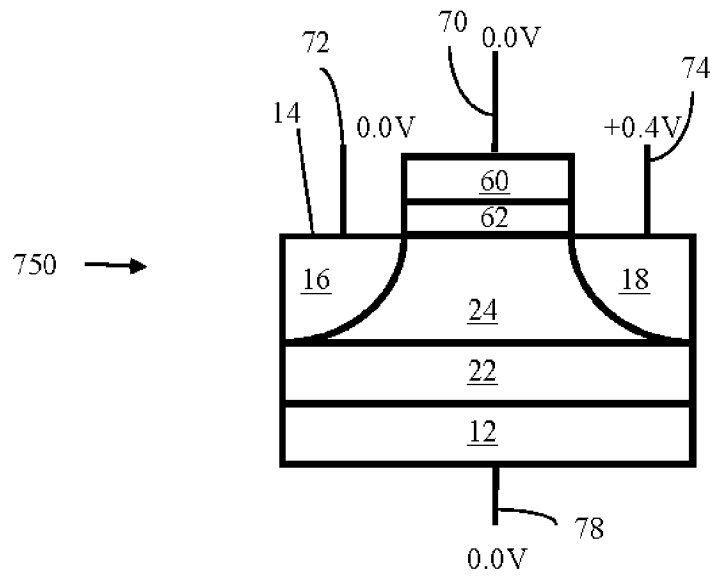


FIG. 94C

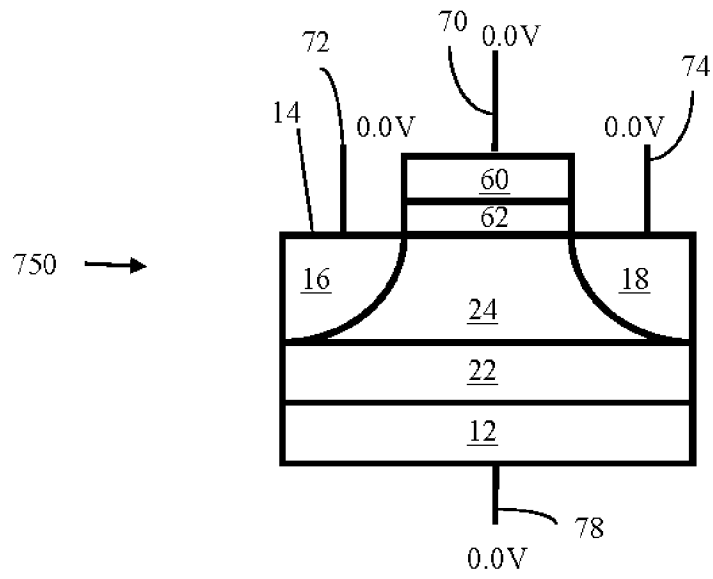


FIG. 94D

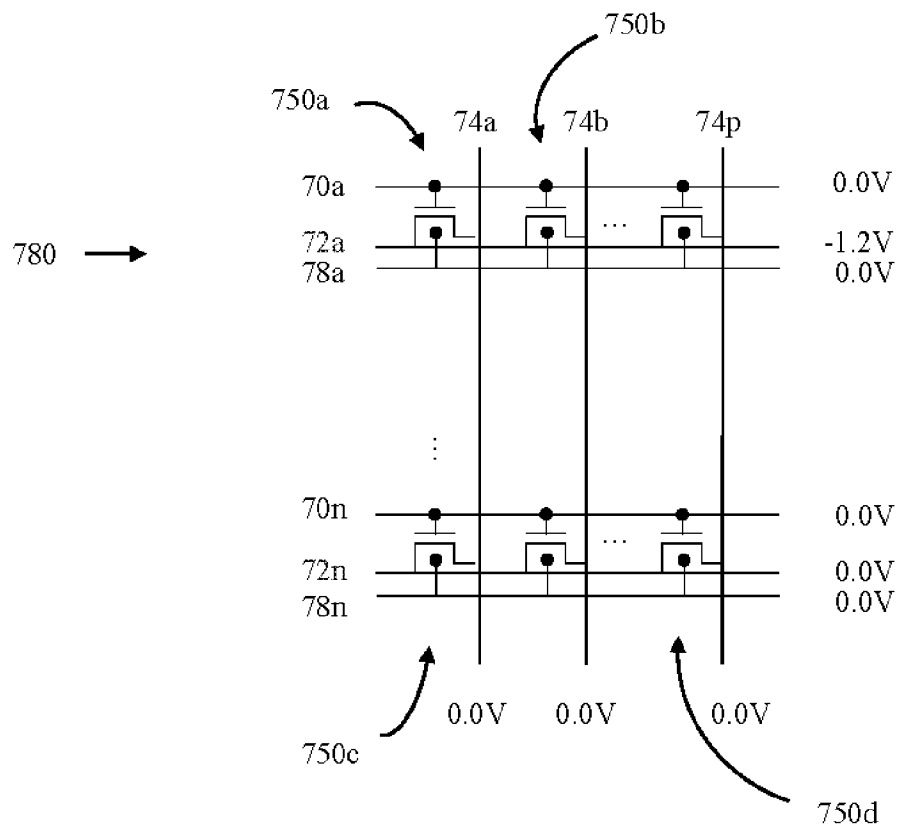


FIG. 95

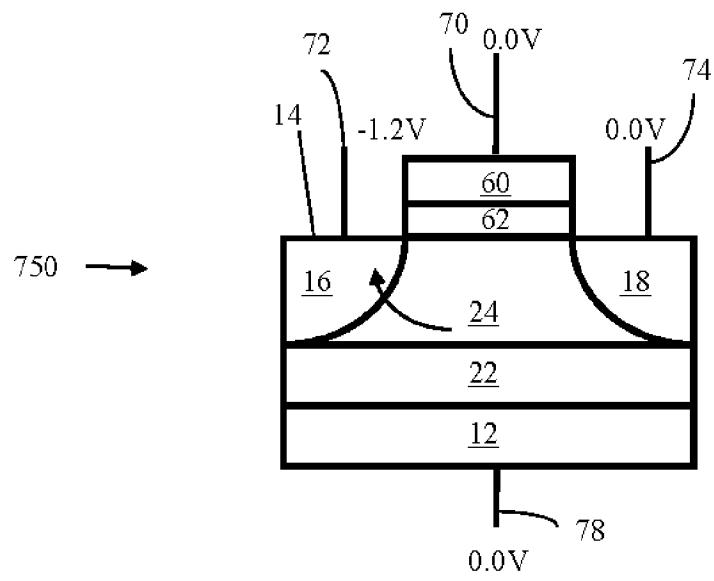


FIG. 96A

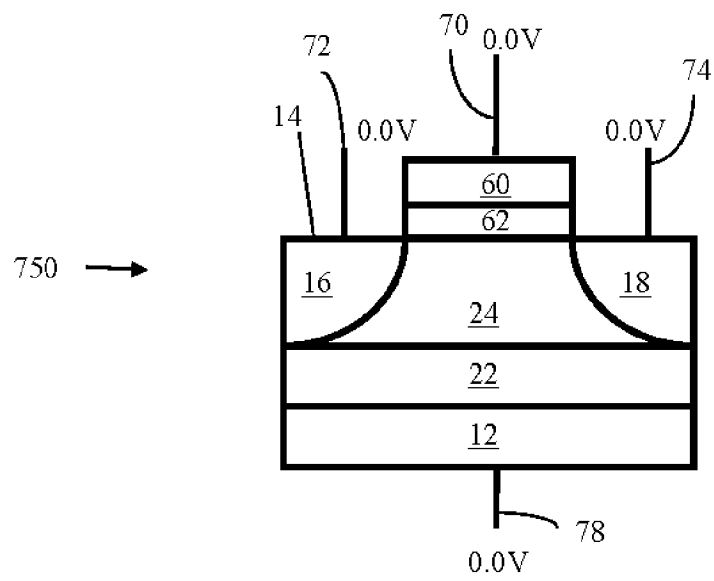


FIG. 96B

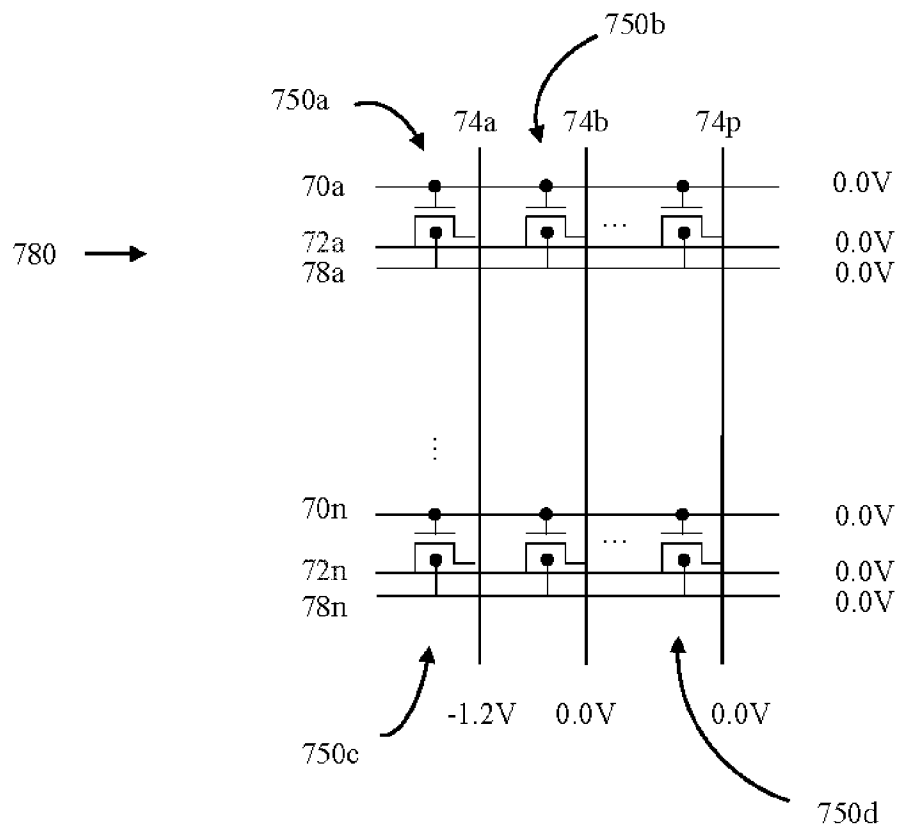


FIG. 97

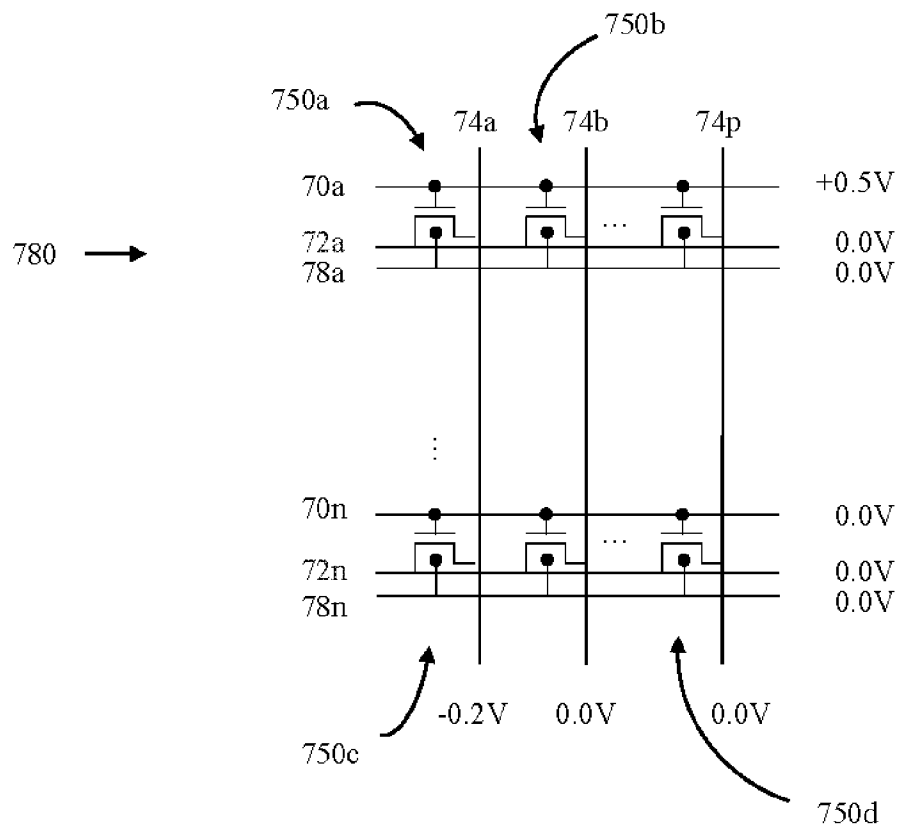


FIG. 98

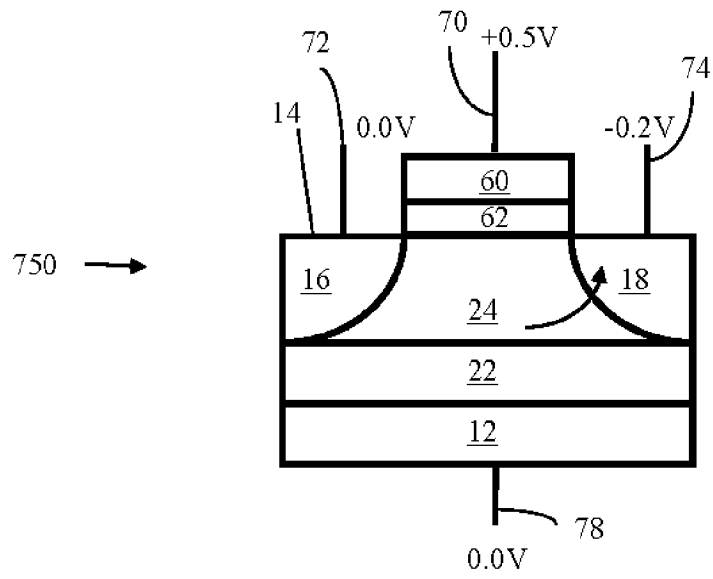


FIG. 99A

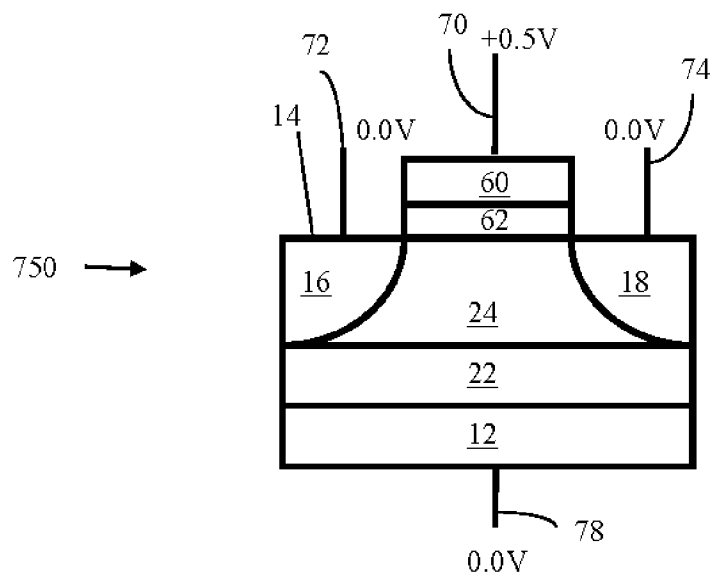


FIG. 99B

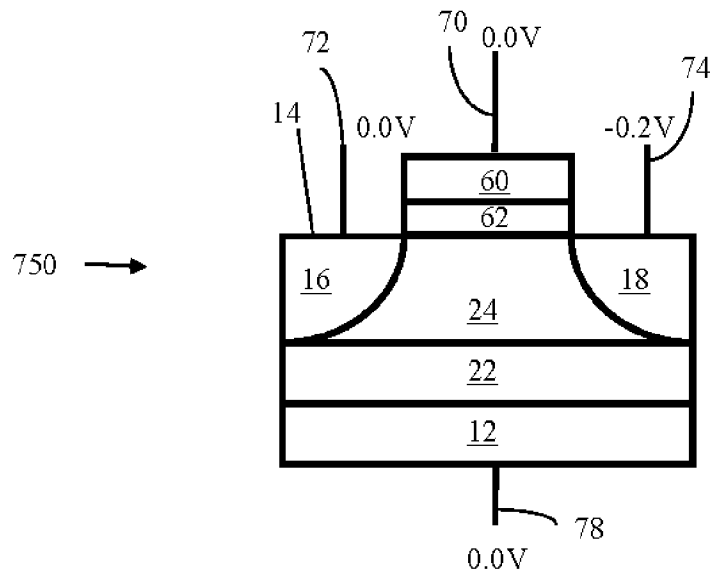


FIG. 99C

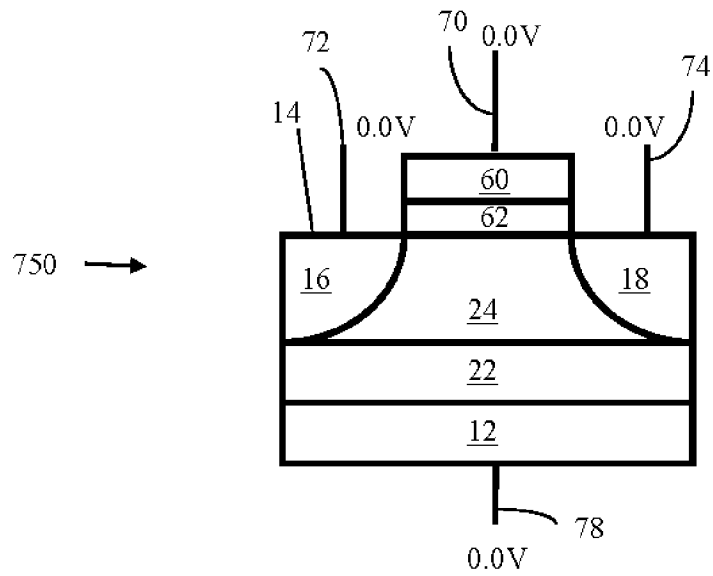


FIG. 99D

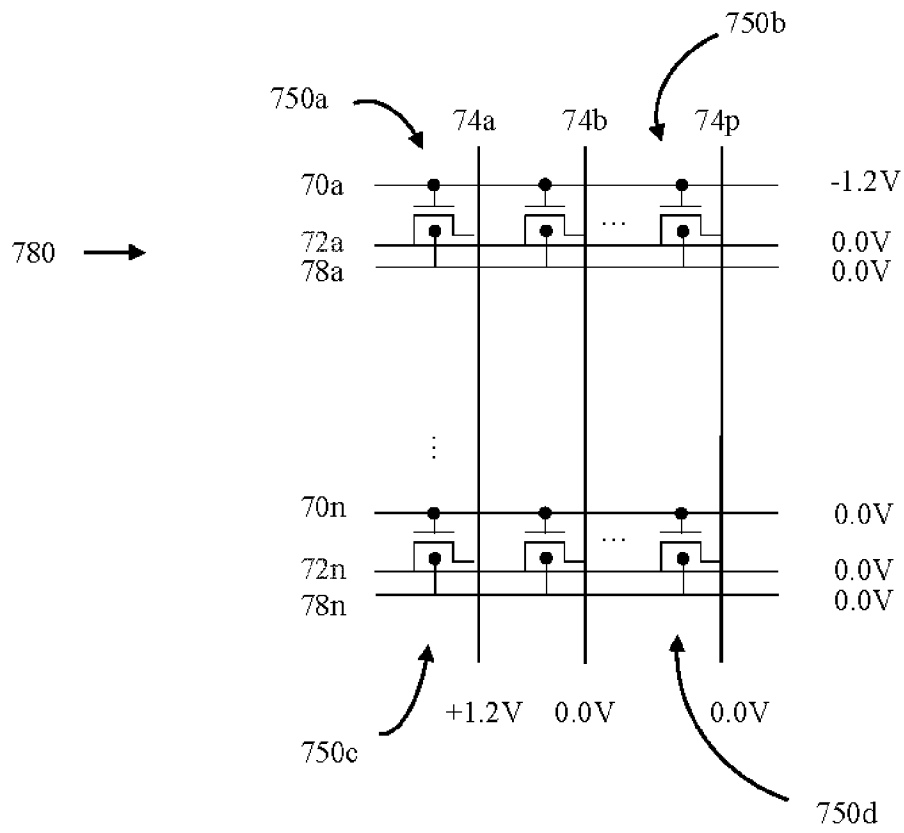


FIG. 100

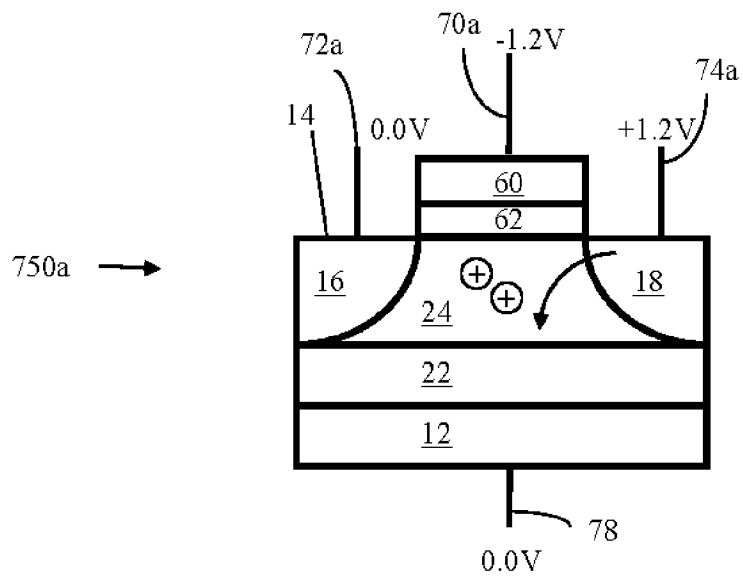


FIG. 101A

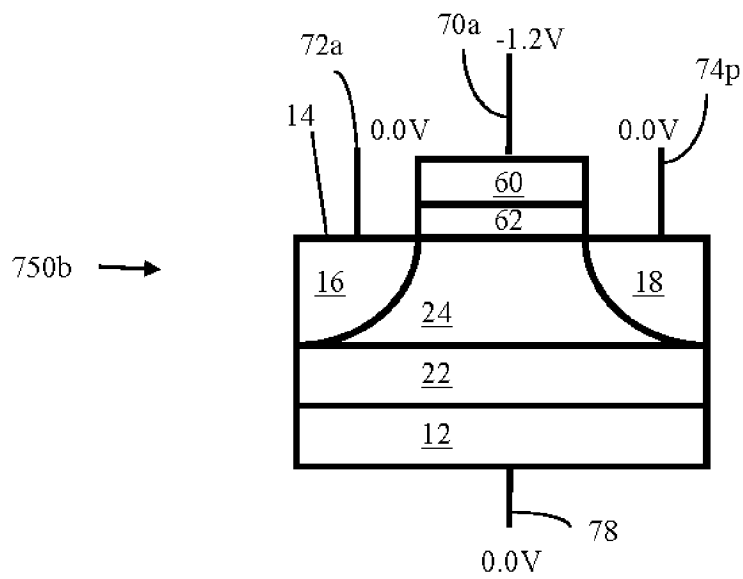


FIG. 101B

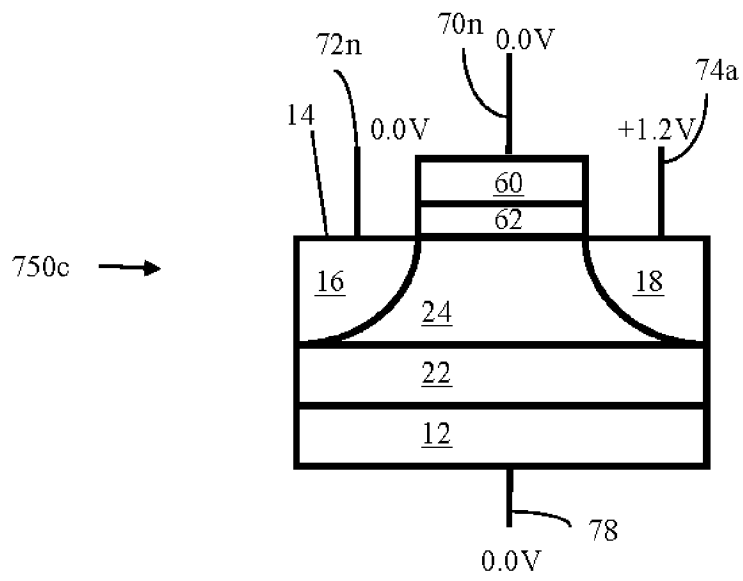


FIG. 101C

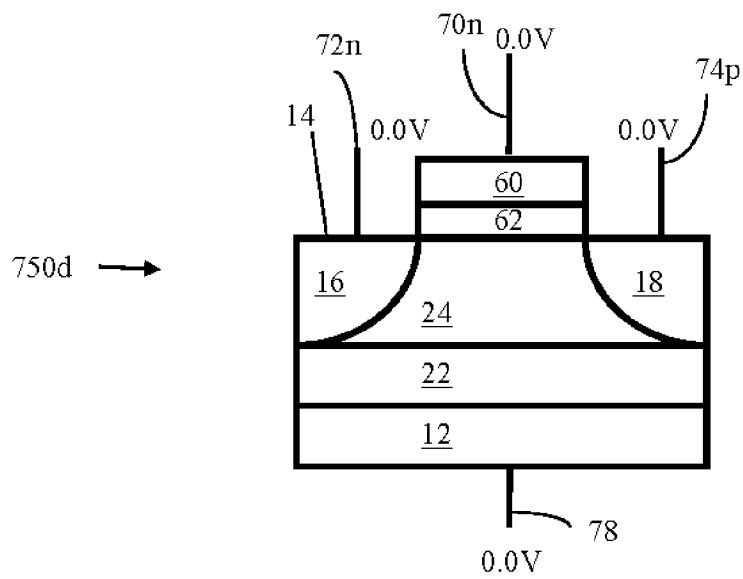


FIG. 101D

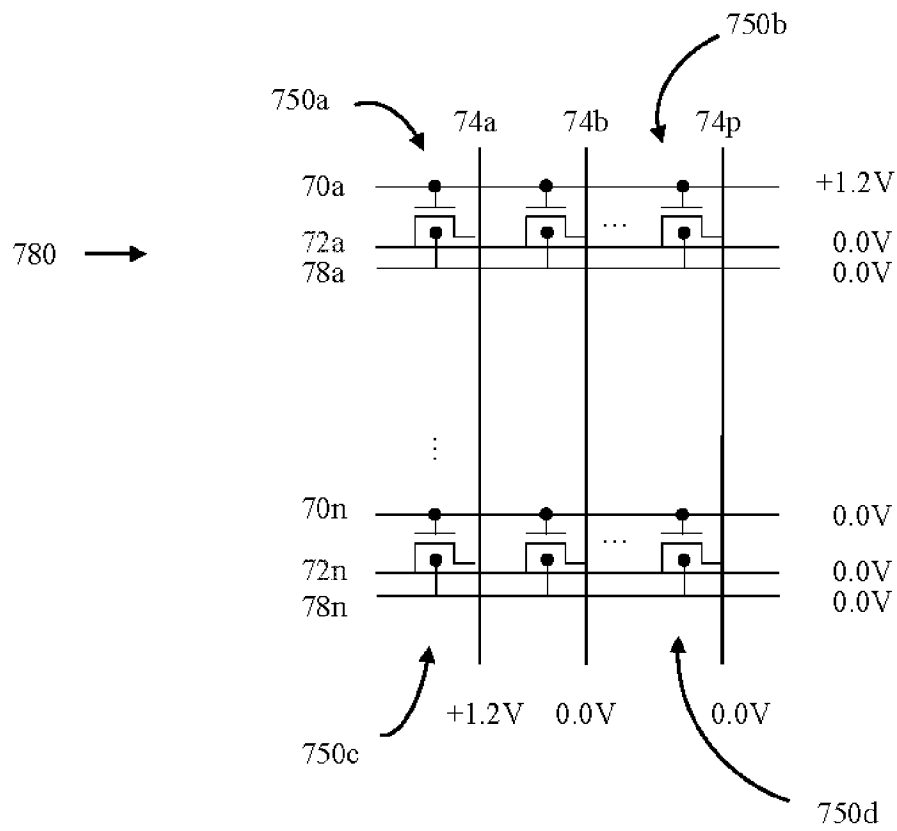


FIG. 102

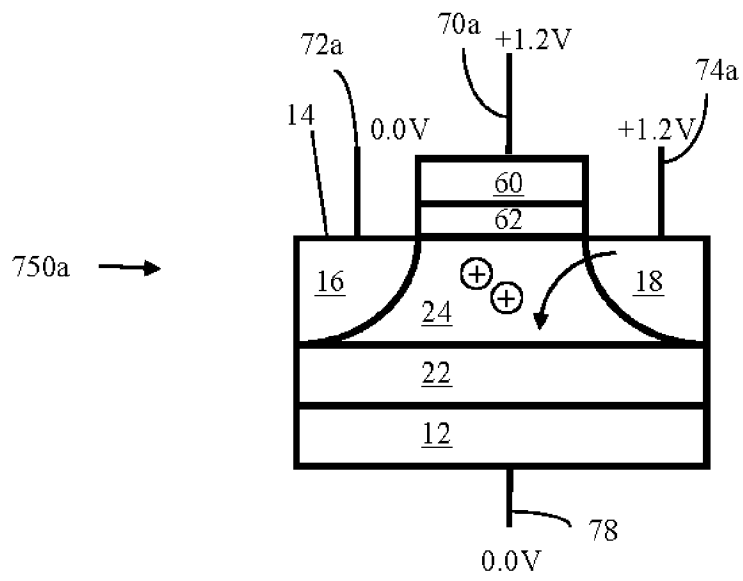


FIG. 103A

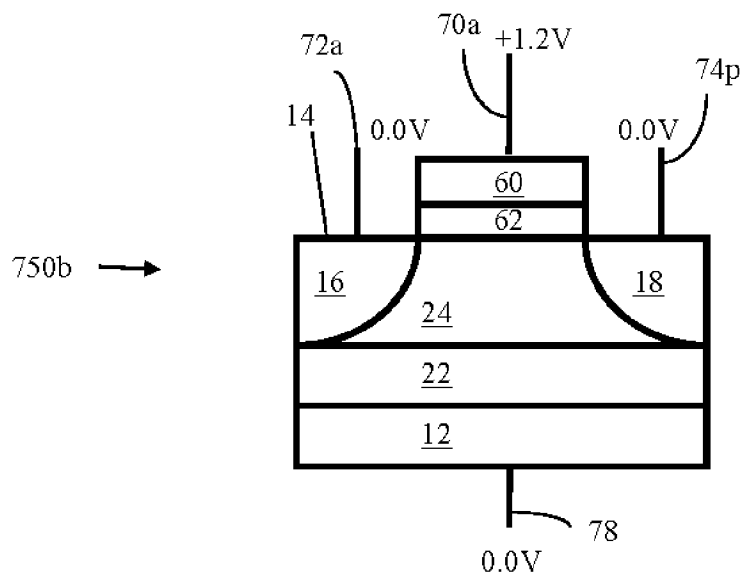


FIG. 103B

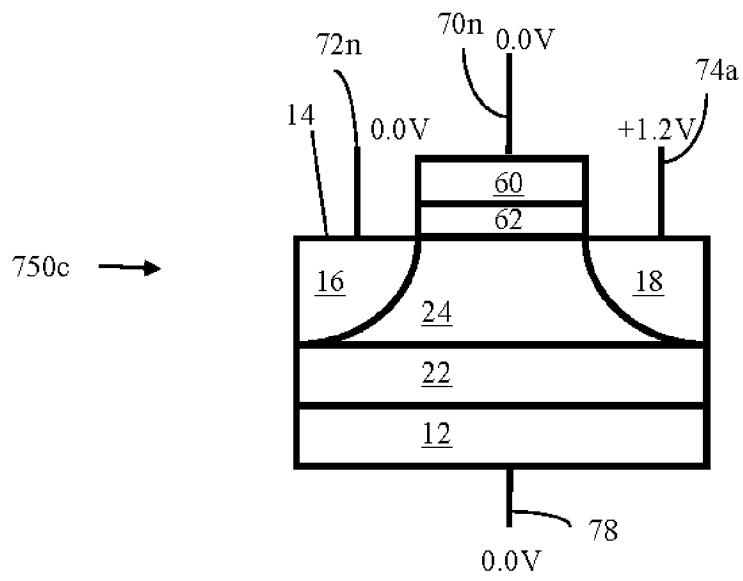


FIG. 103C

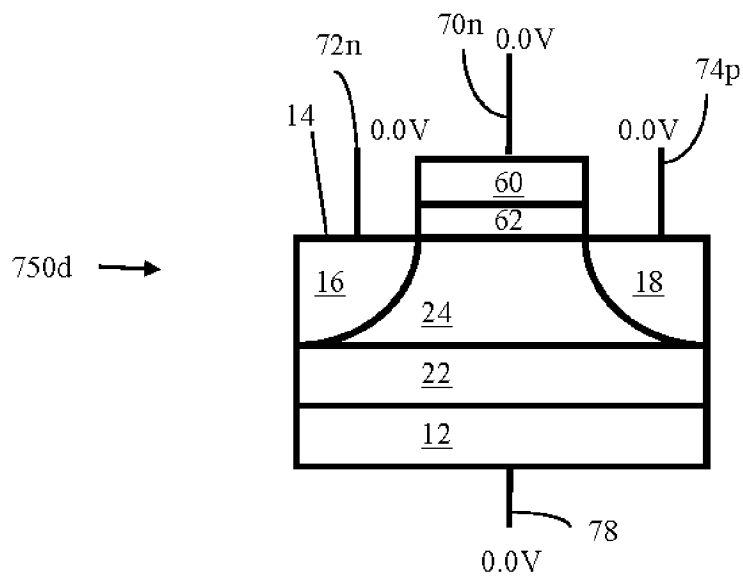


FIG. 103D

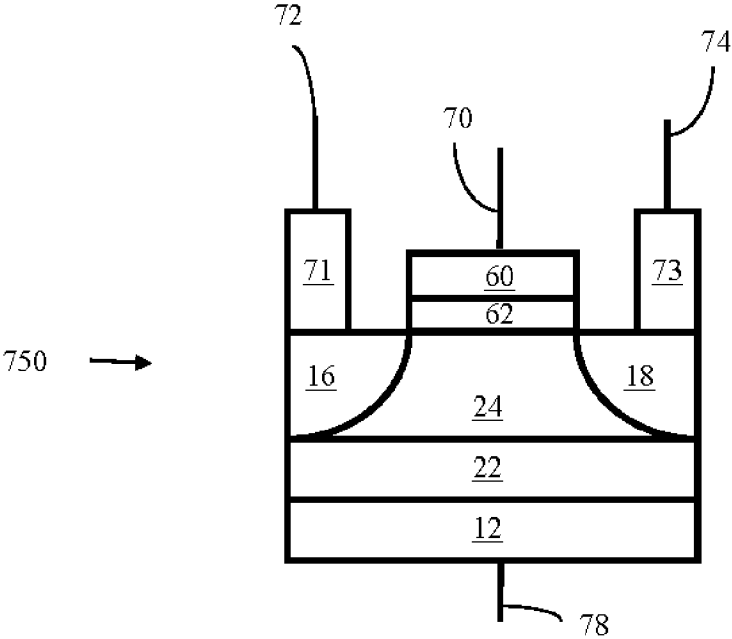


FIG. 104

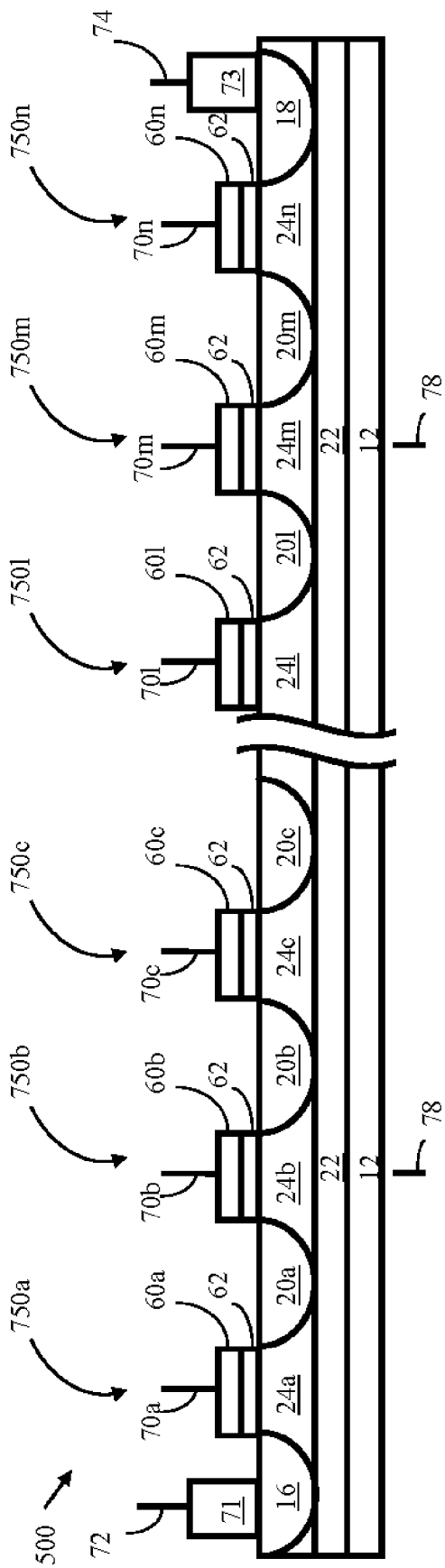


FIG. 106A

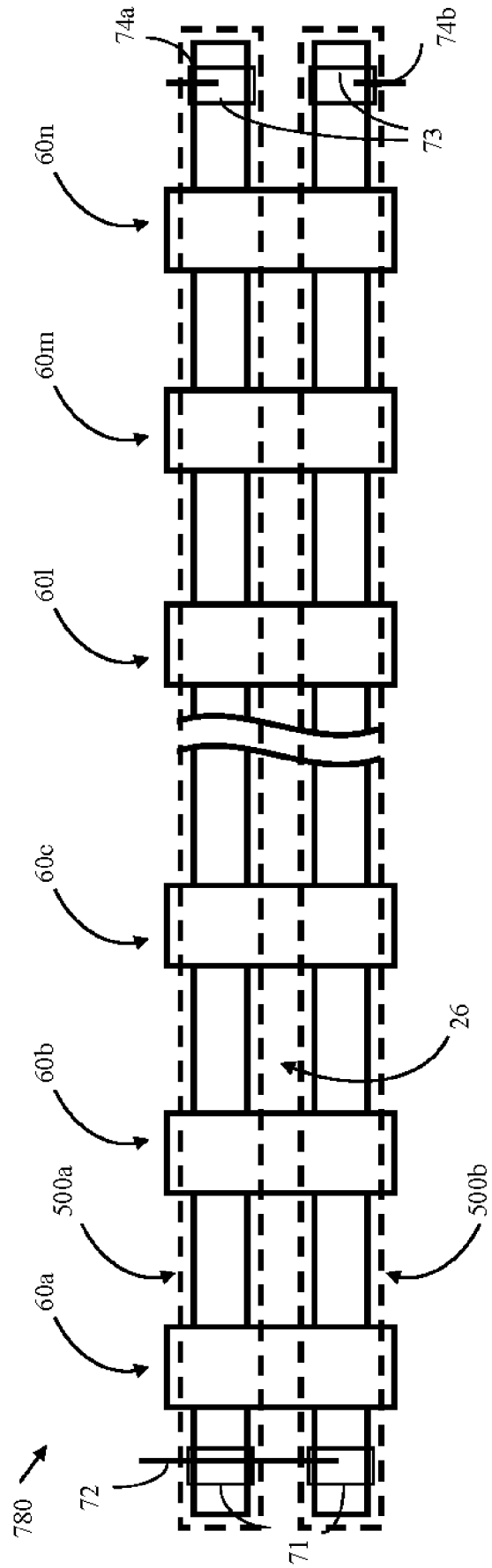


FIG. 106B

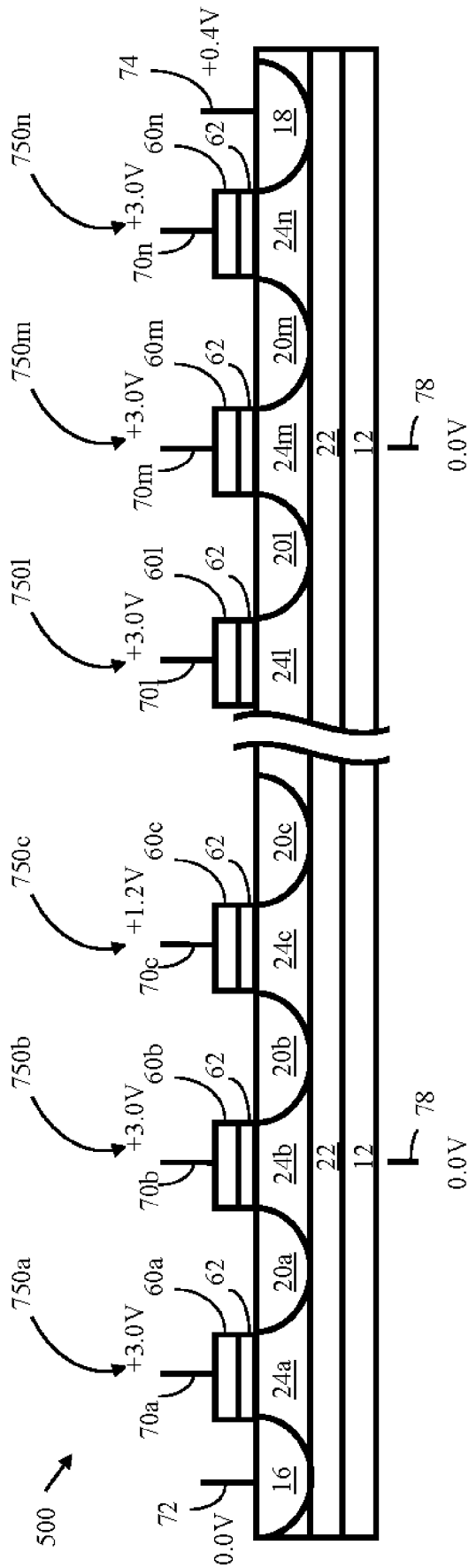


FIG. 108

780 

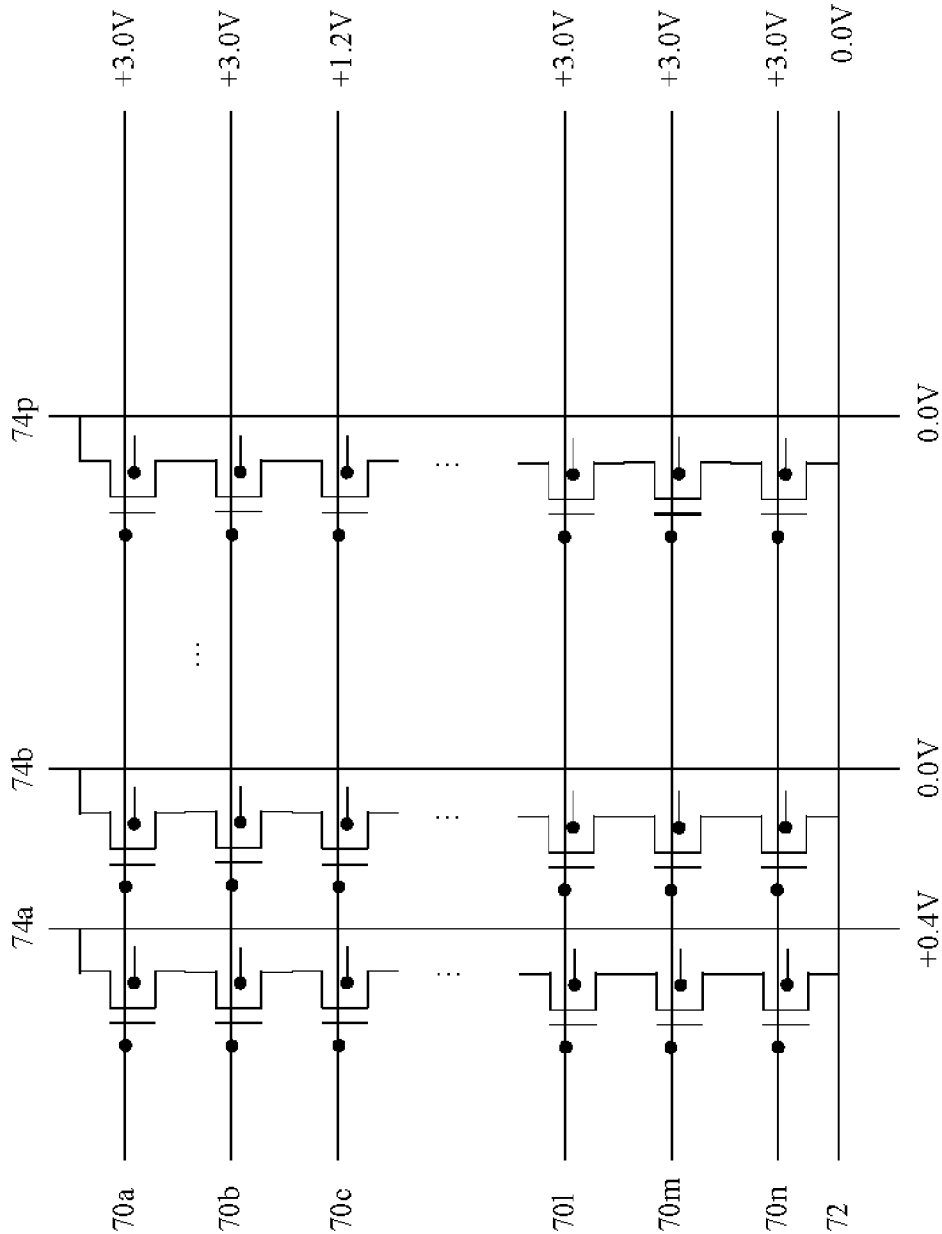
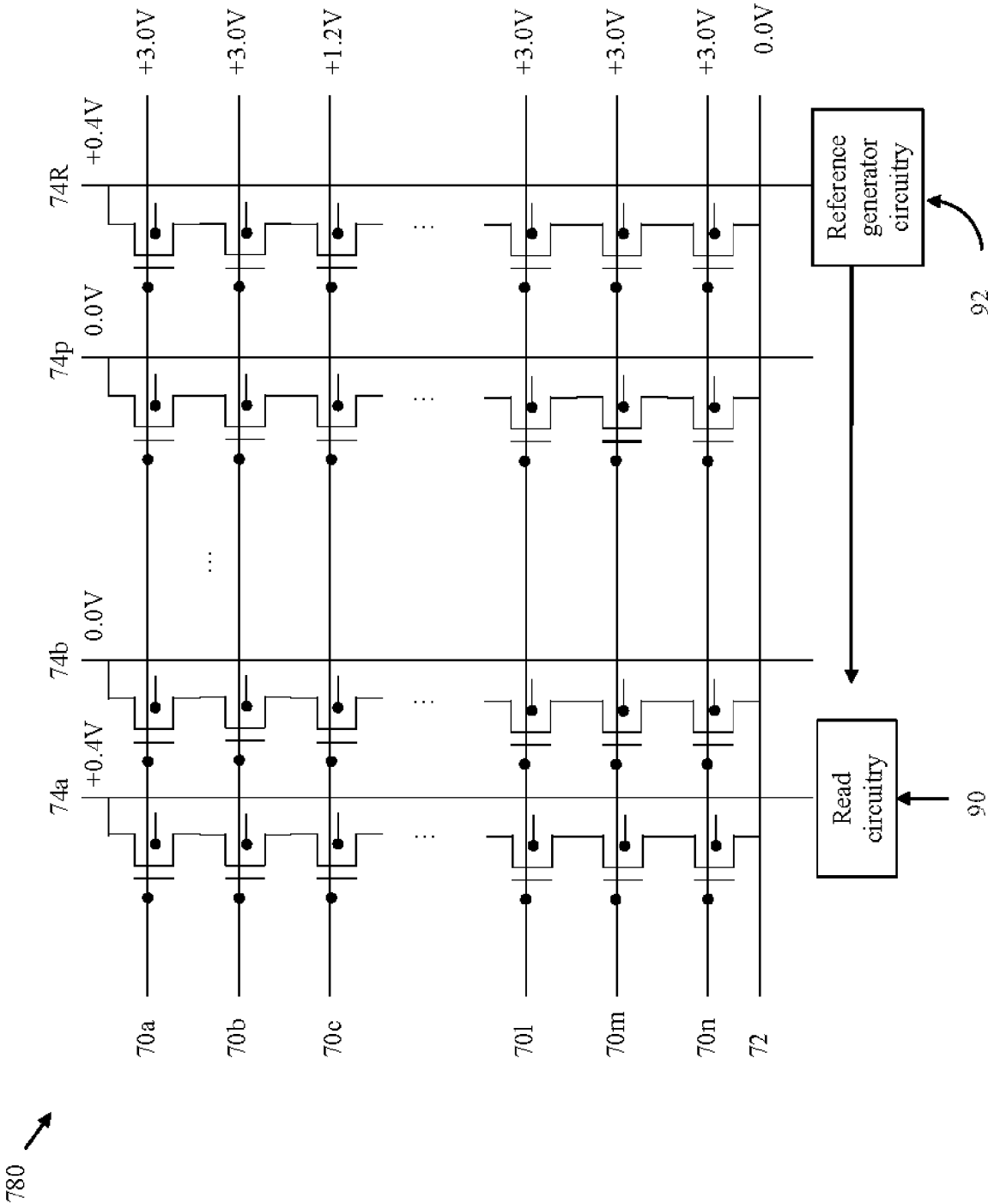


FIG. 109A



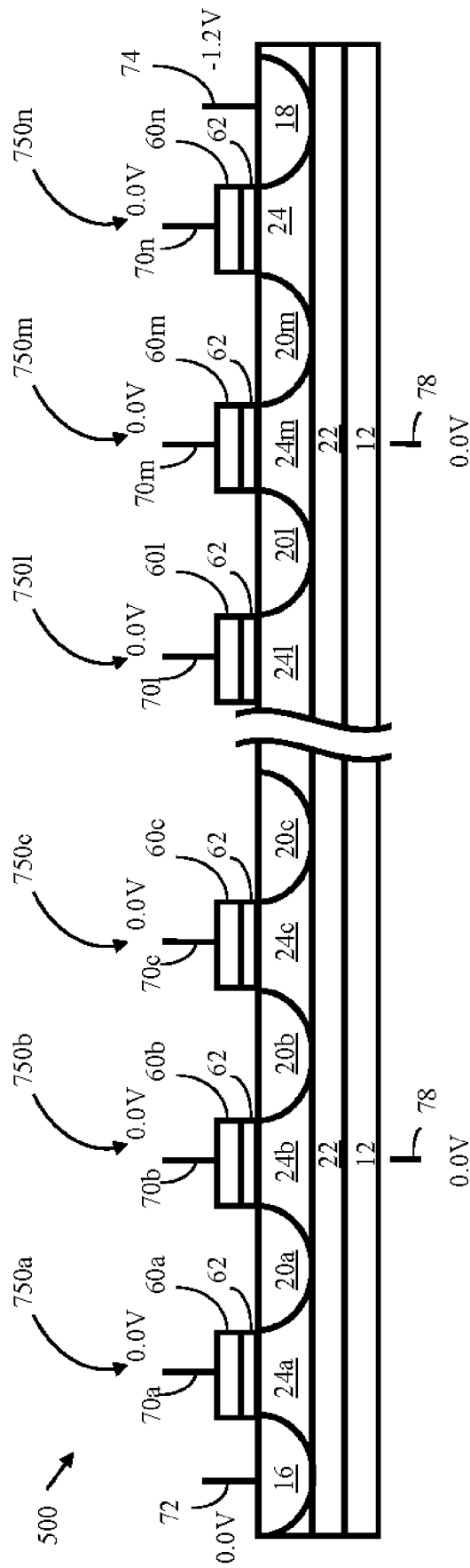


FIG. 110

780 

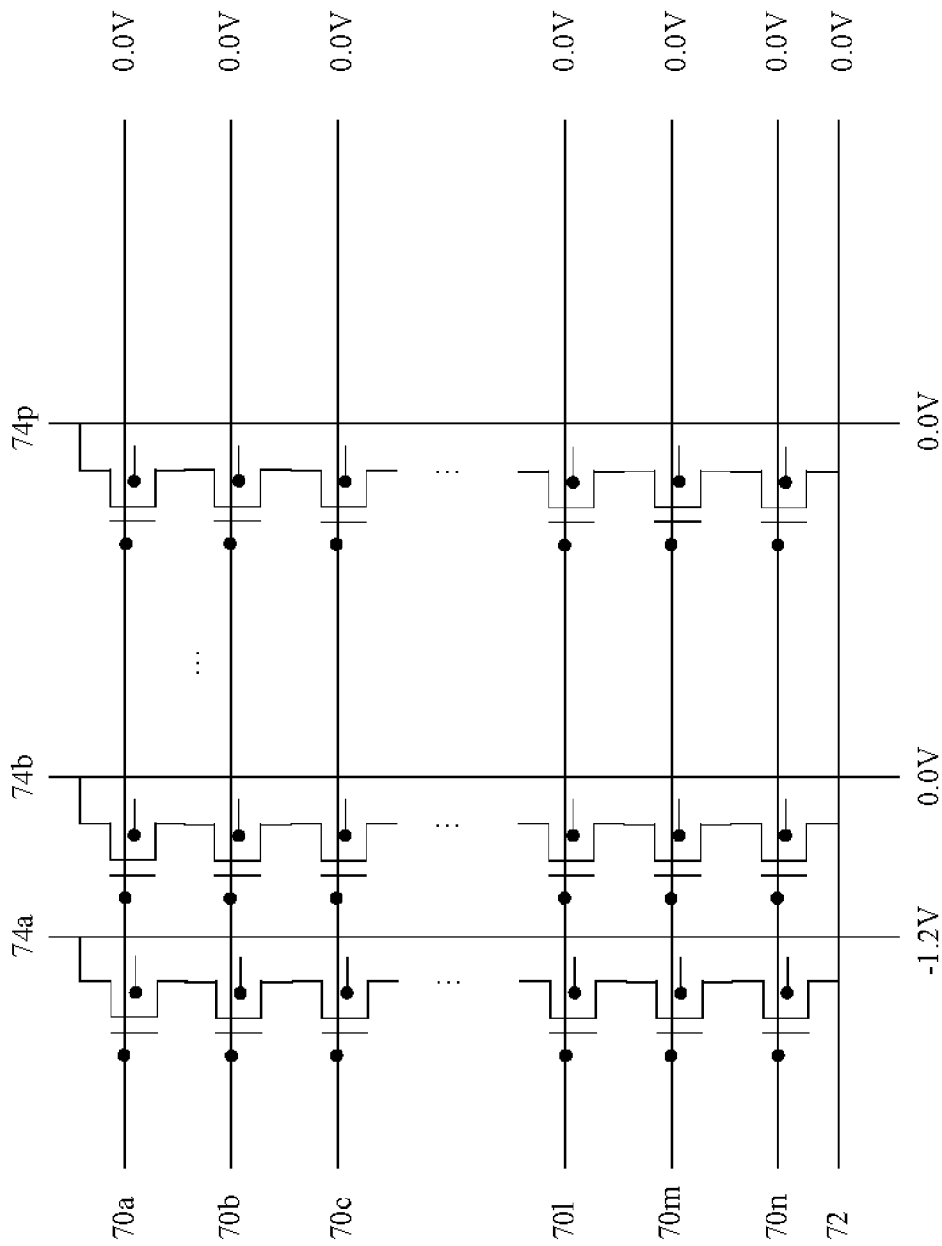


FIG. 111

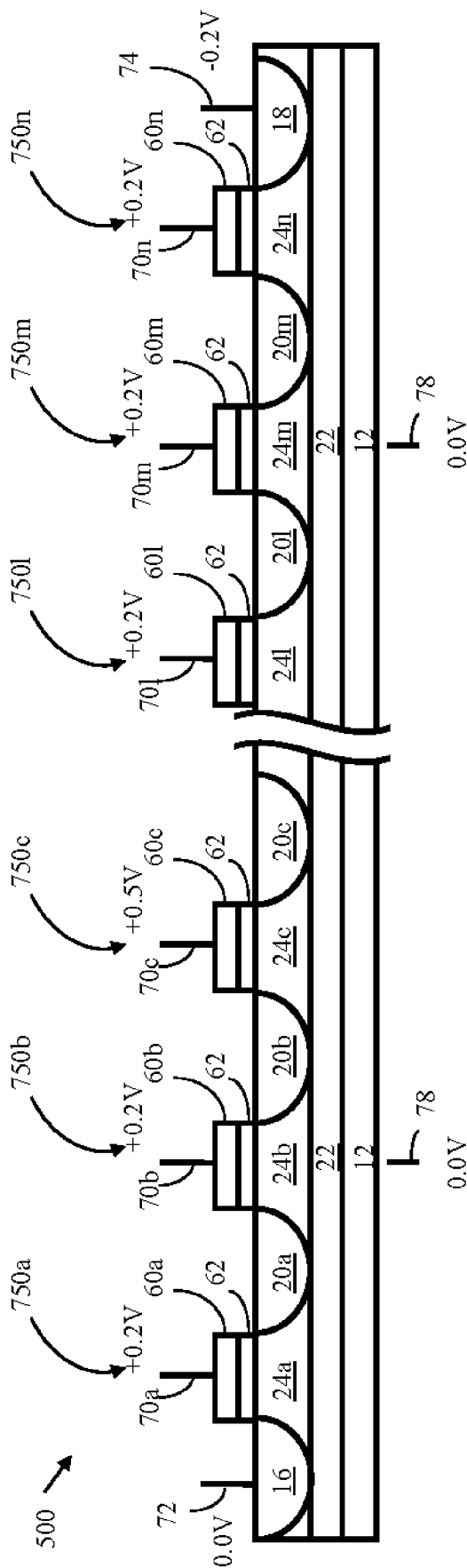


FIG. 112A

780 

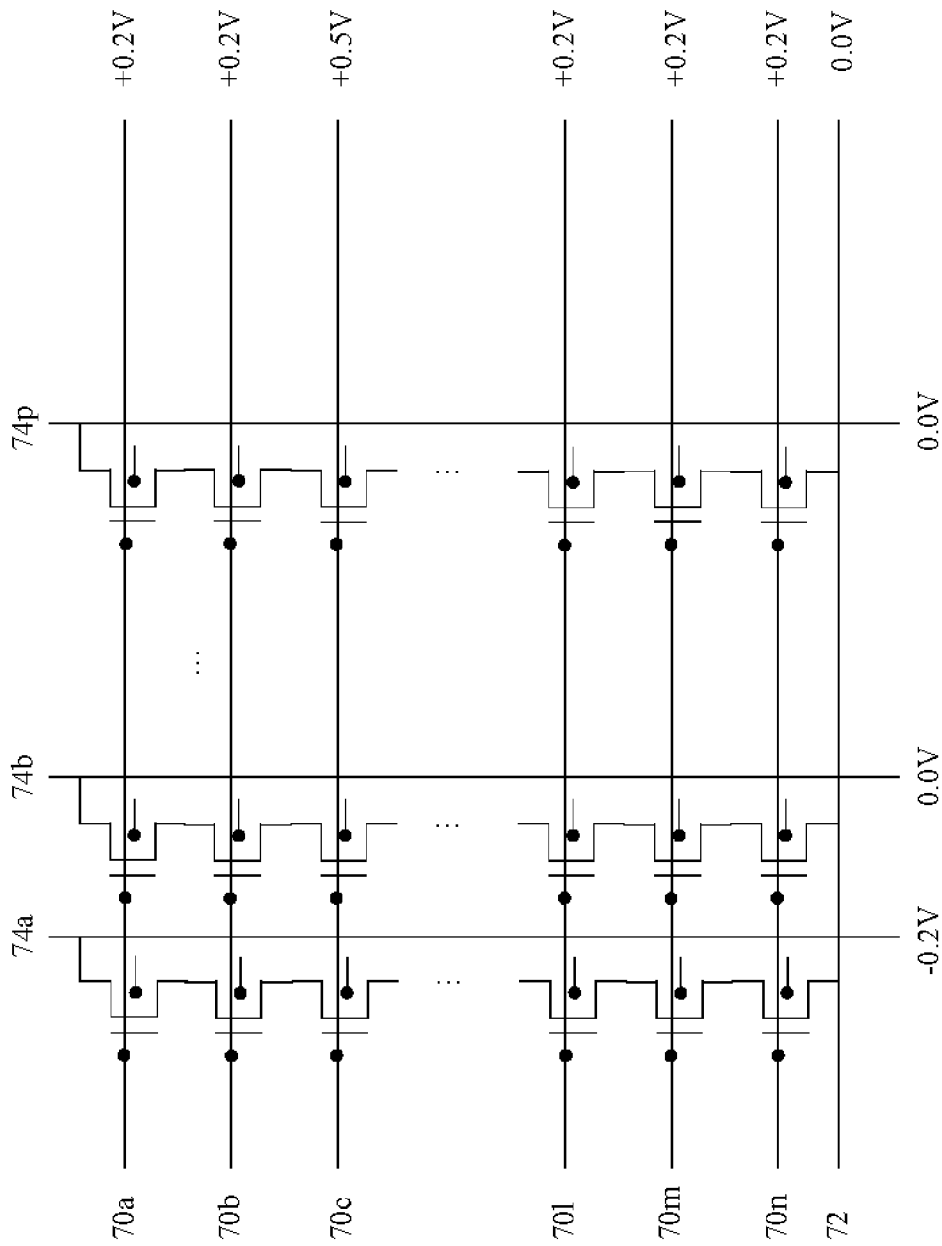


FIG. 112B

780 

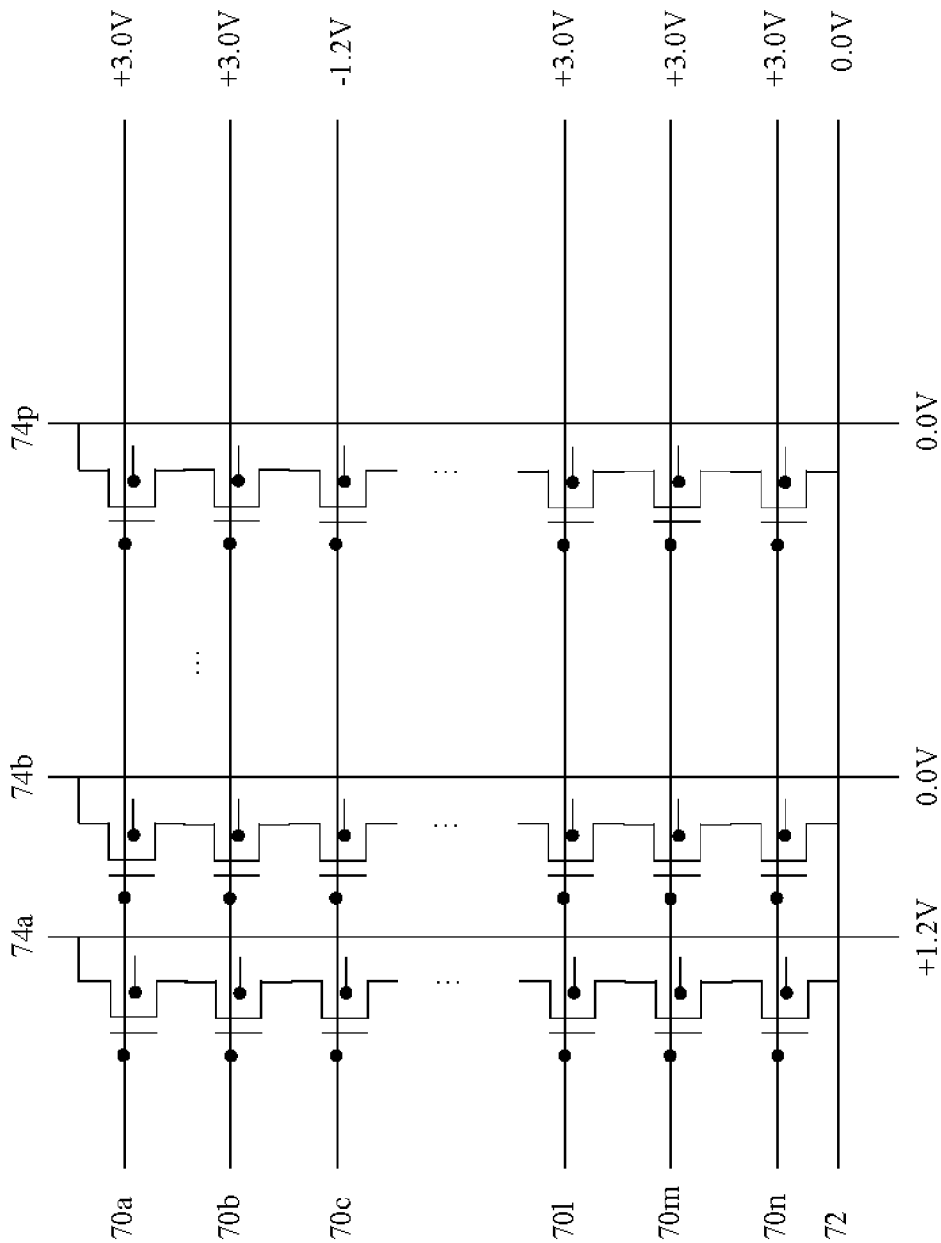


FIG. 113B

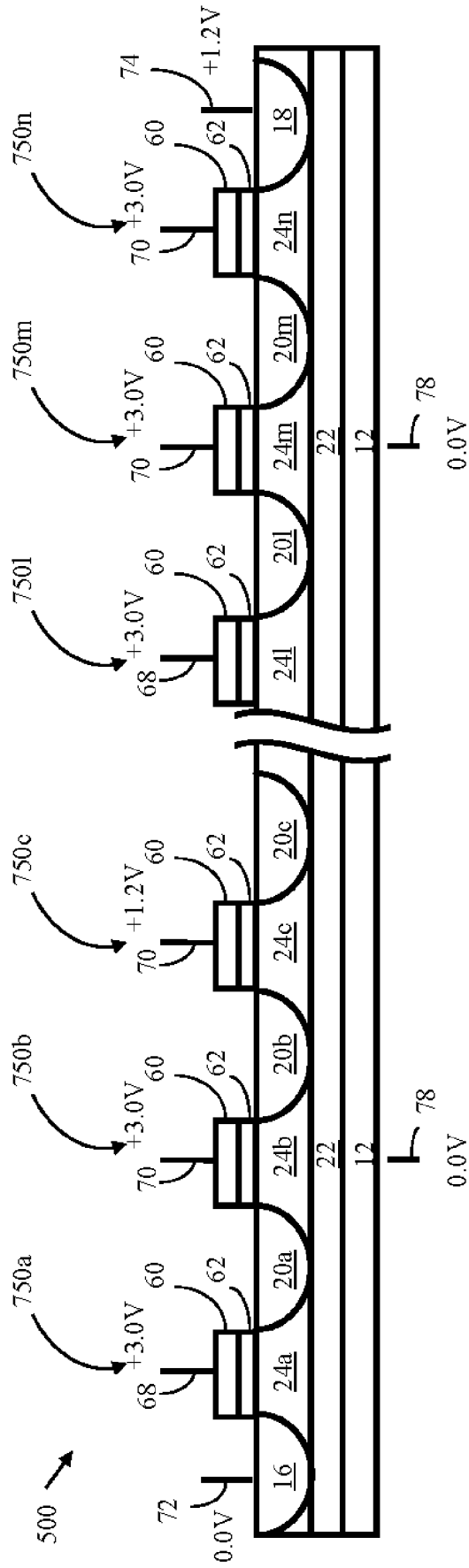


FIG. 114A

780 

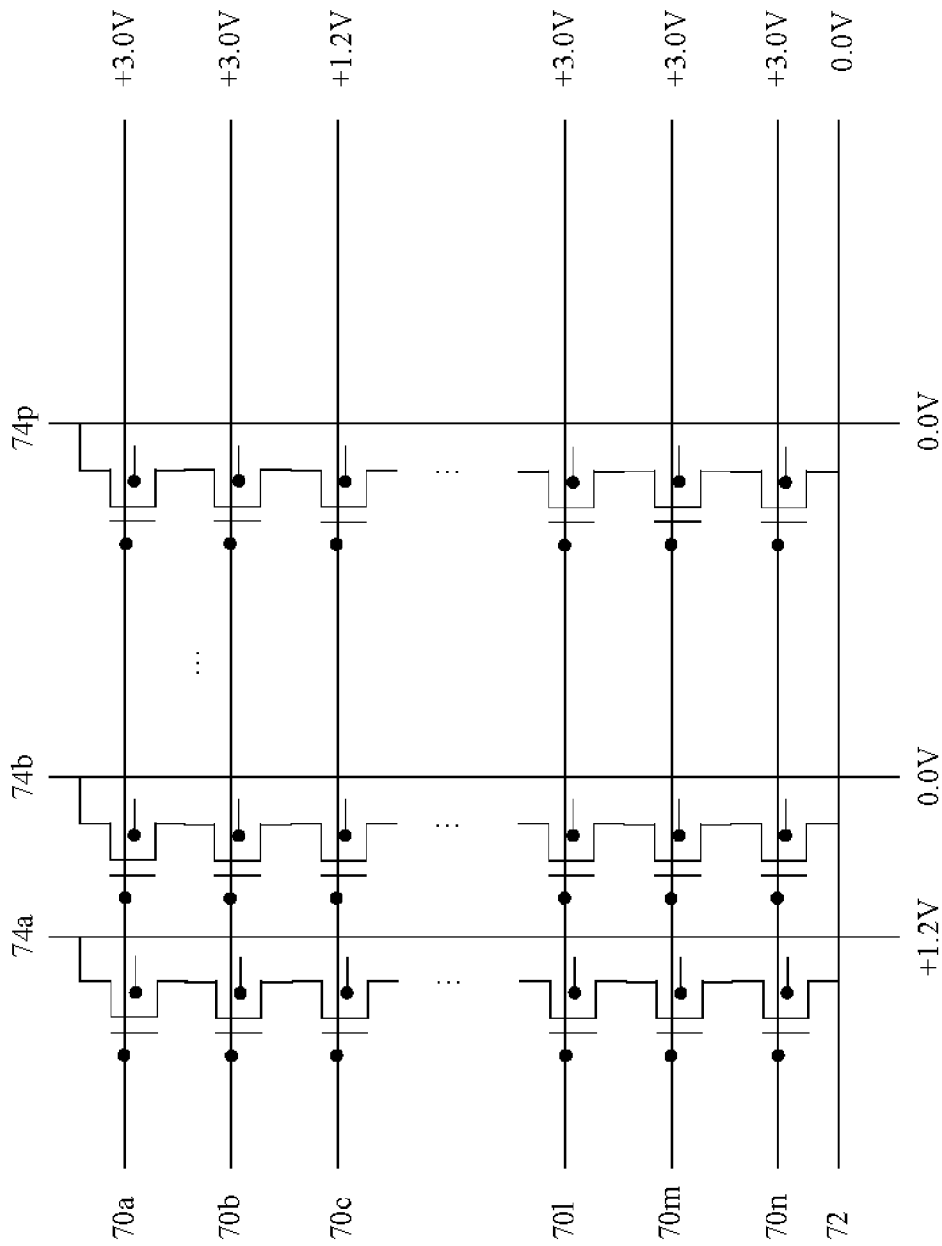


FIG. 114B

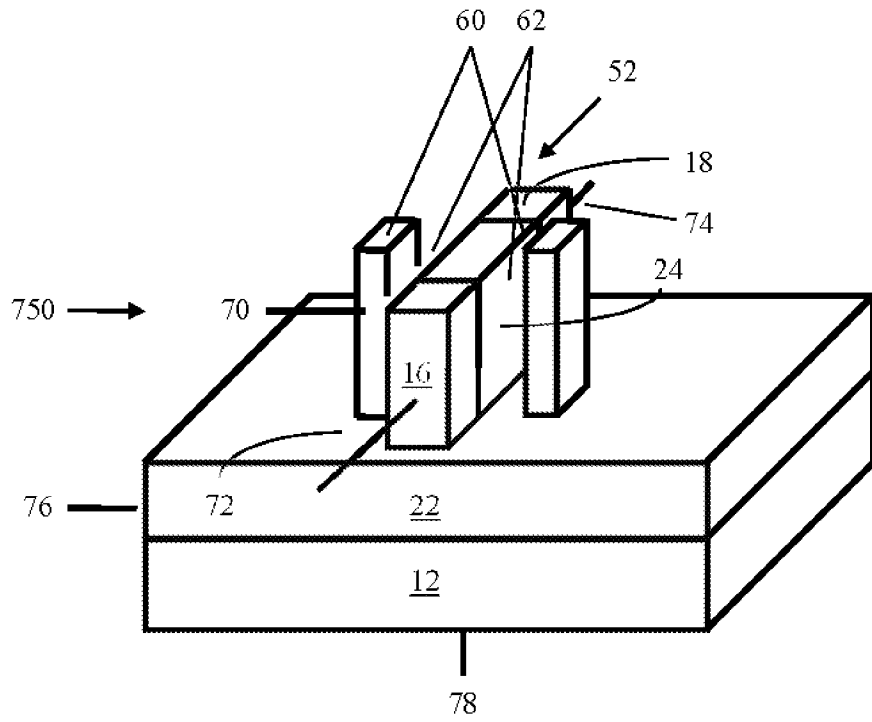


FIG. 115A

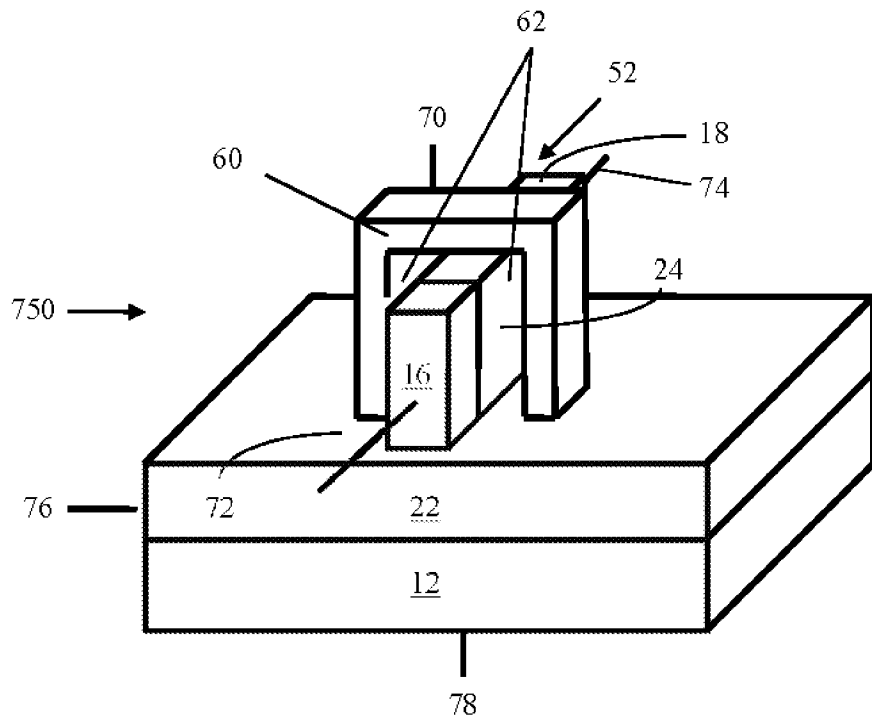


FIG. 115B

Floating Body 24 is positively charged

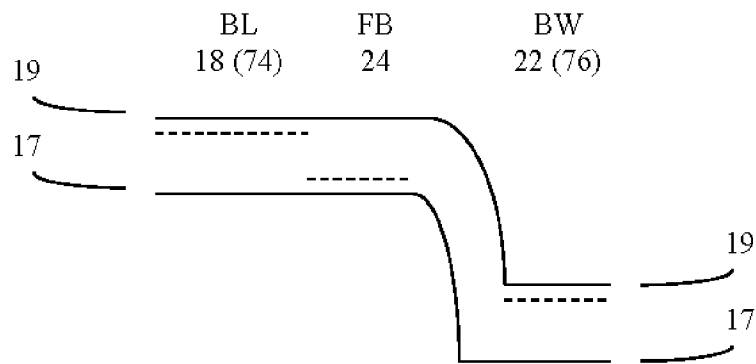


FIG. 116A

FB is neutrally charged: $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

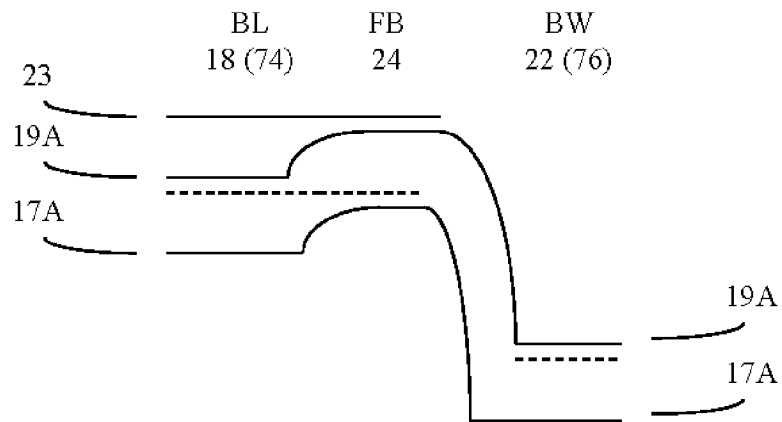


FIG. 116B

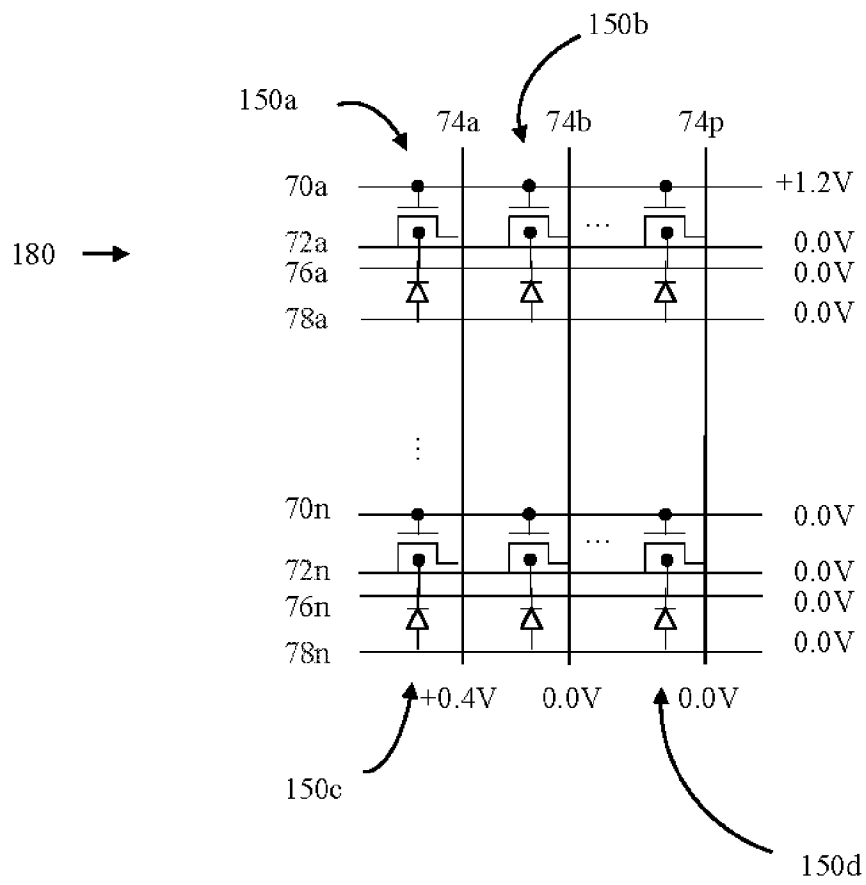


FIG. 117

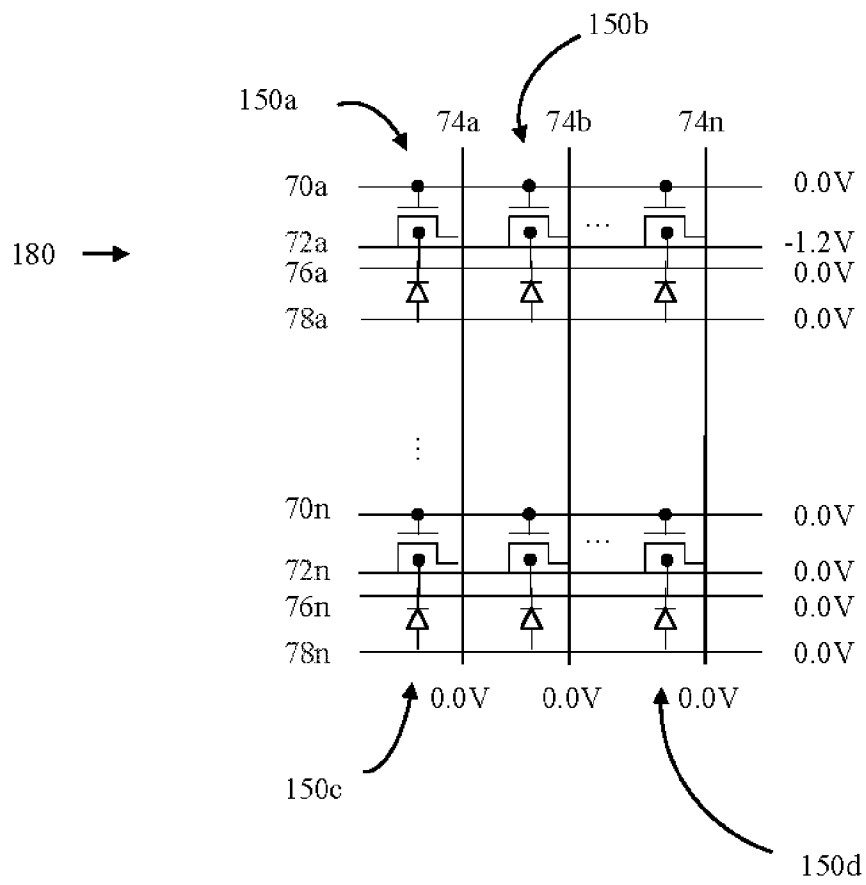
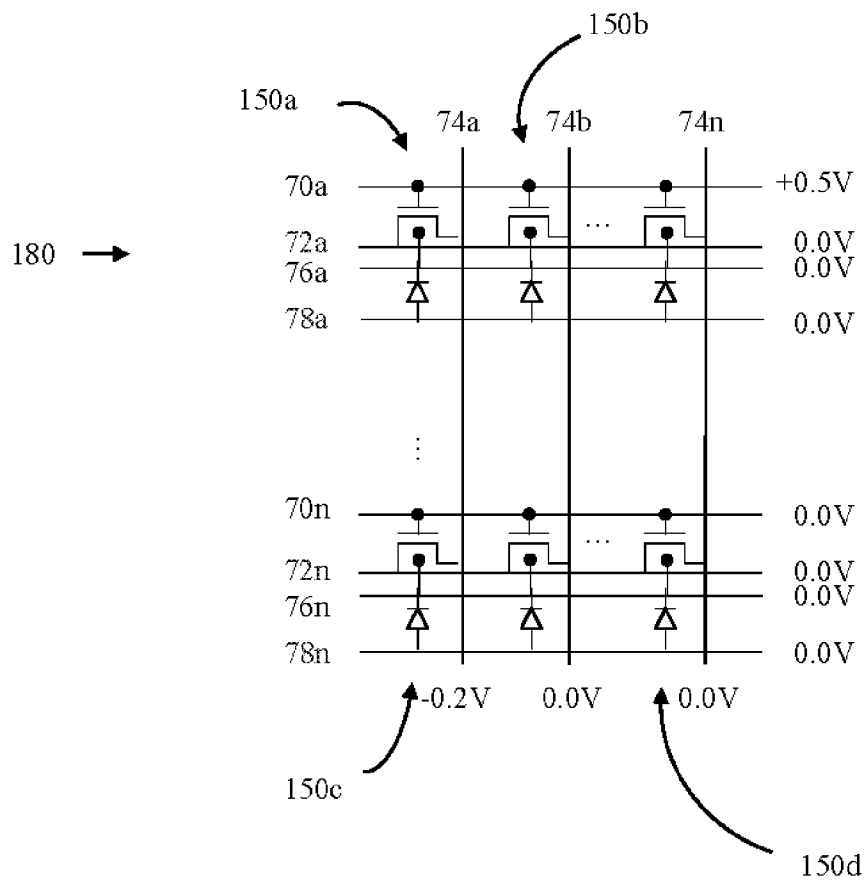


FIG. 118



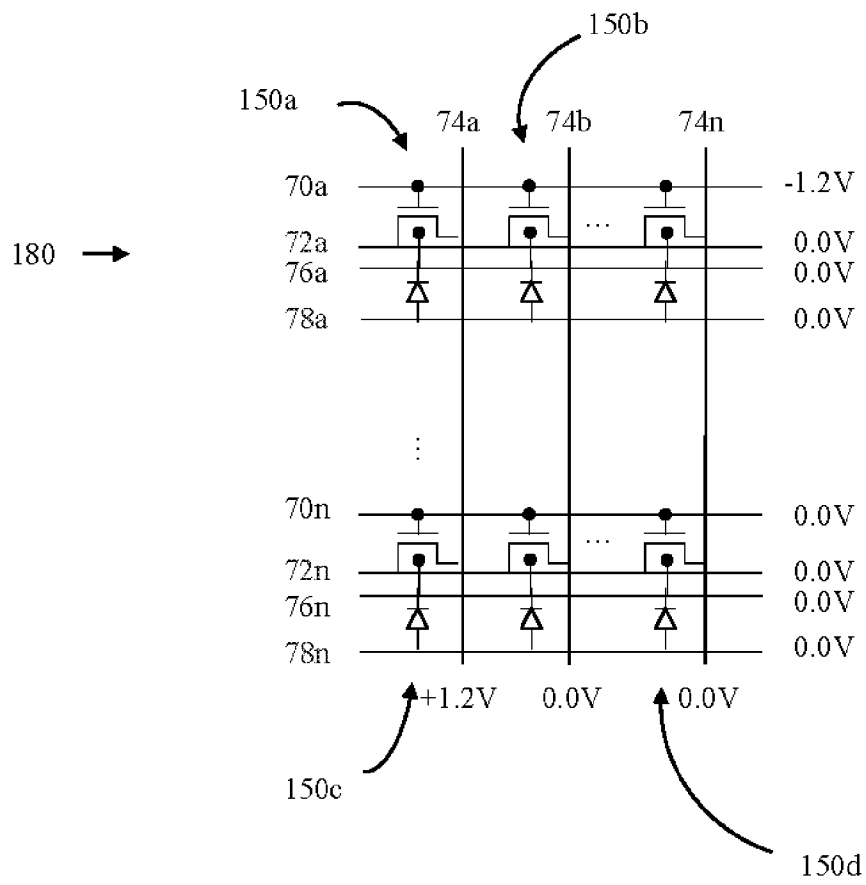


FIG. 120A

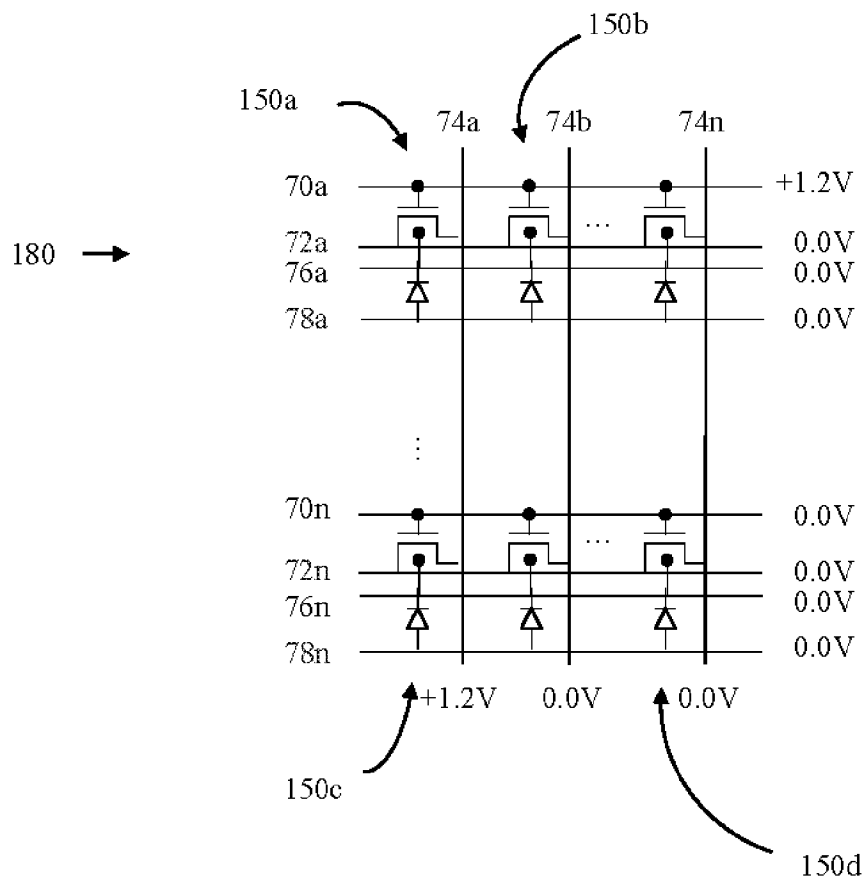


FIG. 120B

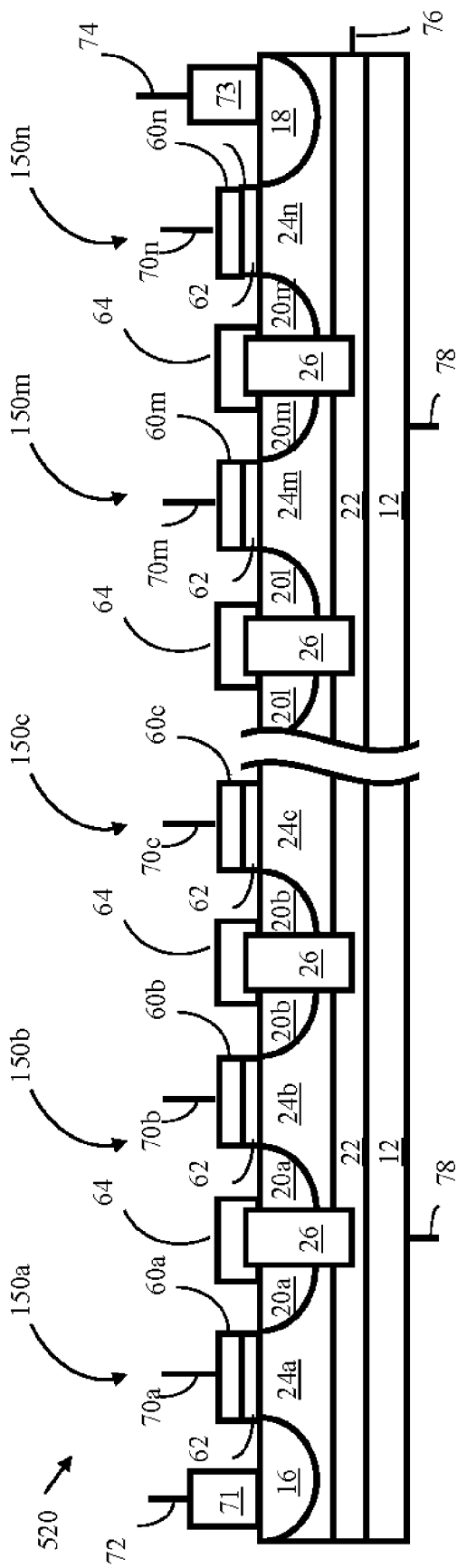


FIG. 121A

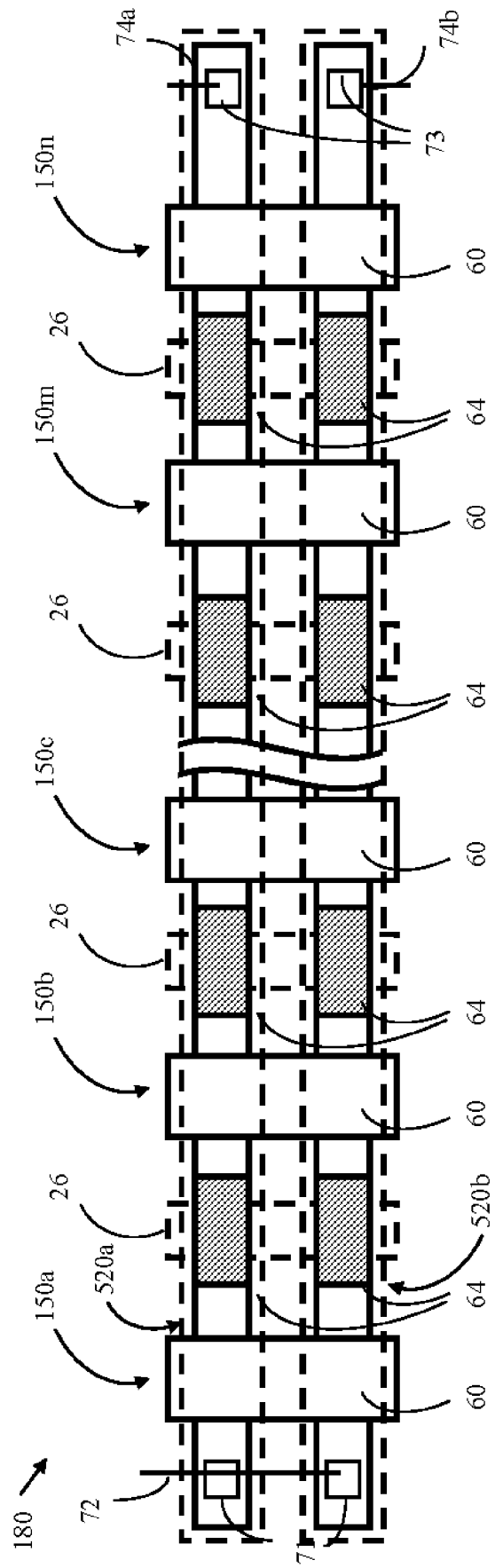


FIG. 121B

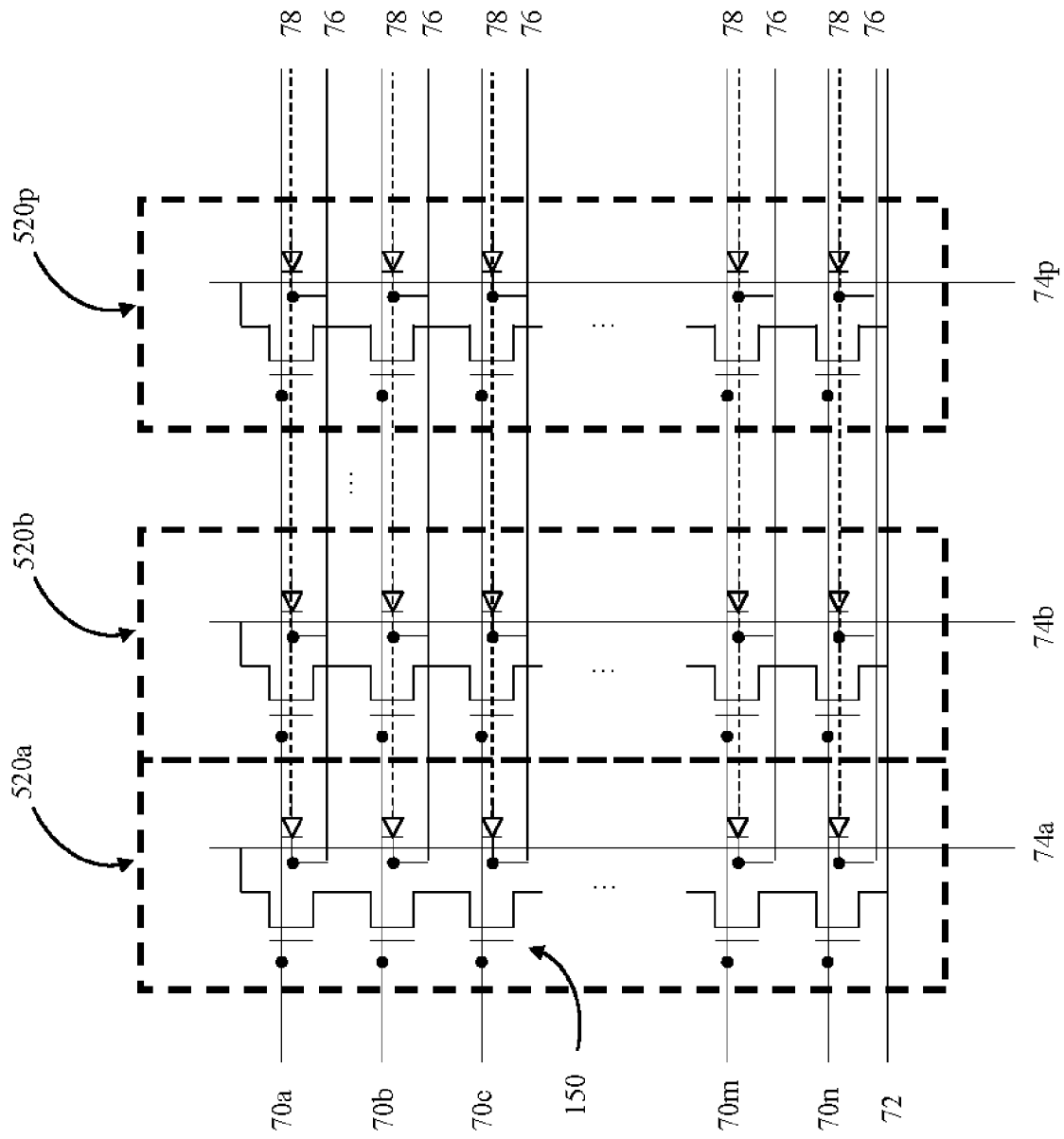


FIG. 121C

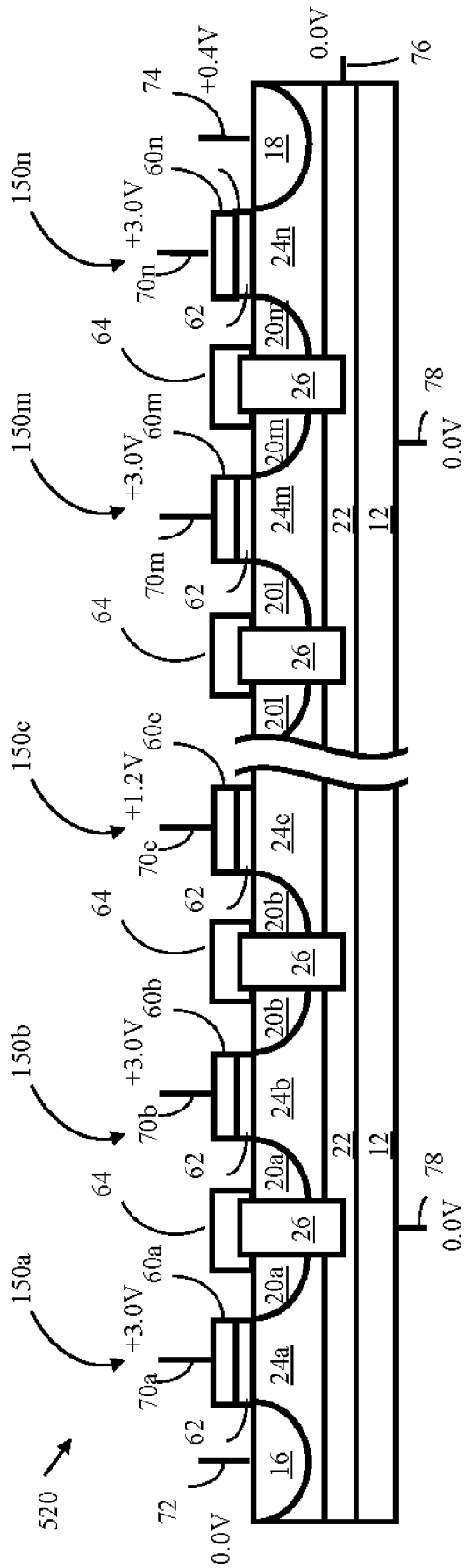


FIG. 122

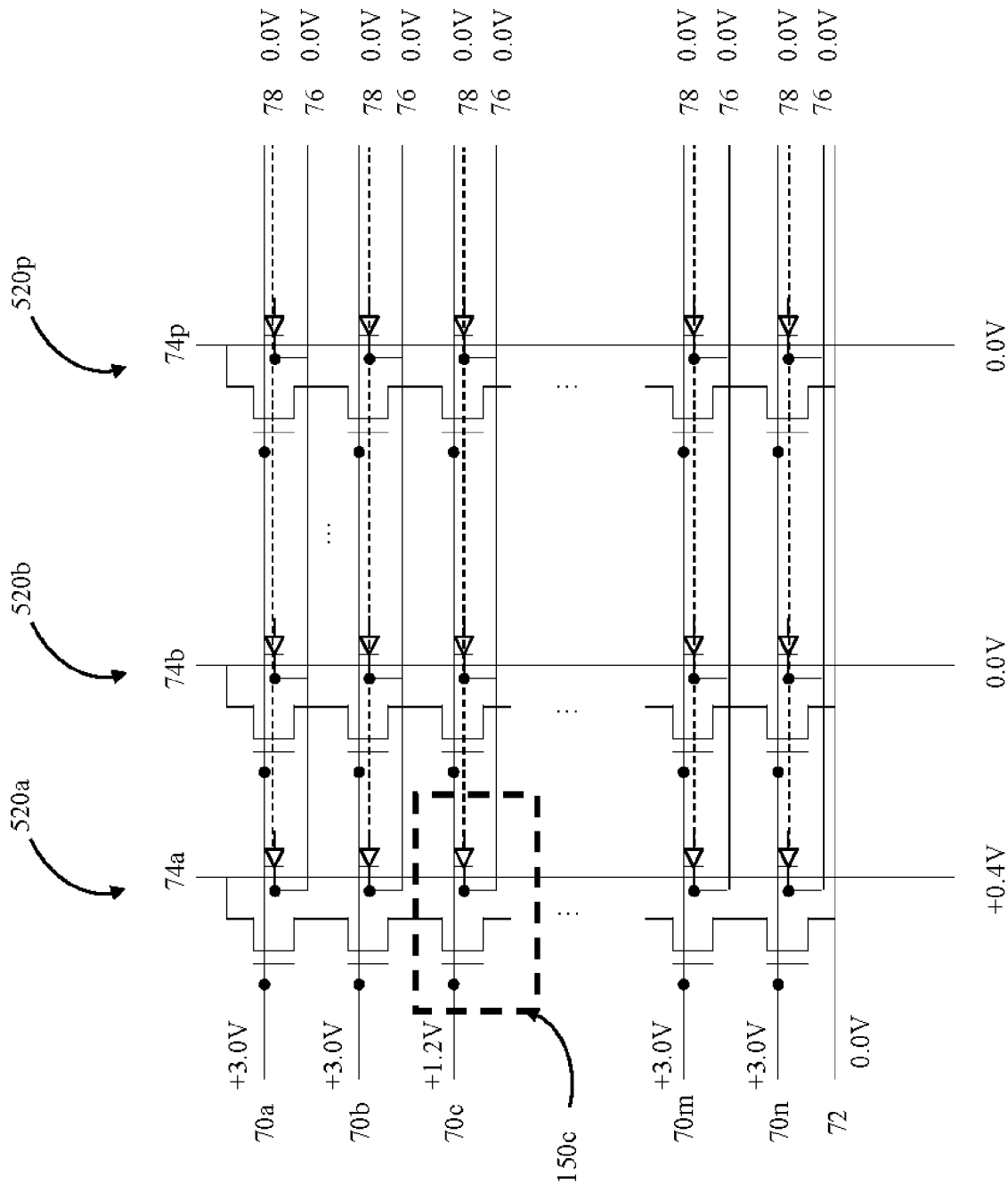


FIG. 123A

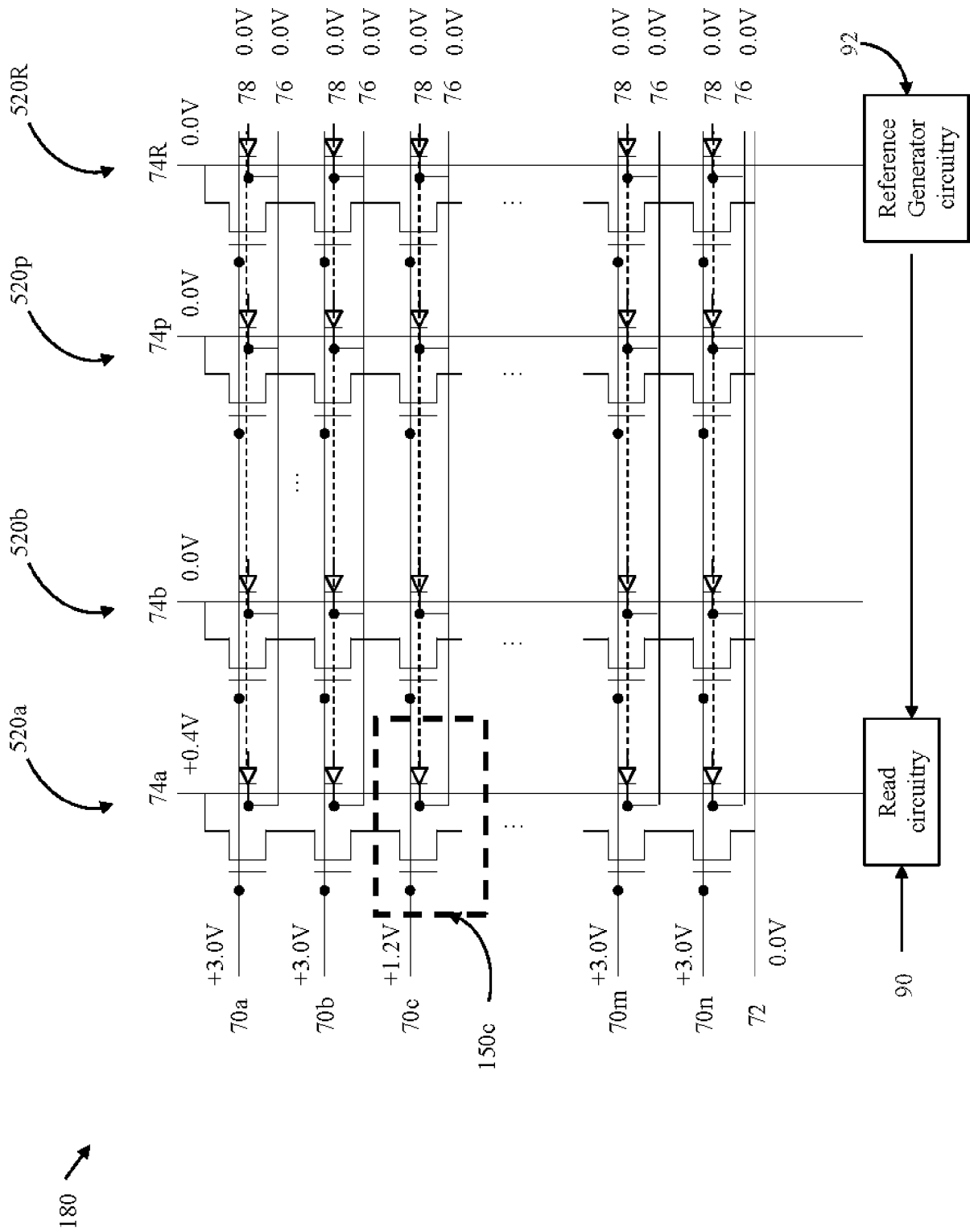


FIG. 123B

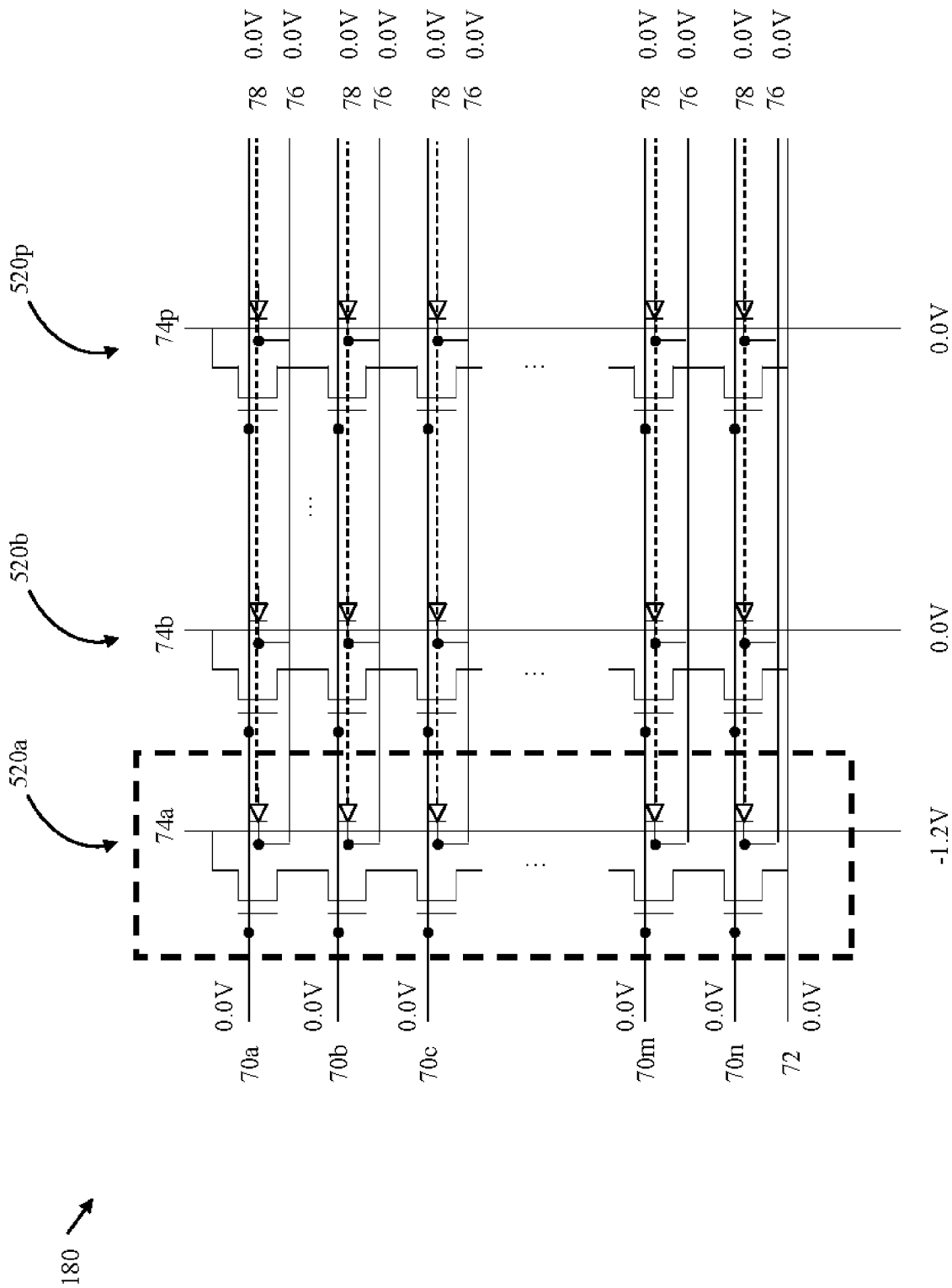


FIG. 125

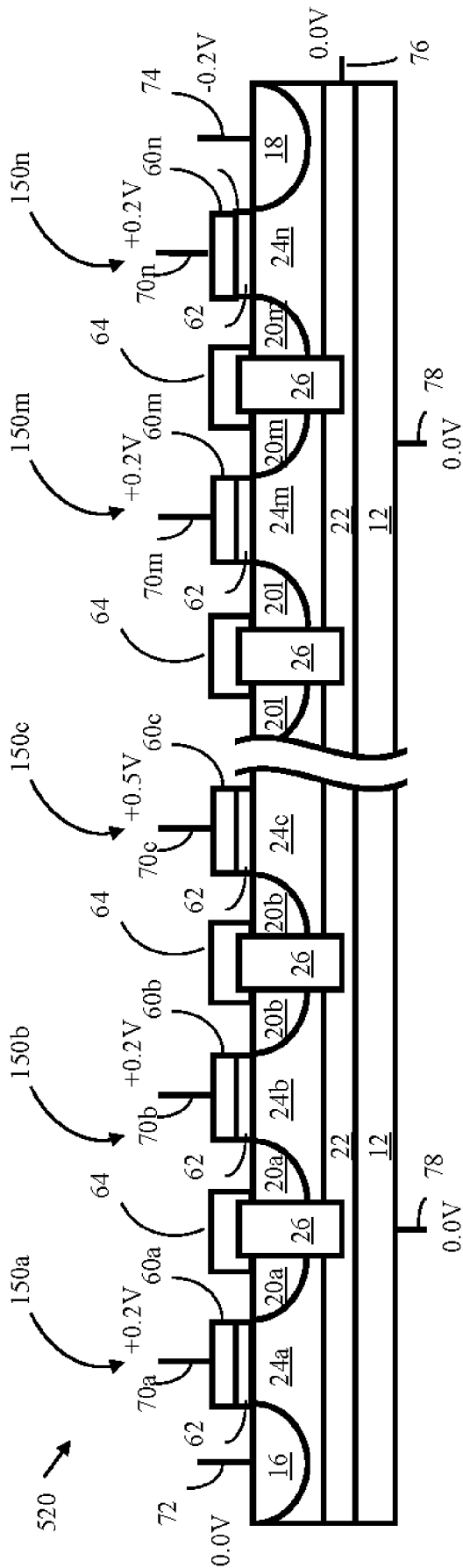


FIG. 126

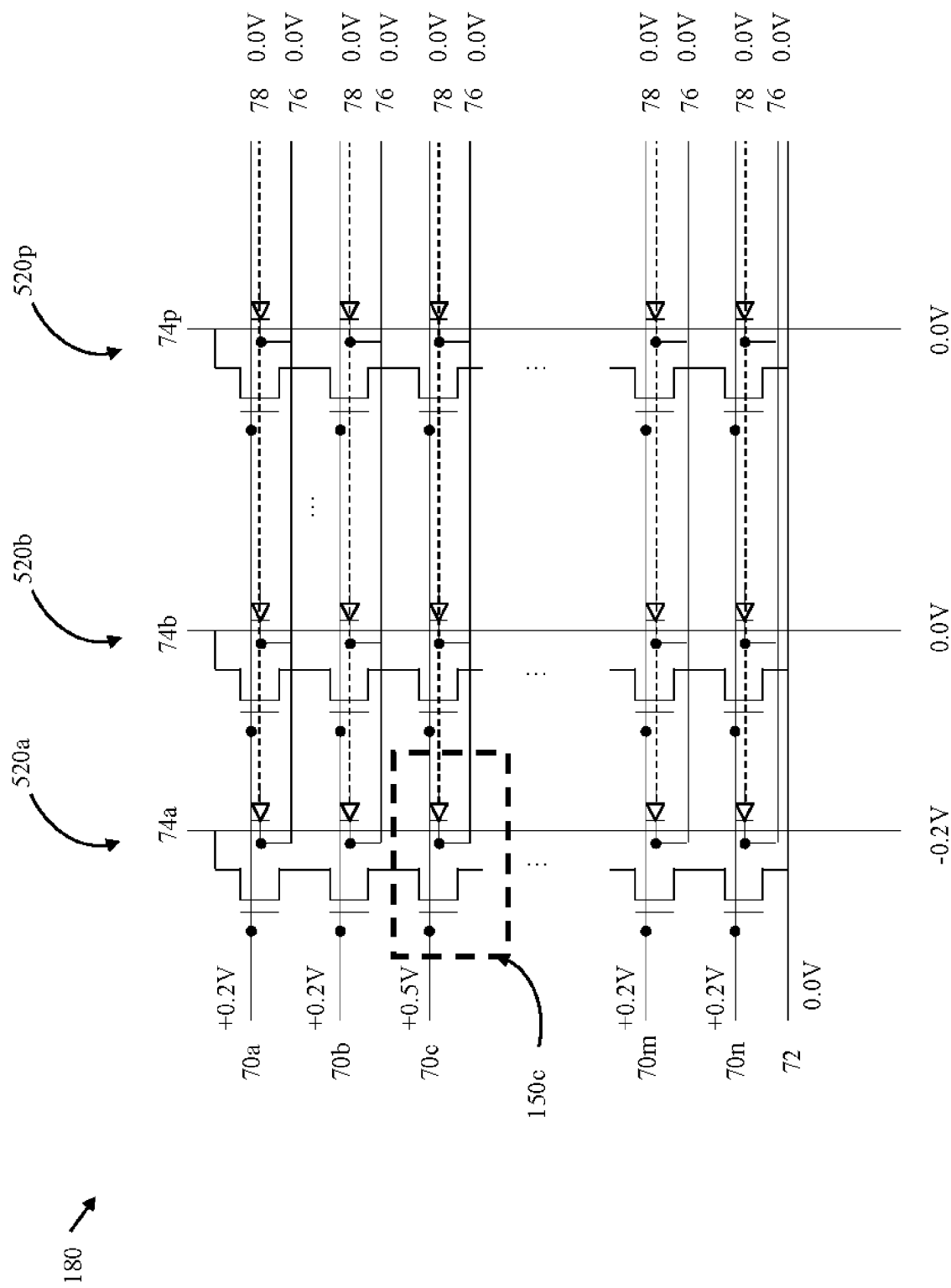
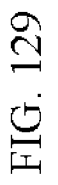


FIG. 127



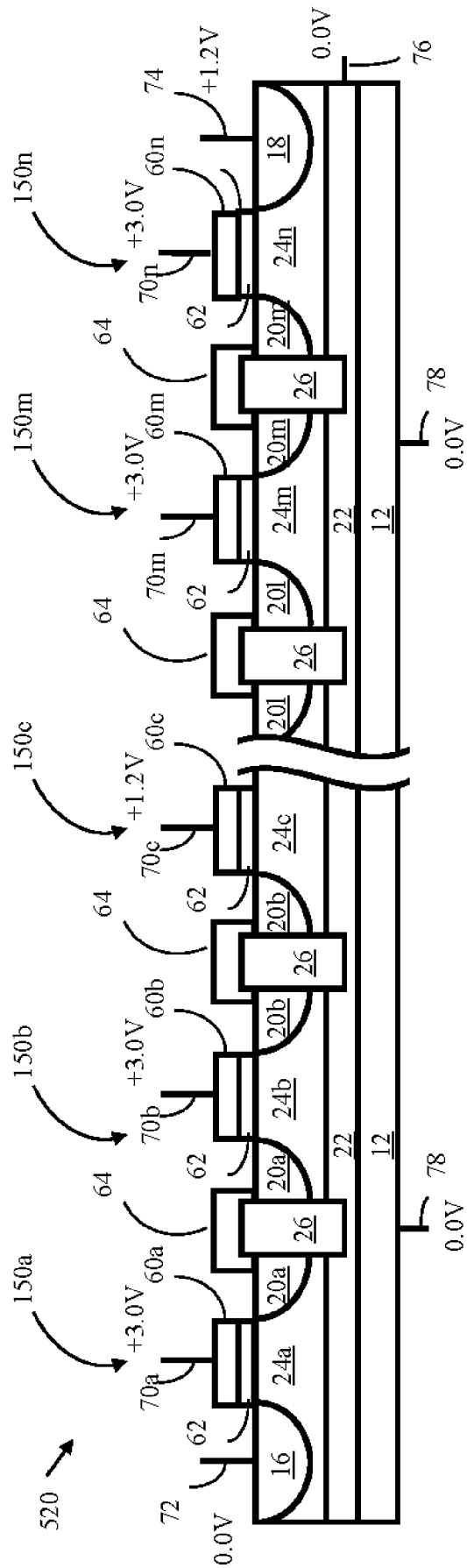


FIG. 130A

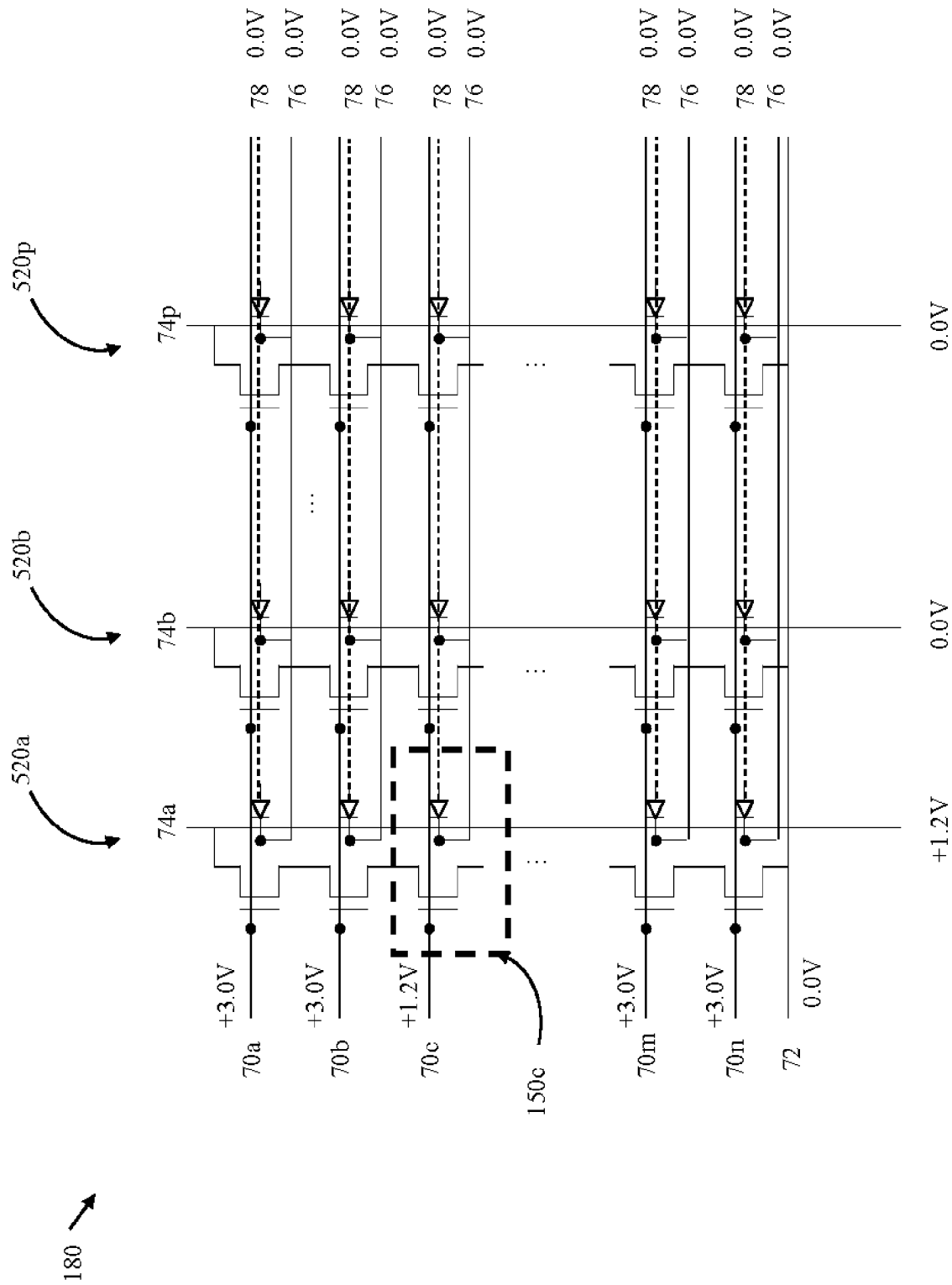


FIG. 130B

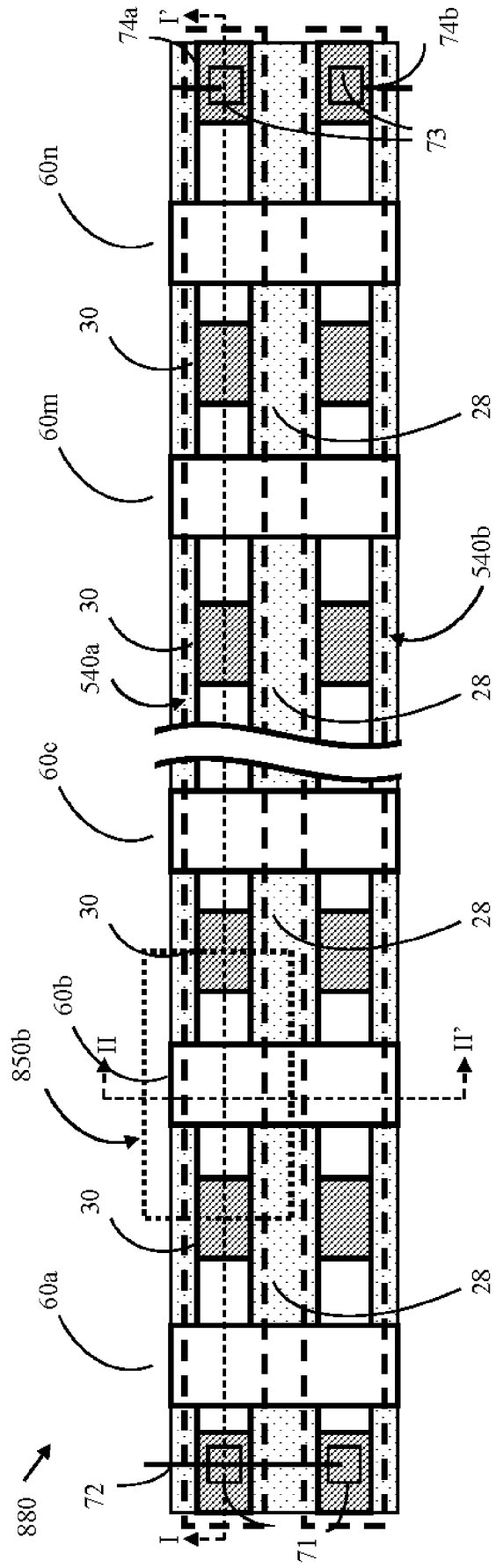


FIG. 131A

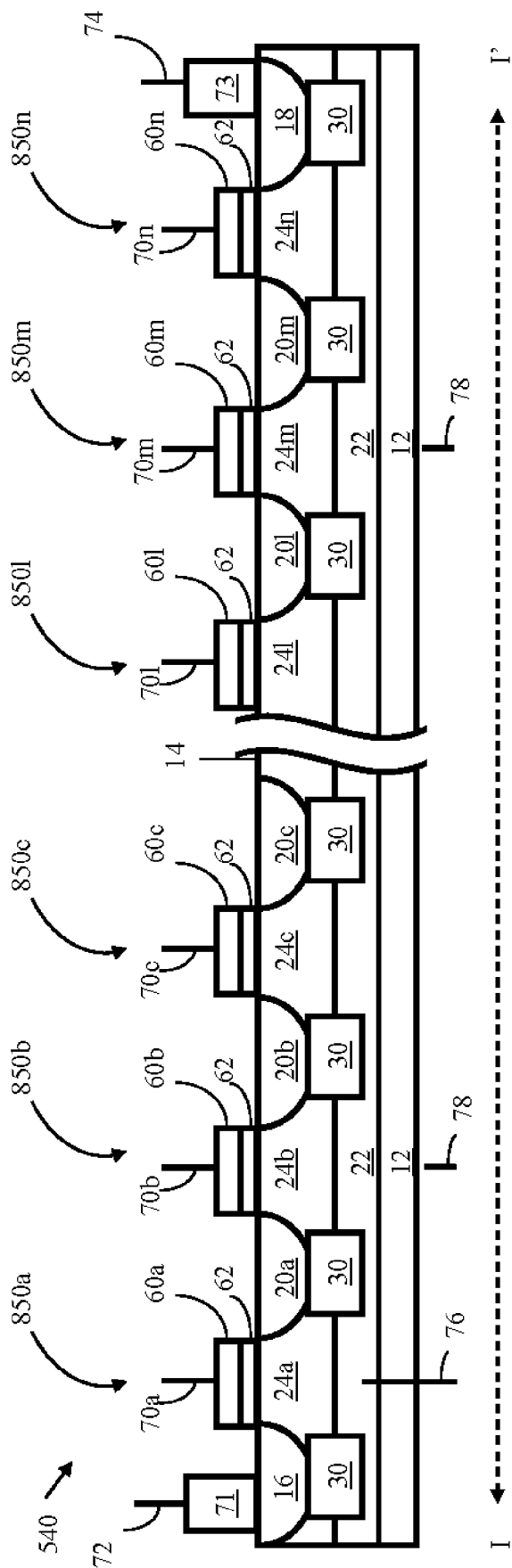


FIG. 131B

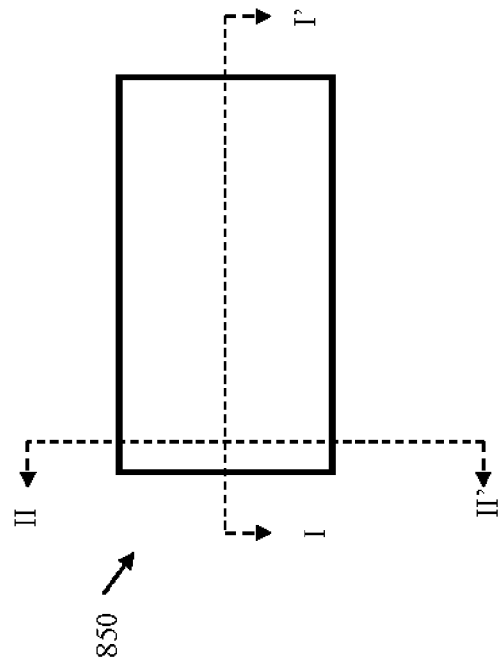


FIG. 132A

850 ↗

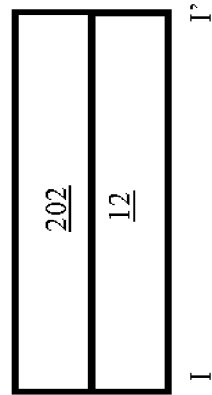


FIG. 132B

850 ↗

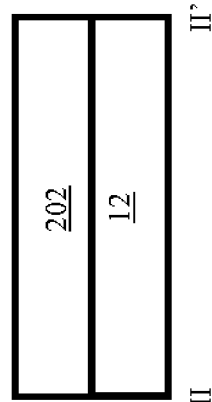


FIG. 132C

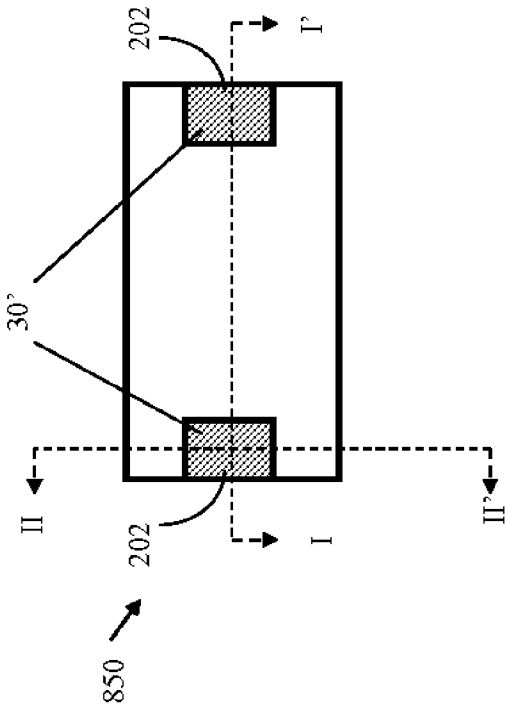


FIG. 132D

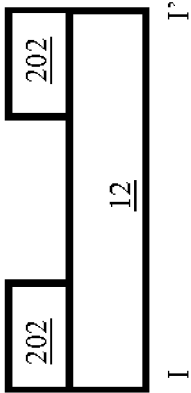


FIG. 132E

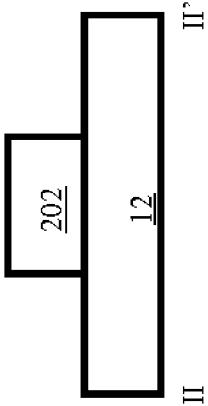


FIG. 132F

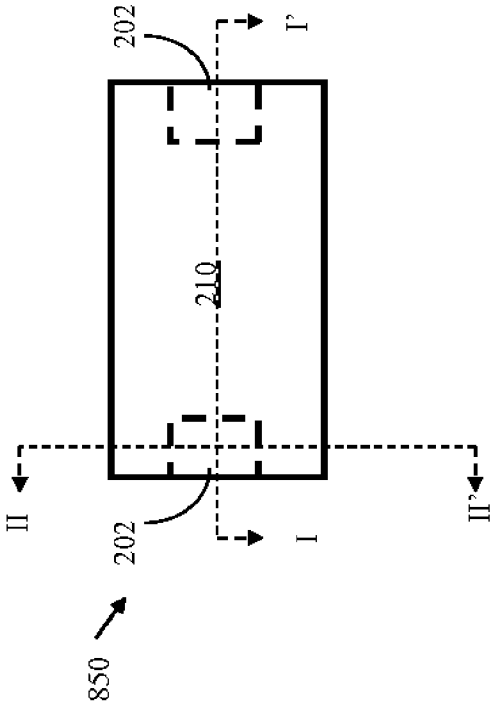


FIG. 132G

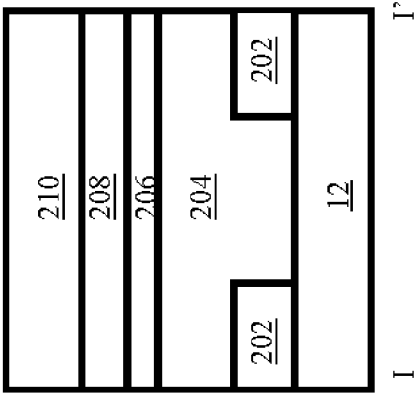


FIG. 132H

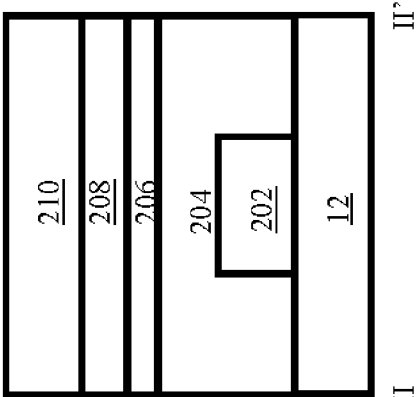


FIG. 132I

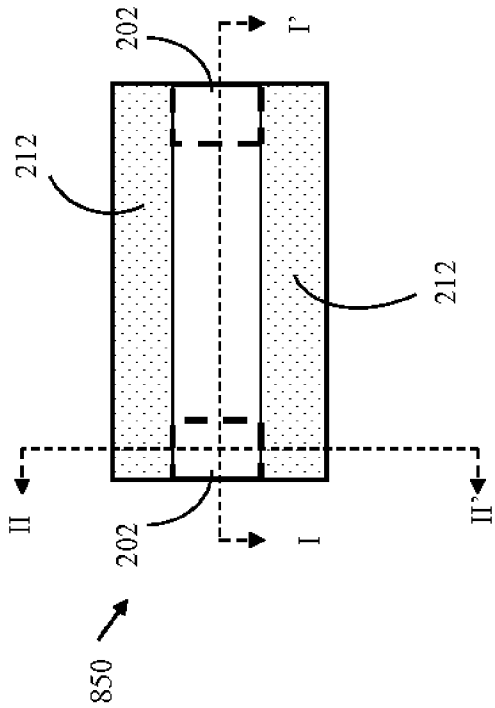


FIG. 132J

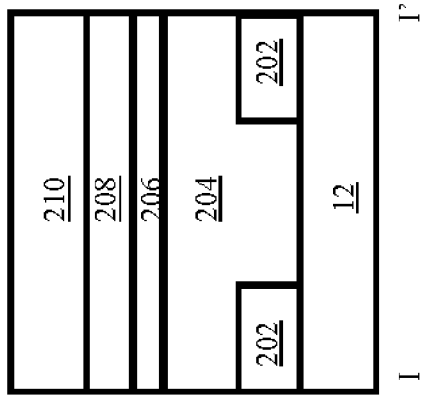


FIG. 132K

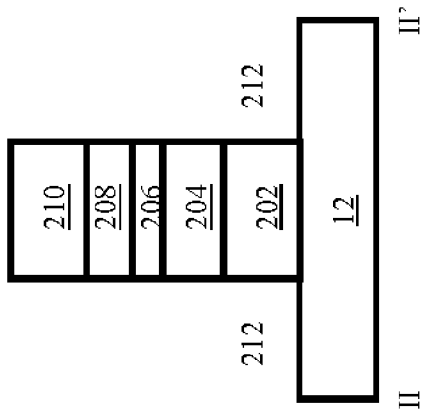
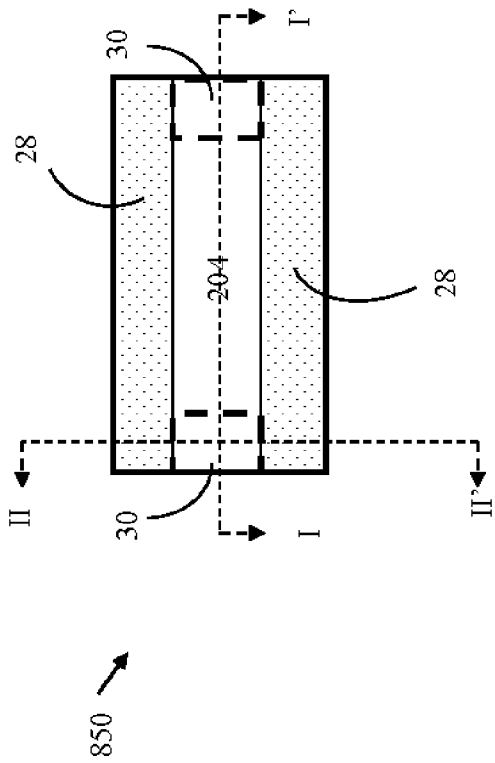
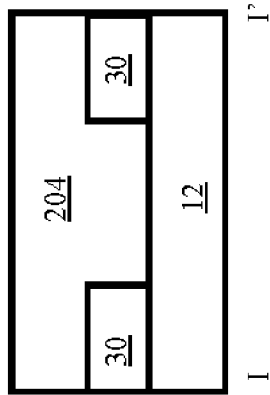


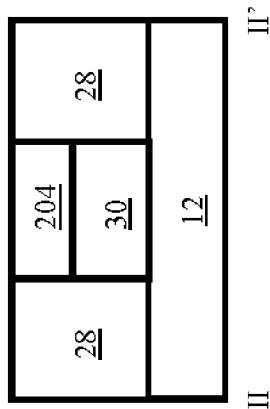
FIG. 132L



850 ↗



850 ↗



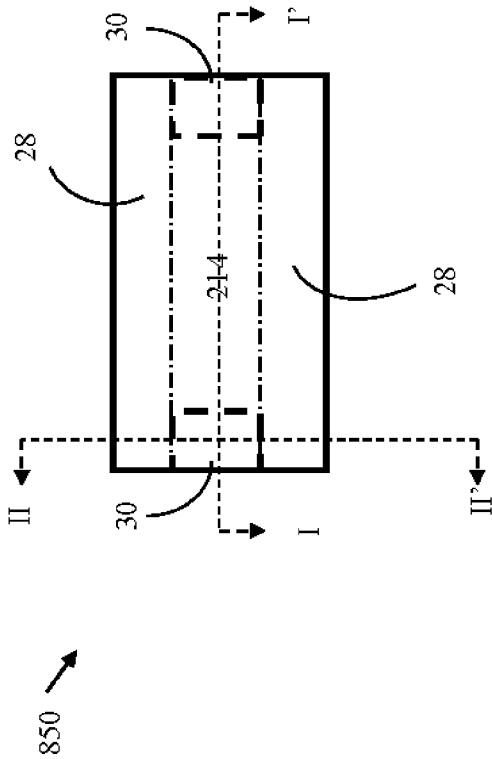


FIG. 132P

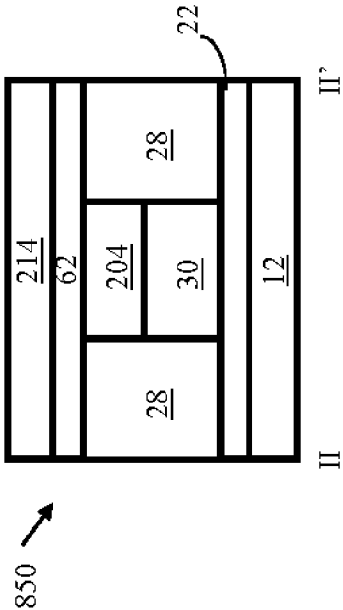


FIG. 132R

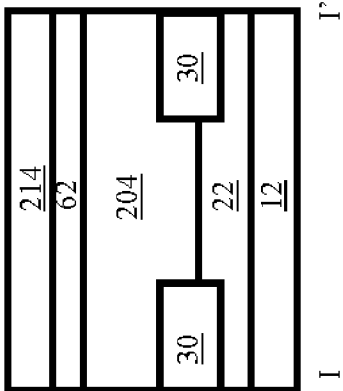


FIG. 132Q

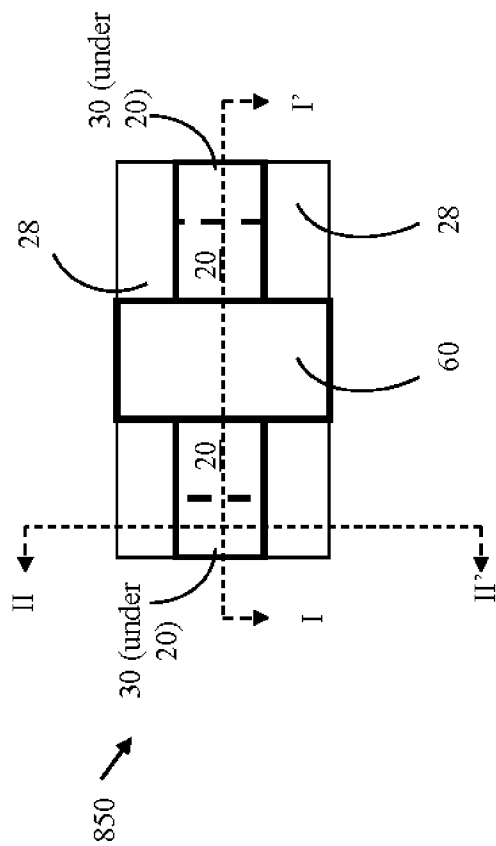


FIG. 132S

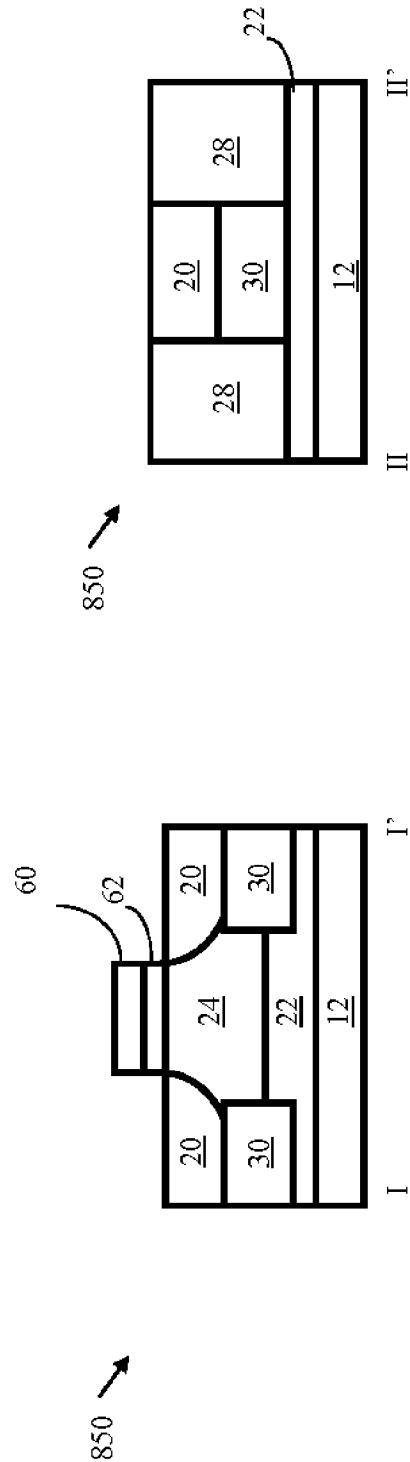


FIG. 132U

FIG. 132T

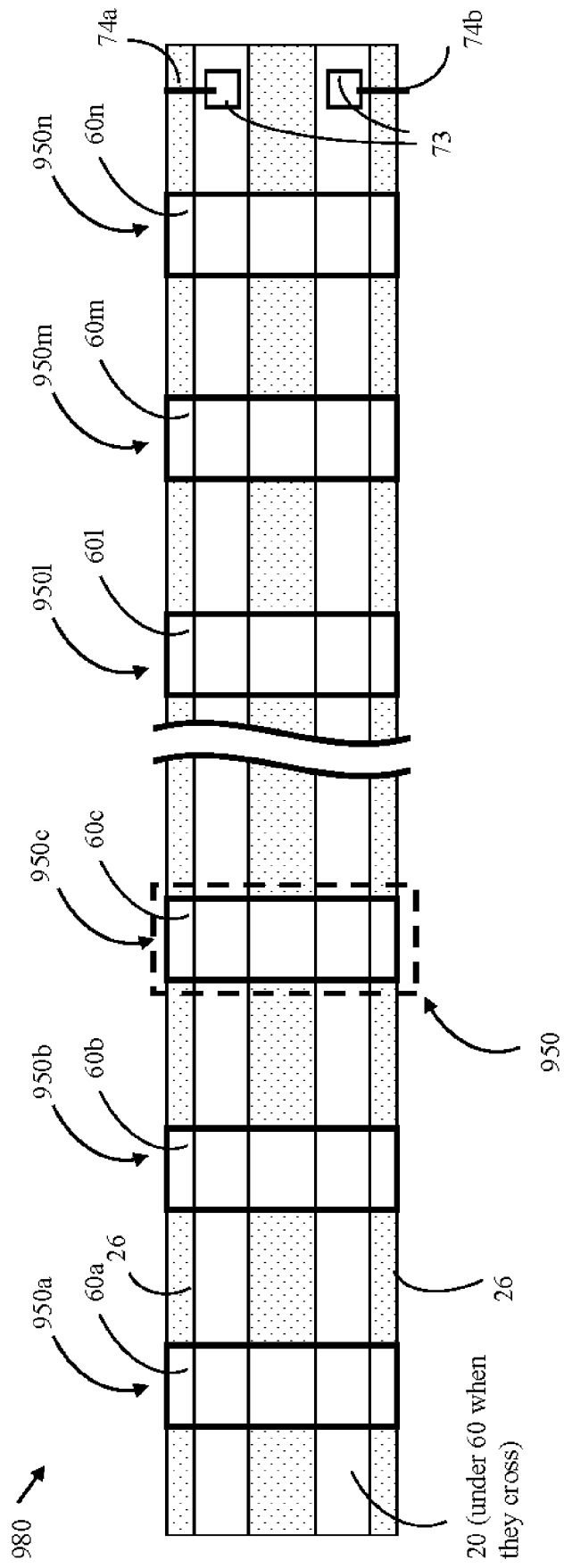
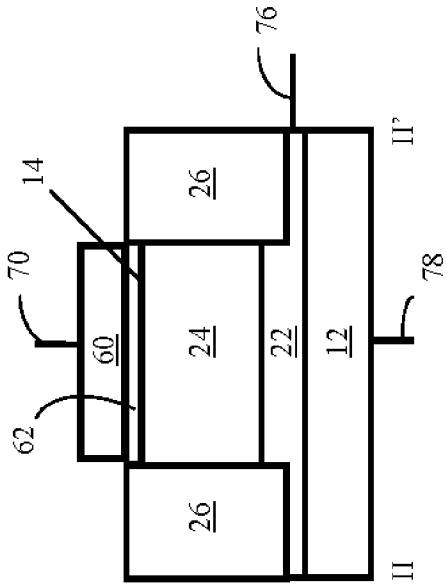
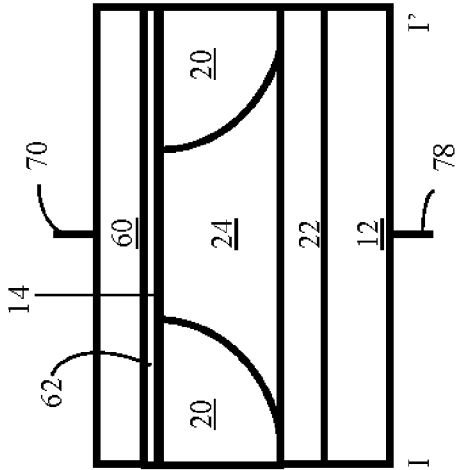
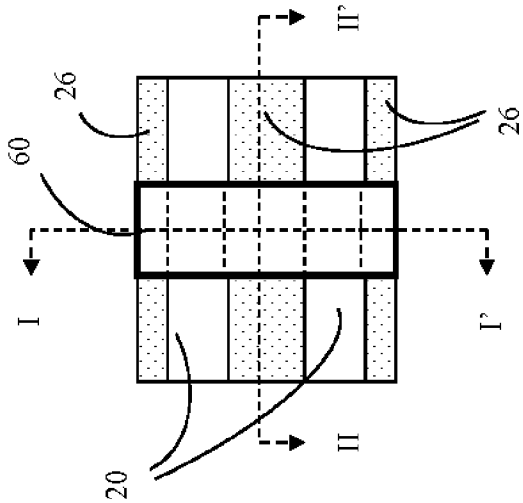


FIG. 133



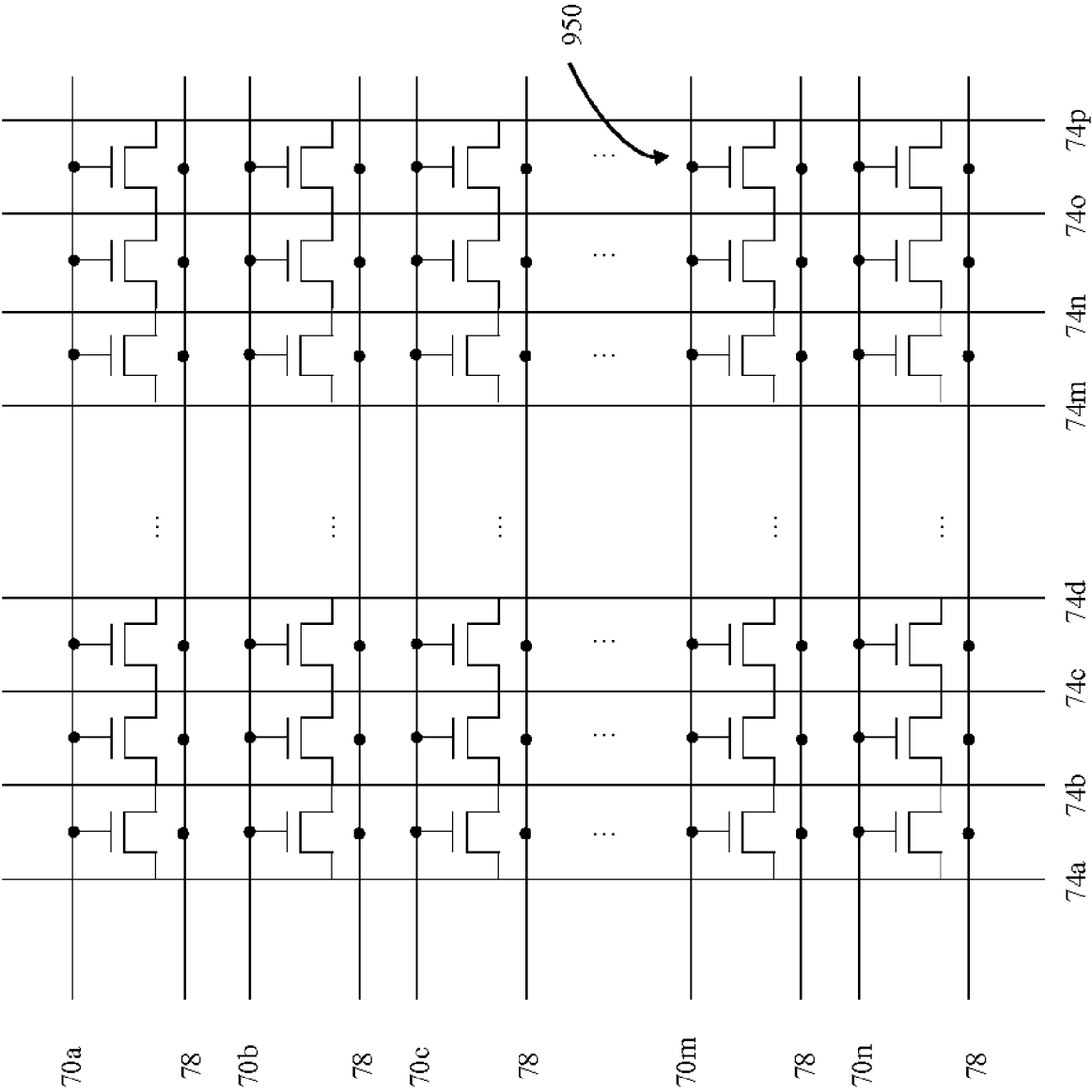


FIG. 135

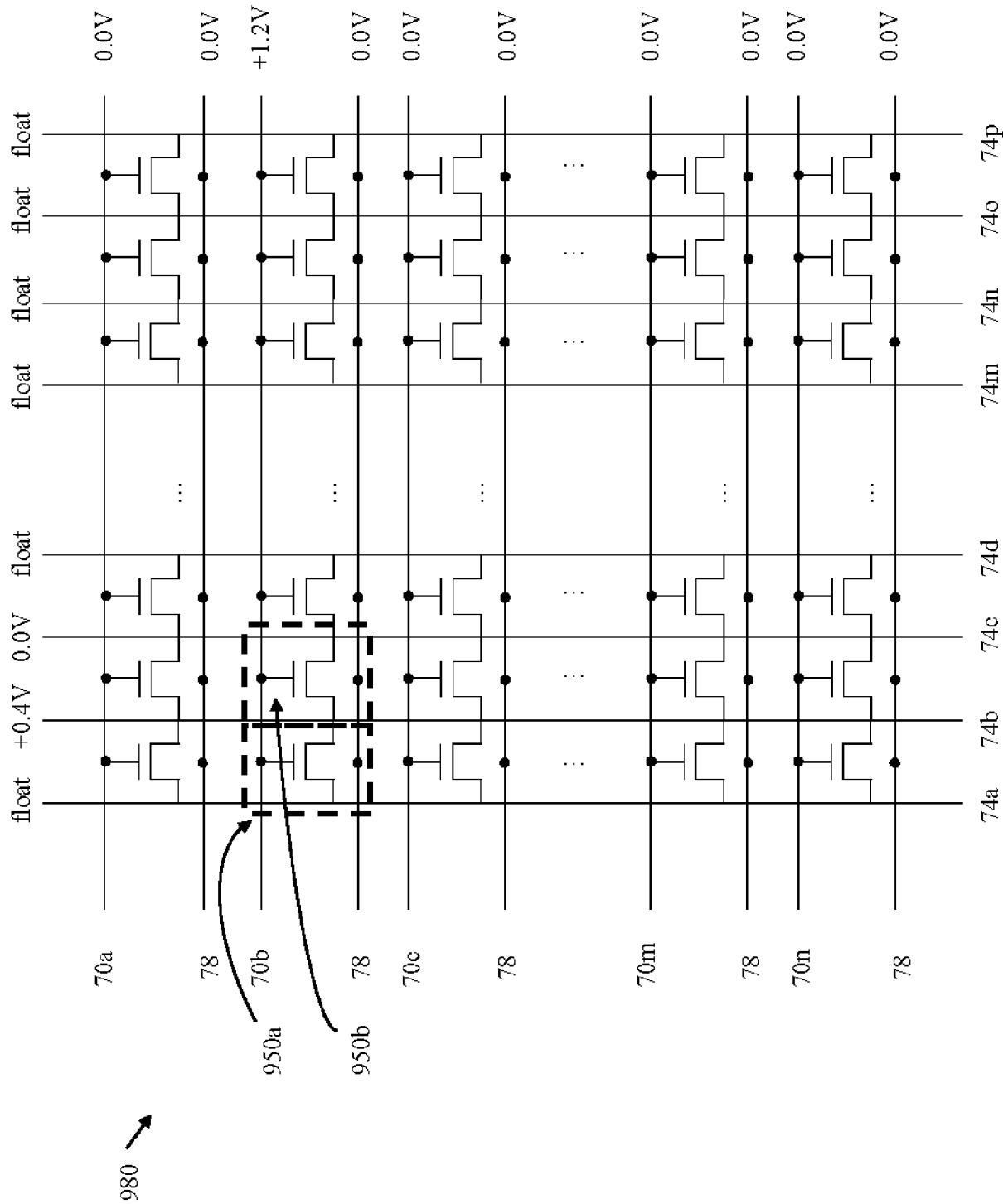


FIG. 136

950b →

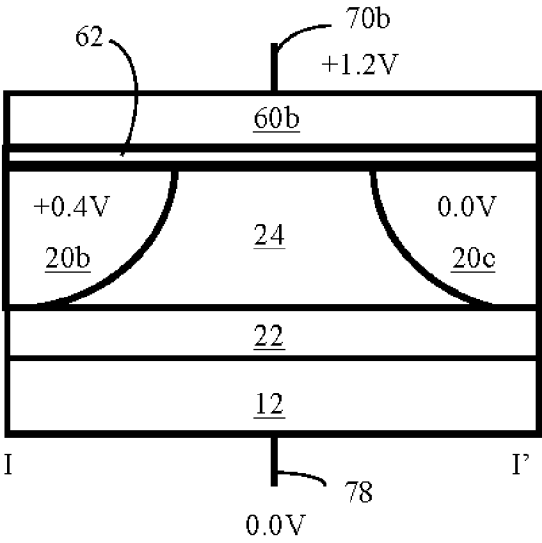


FIG. 137

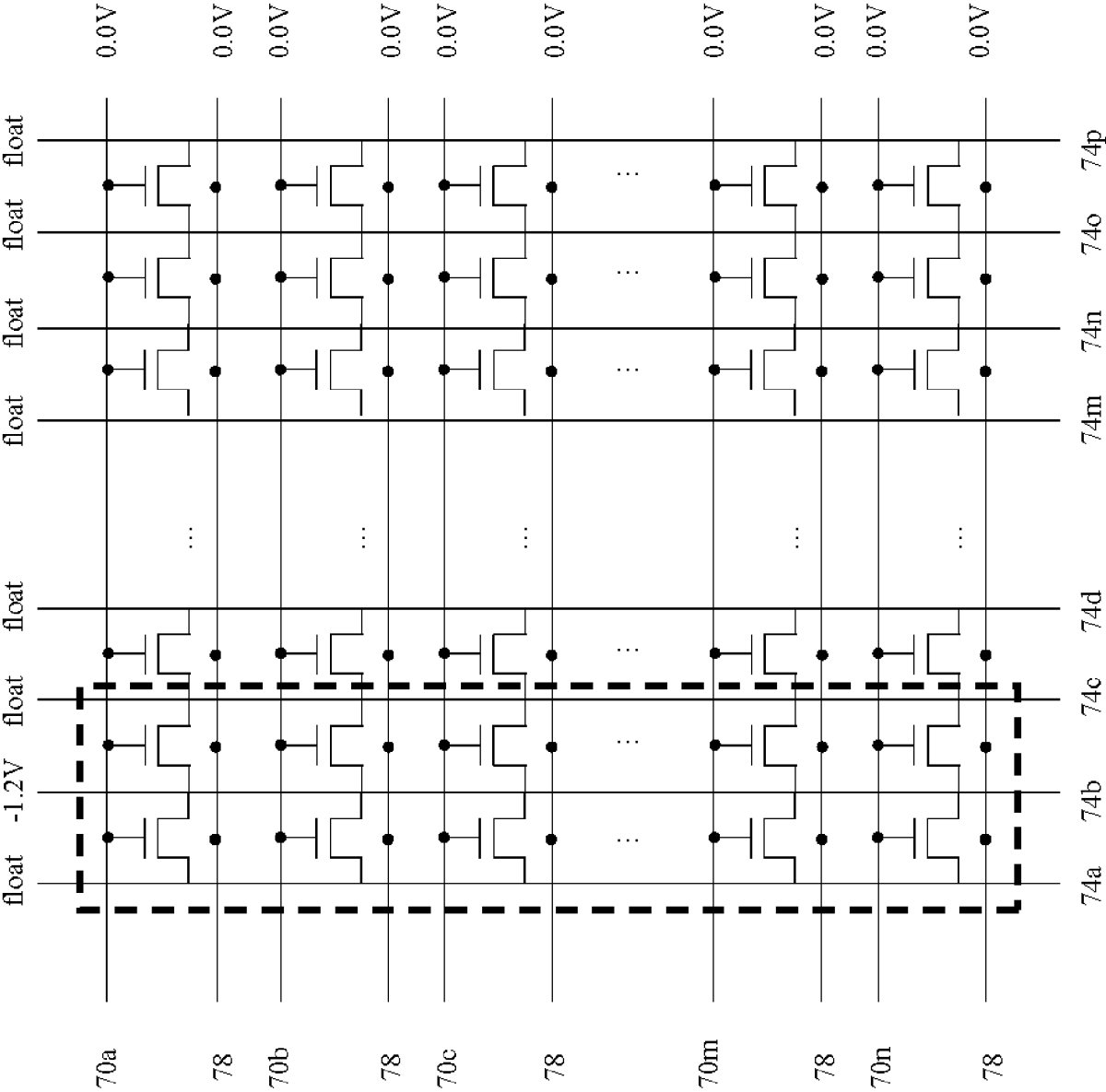


FIG. 138

980 ↗

950b →

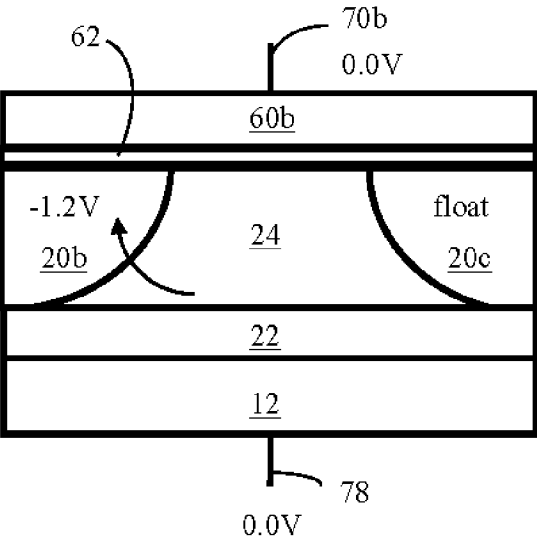


FIG. 139

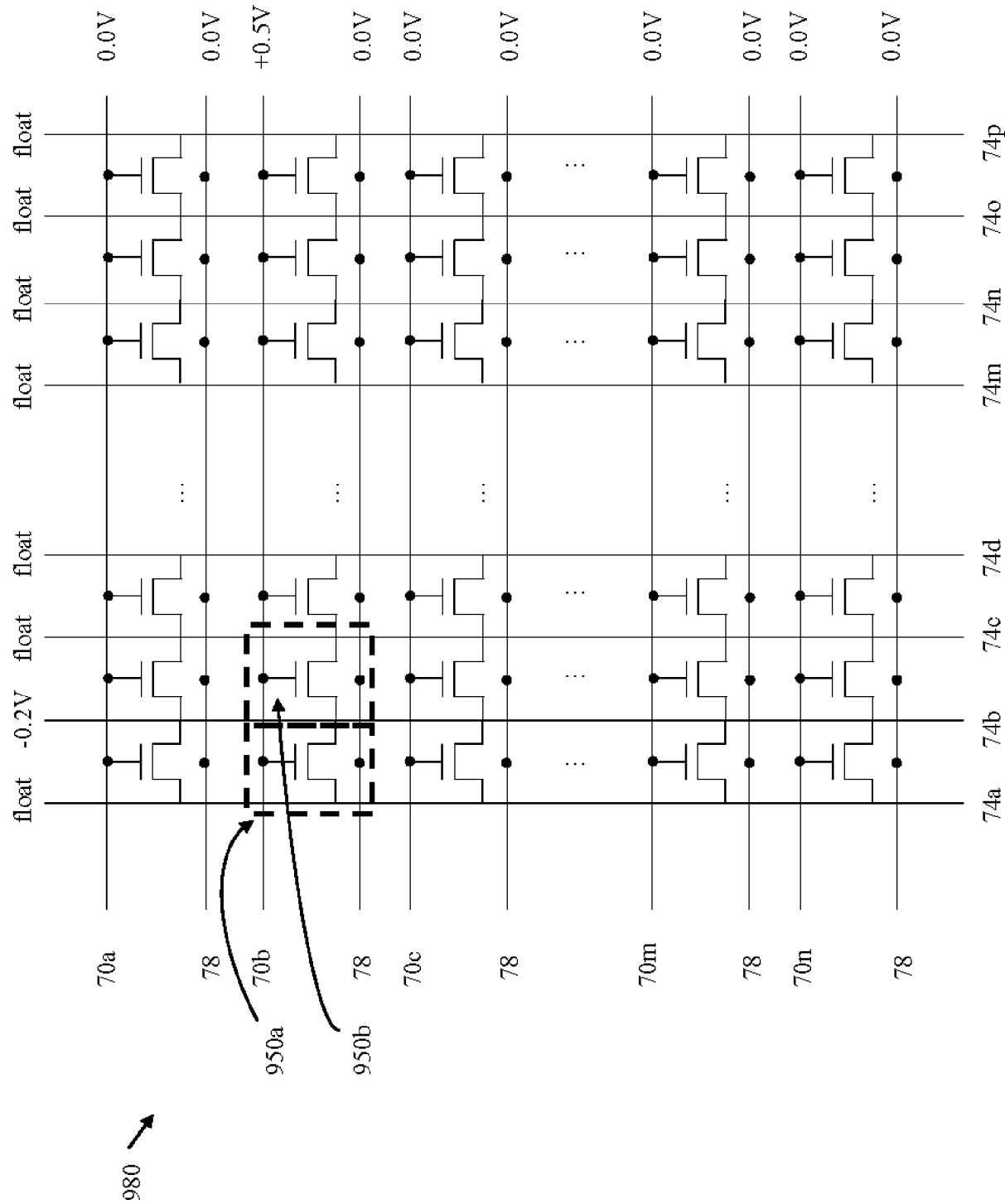


FIG. 140

950b →

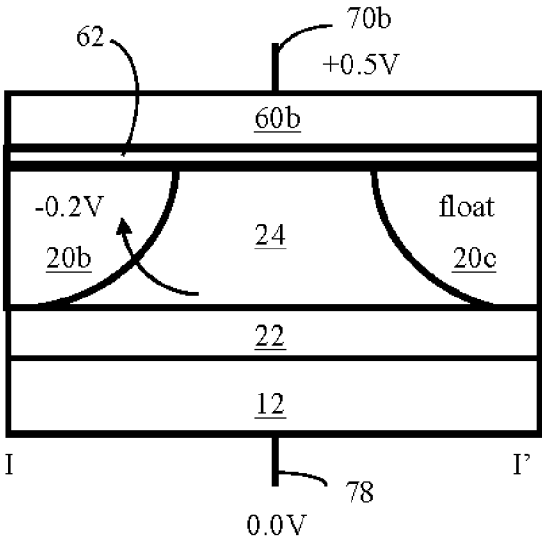


FIG. 141

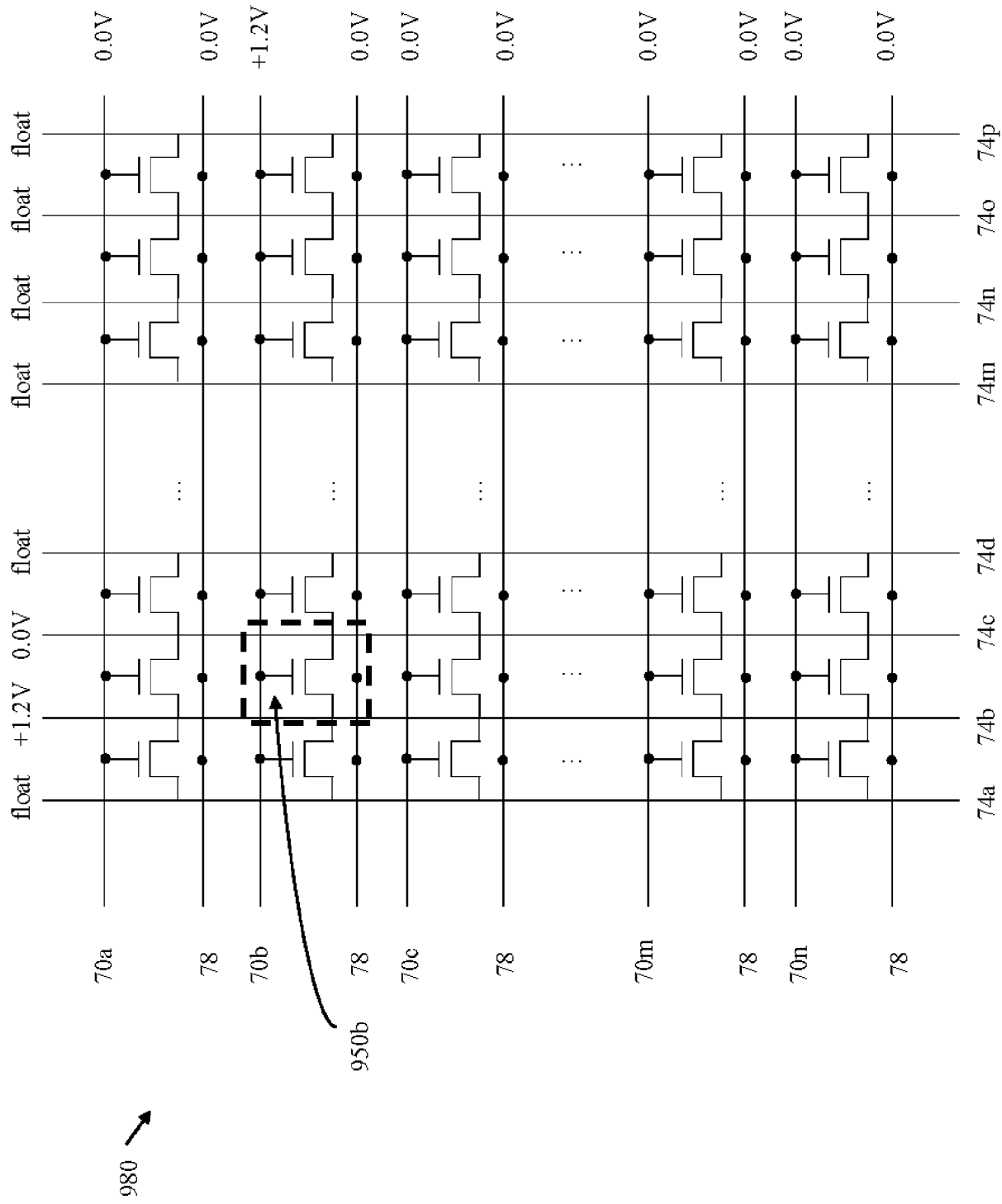


FIG. 142

950b →

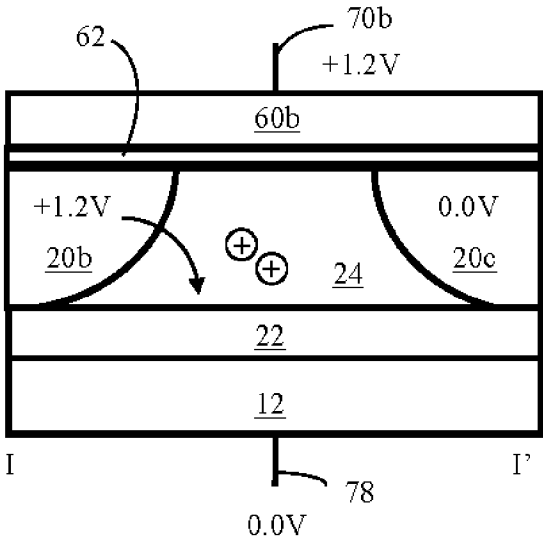


FIG. 143

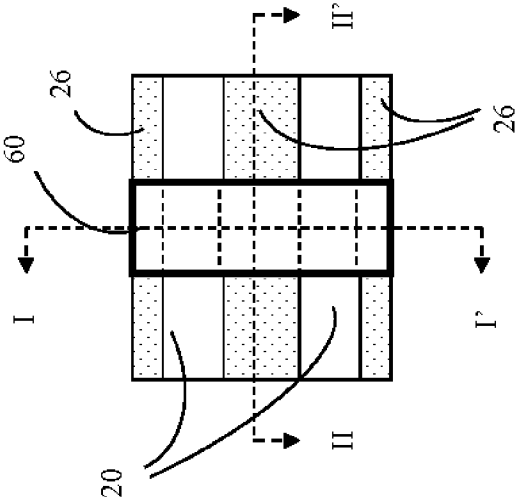


FIG. 145A

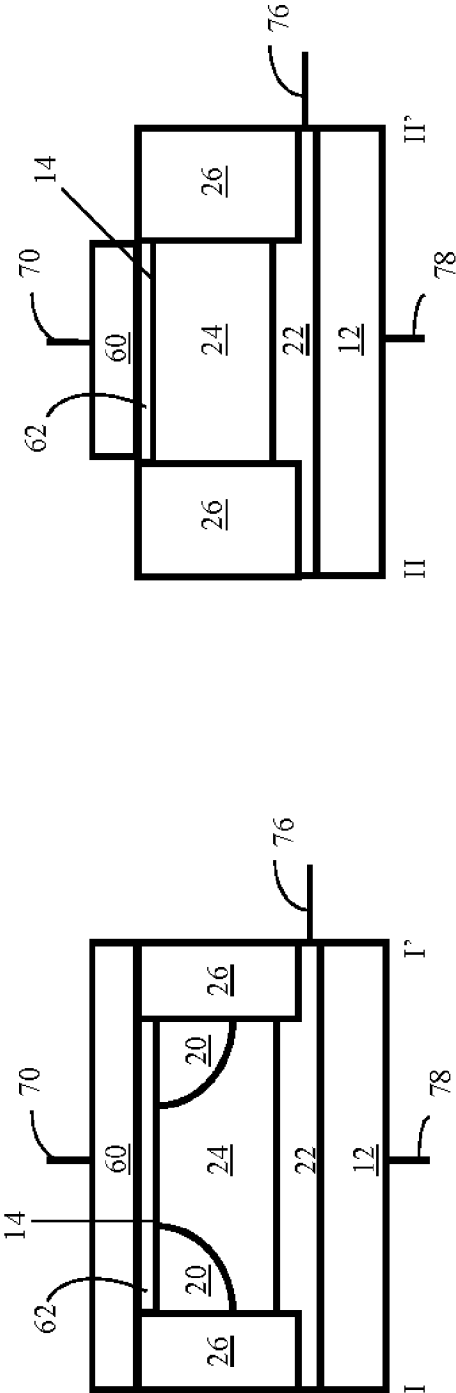


FIG. 145C

FIG. 145B

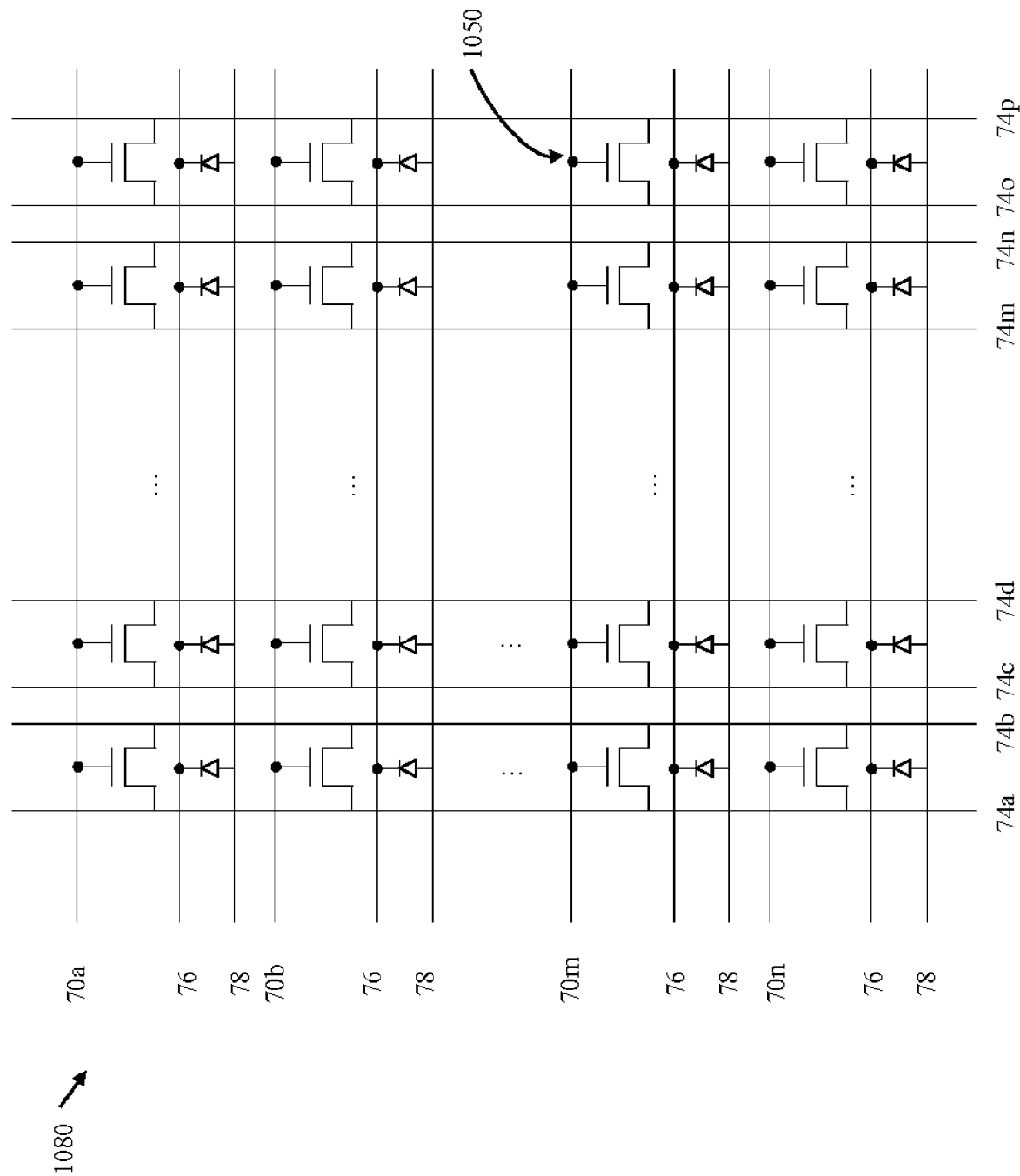


FIG. 146

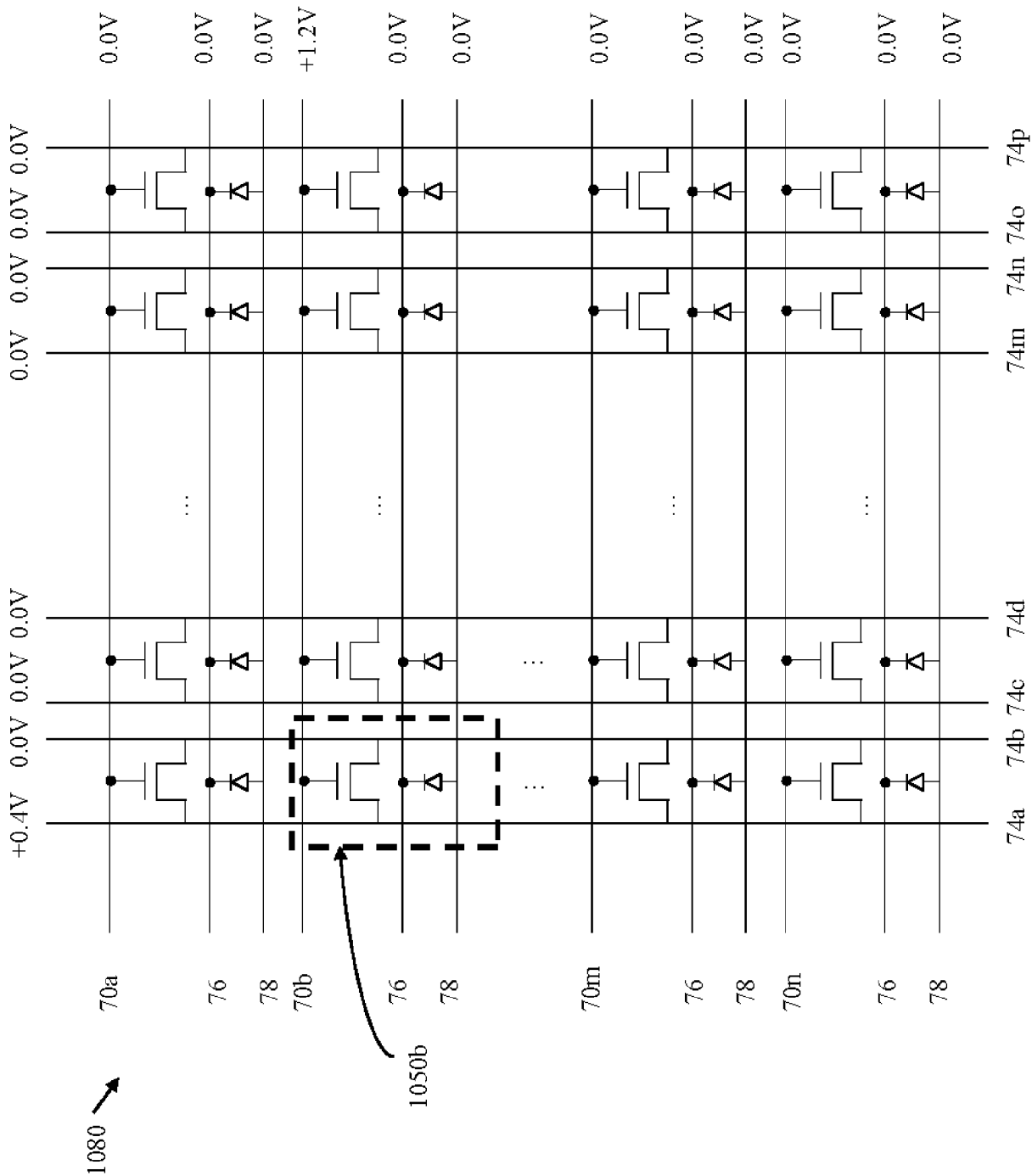


FIG. 147

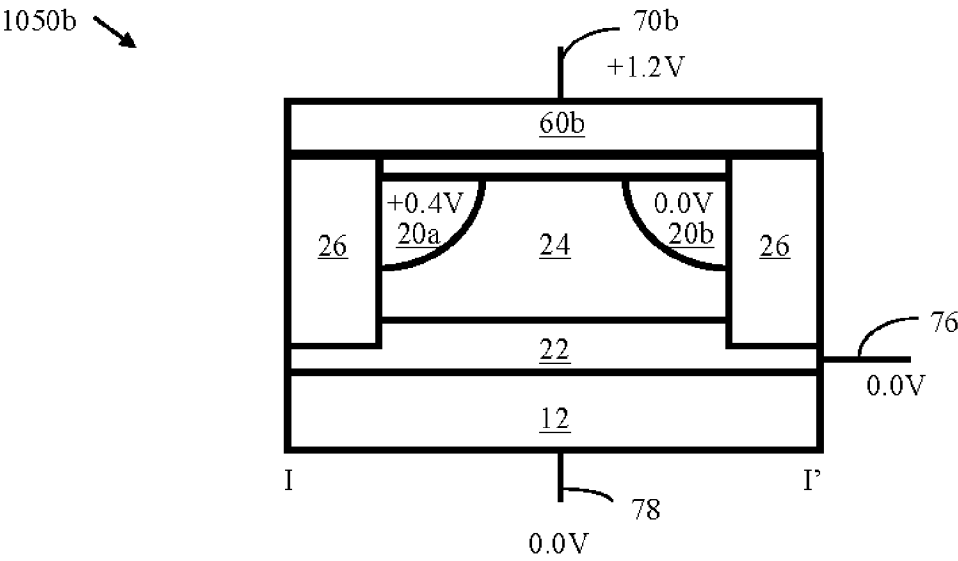


FIG. 148

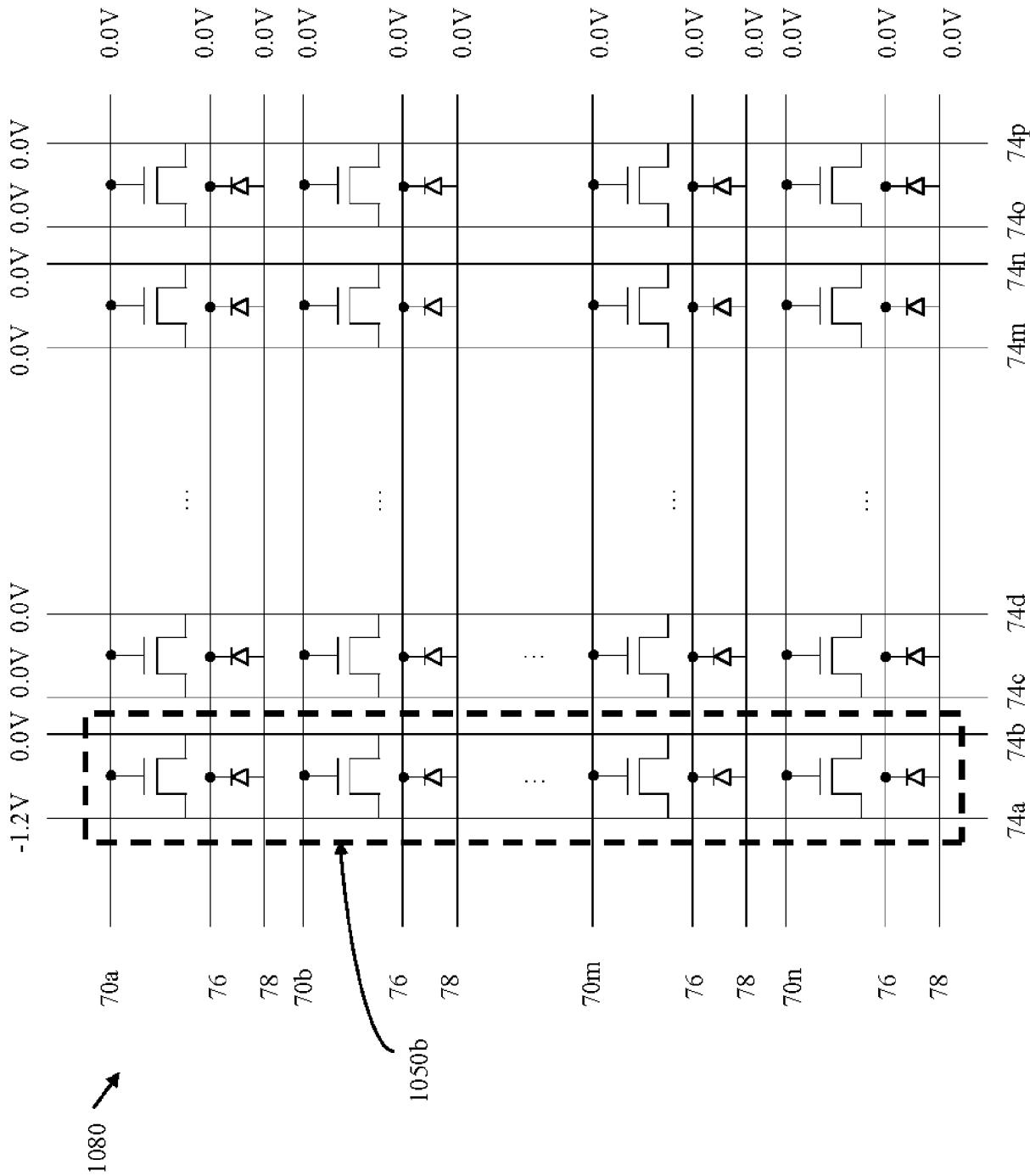


FIG. 149

1050b →

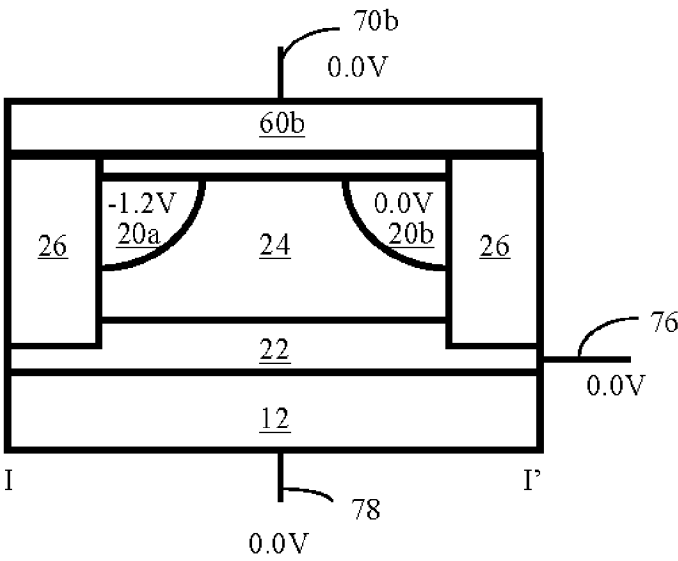


FIG. 150

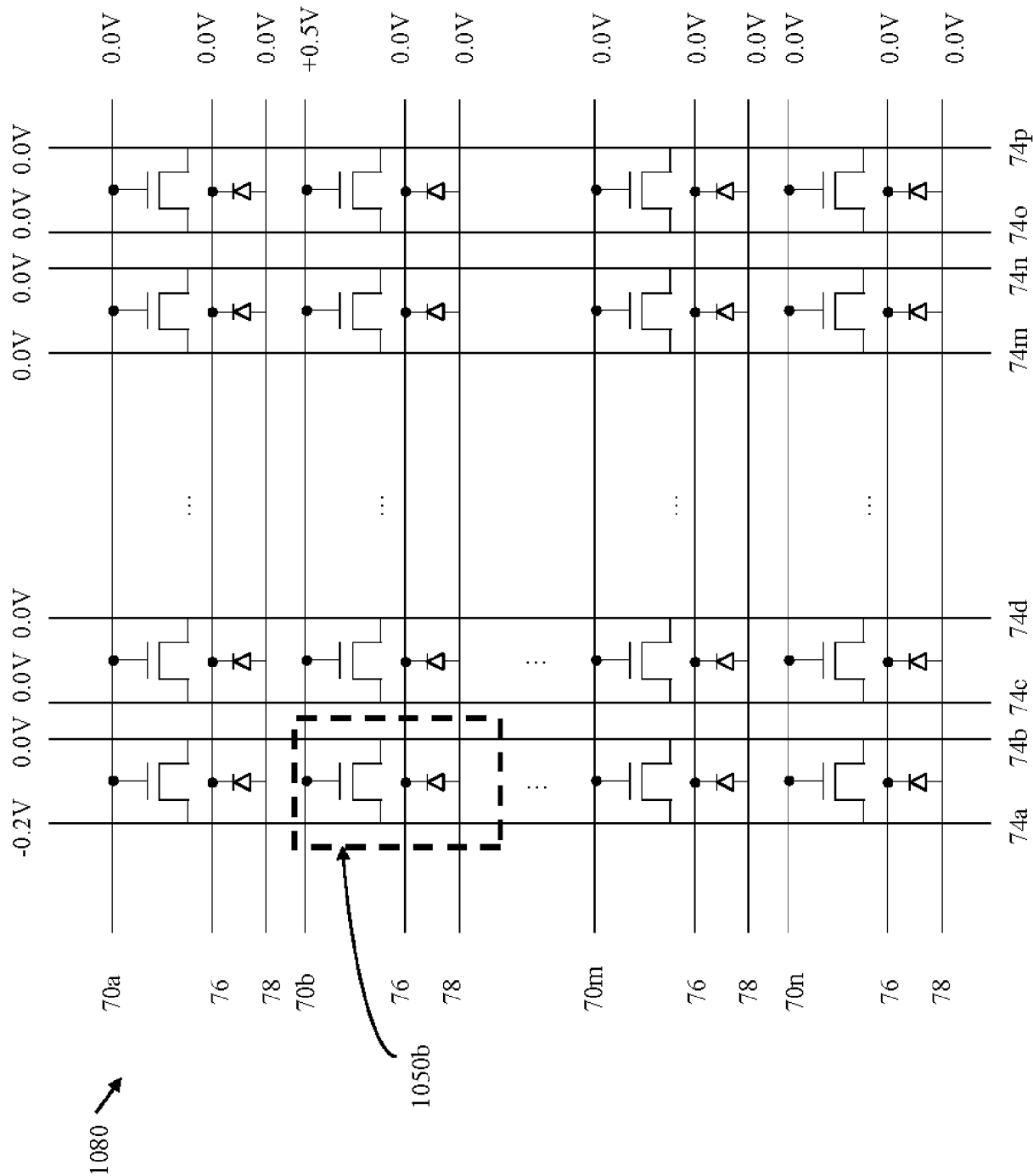


FIG. 151

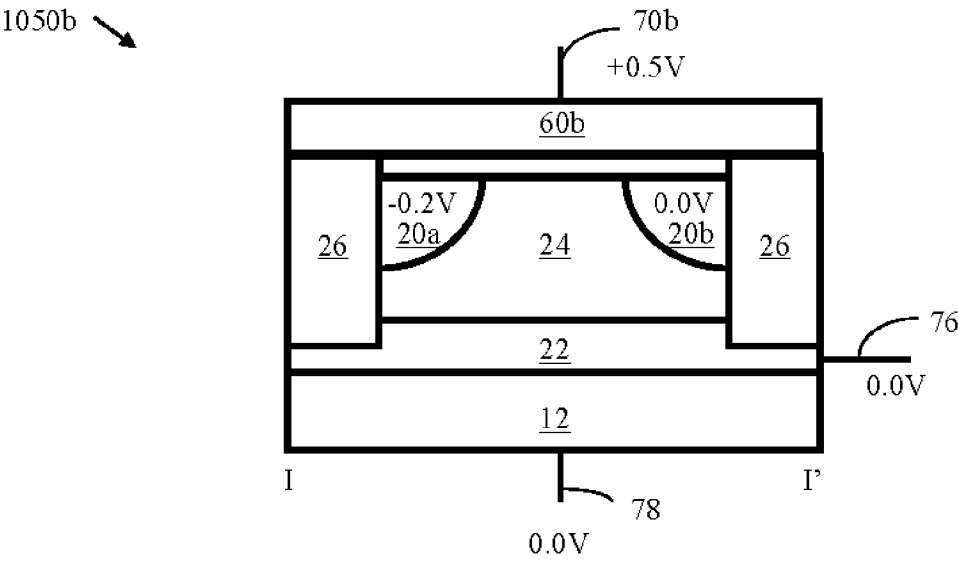


FIG. 152

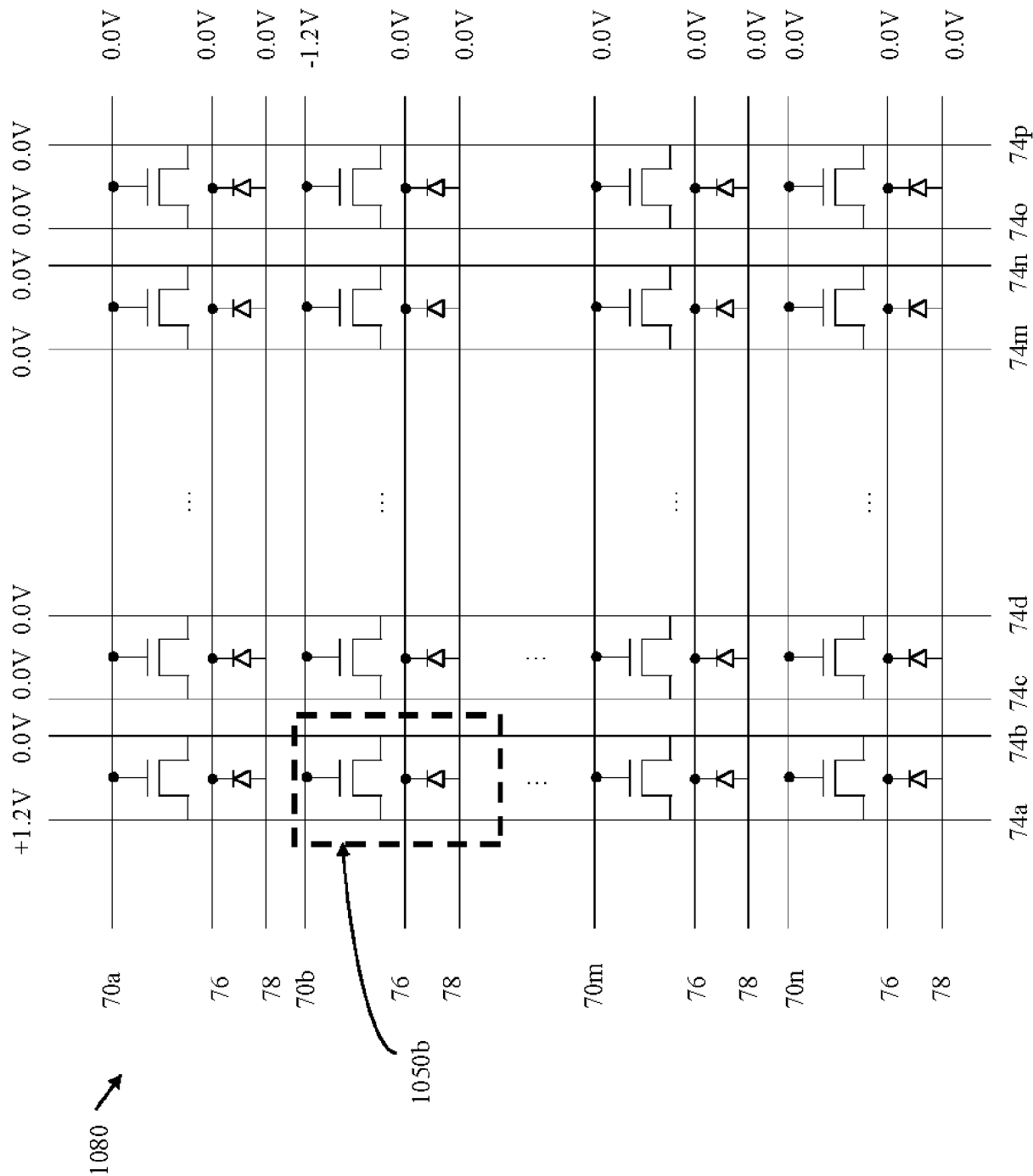


FIG. 153

1050b →

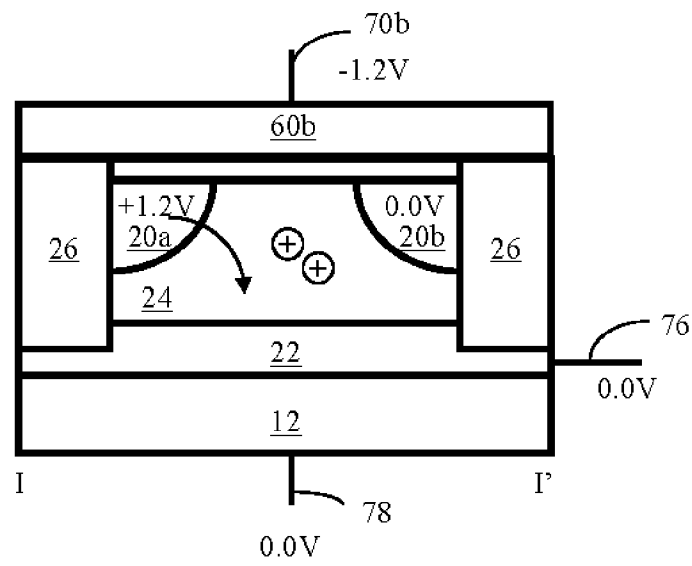


FIG. 154

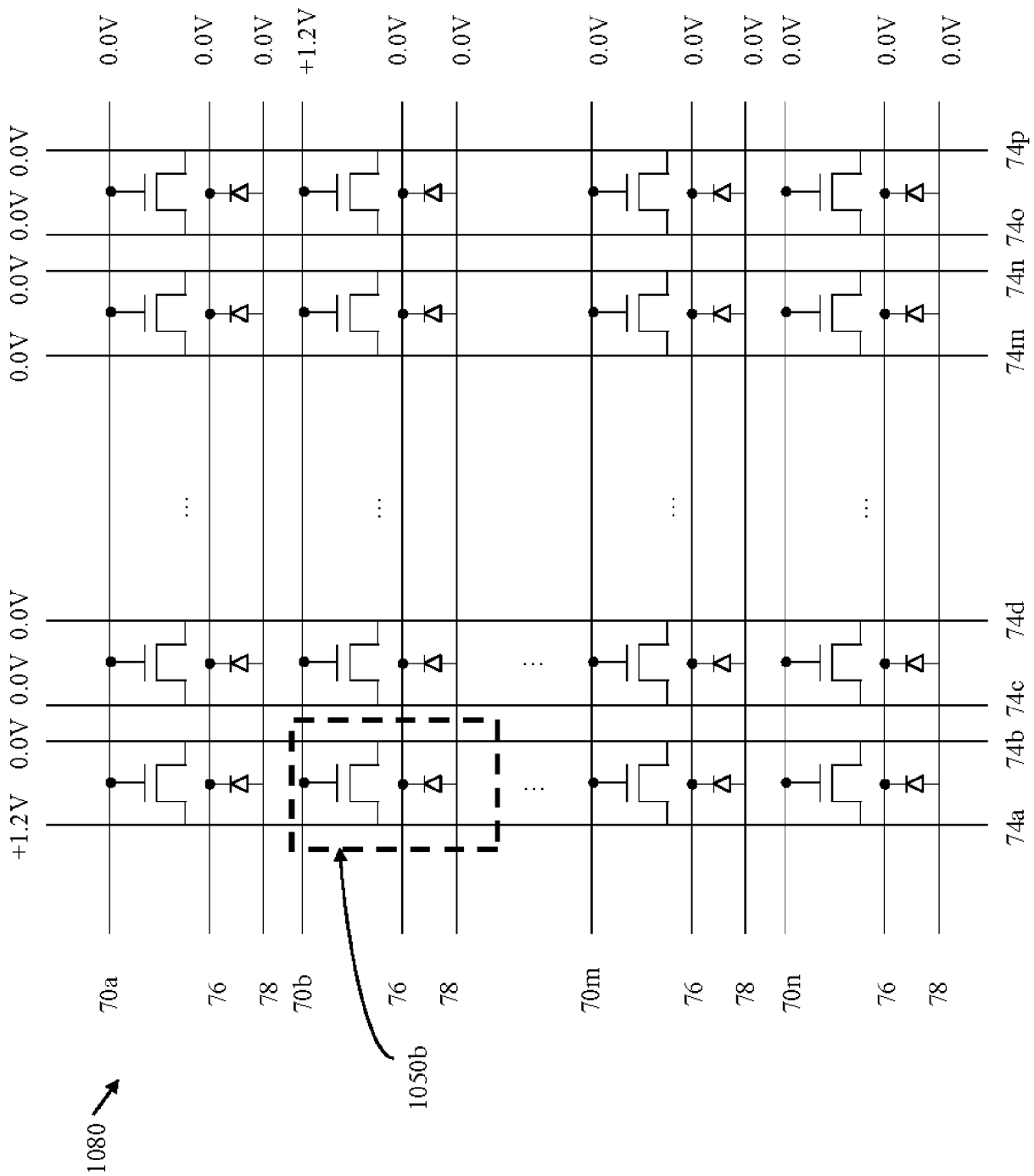


FIG. 155

1050b →

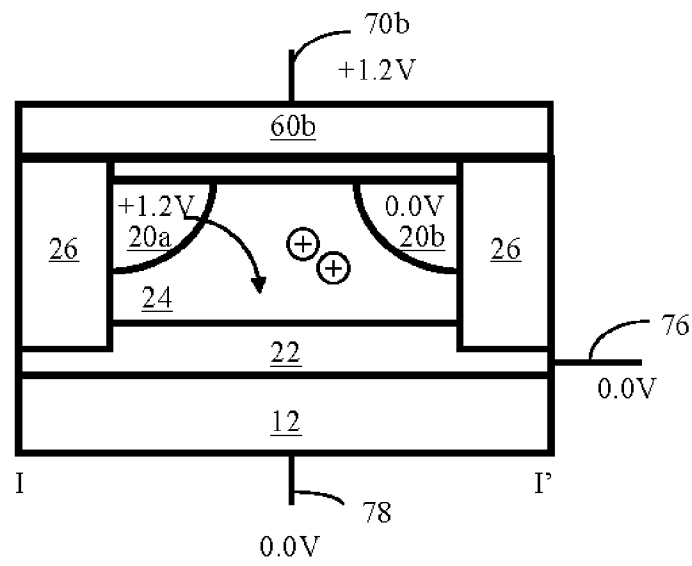


FIG. 156

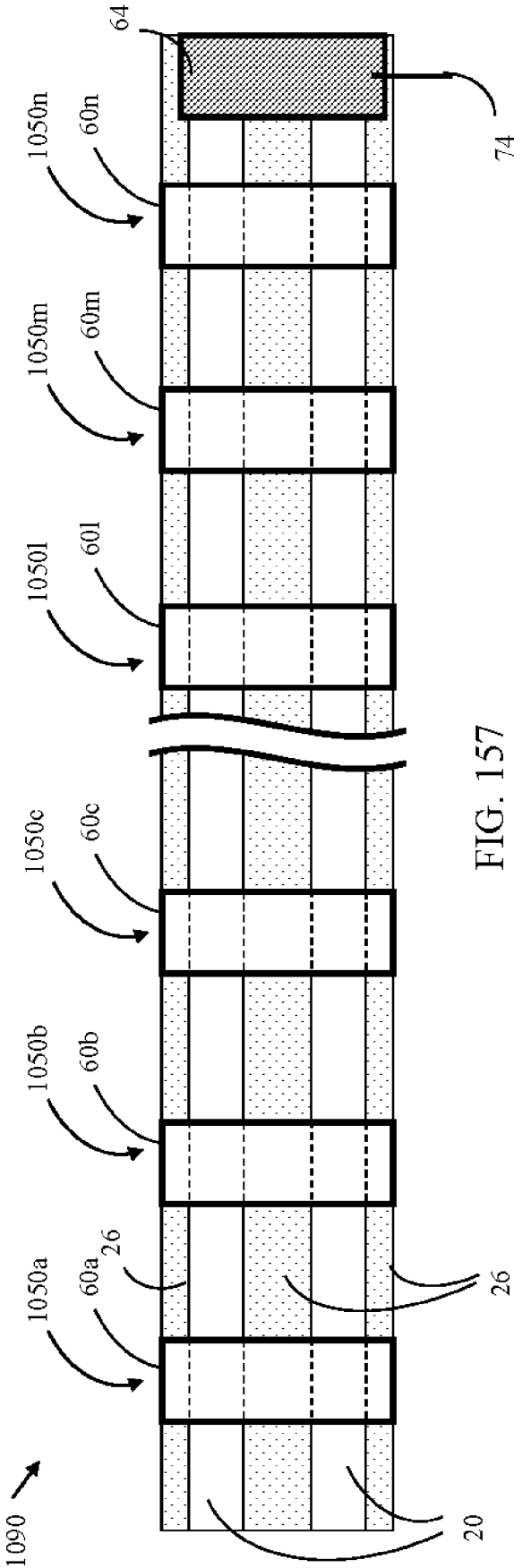


FIG. 157

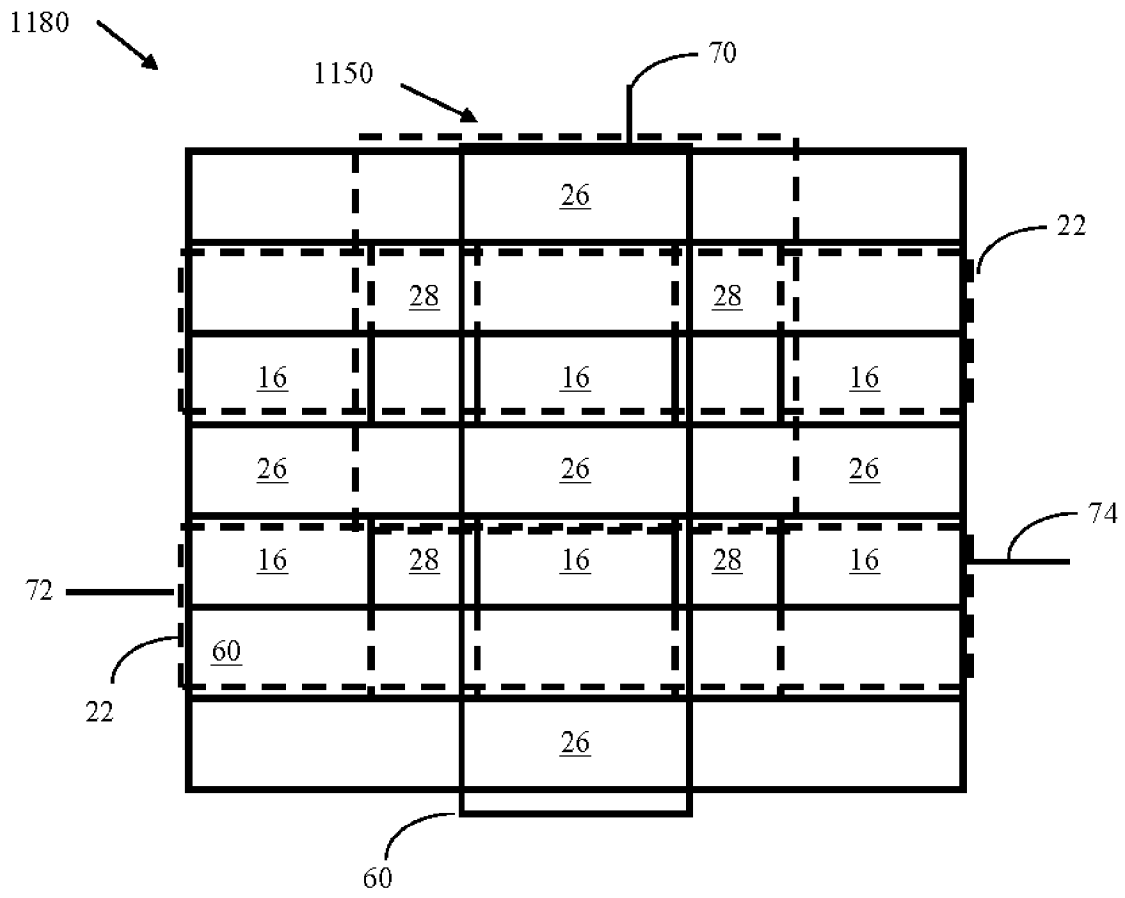


FIG. 158A

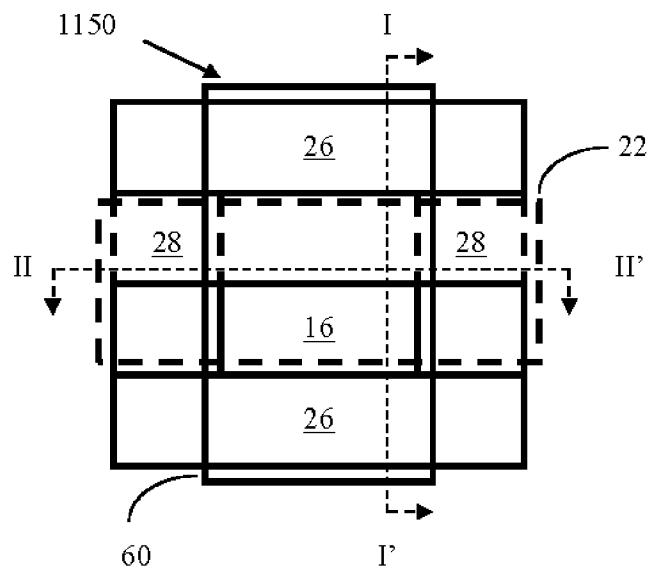


FIG. 158B

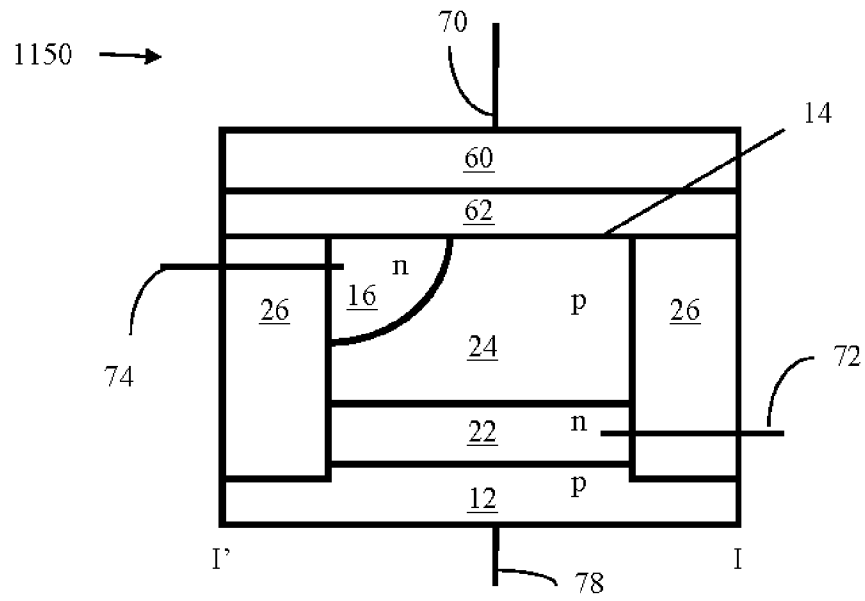


FIG. 158C

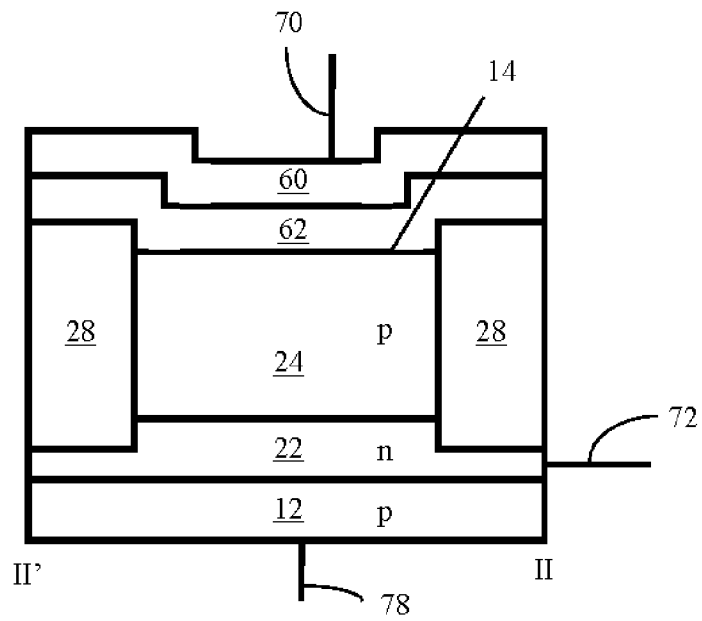


FIG. 158D

1180

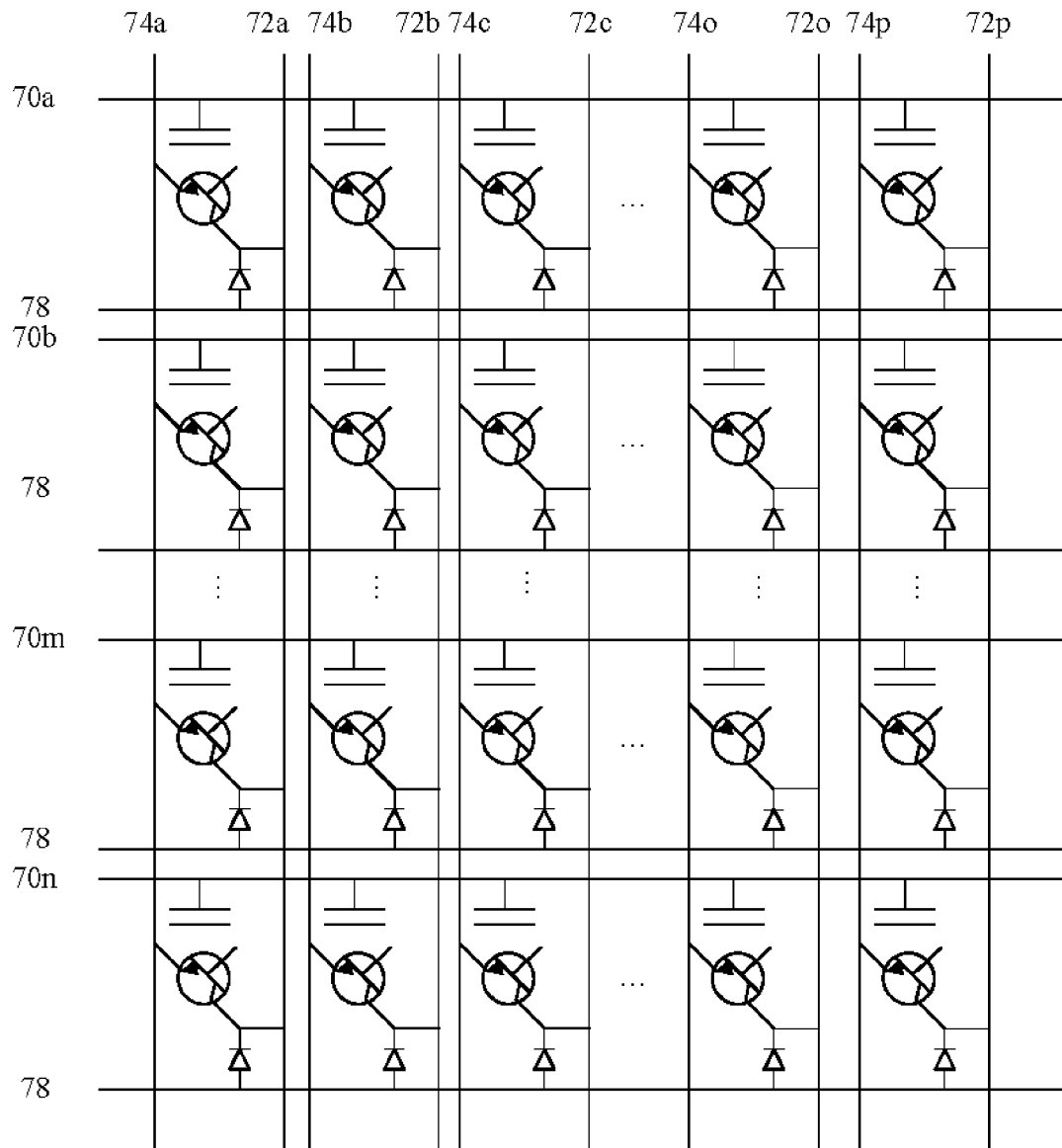


FIG. 159

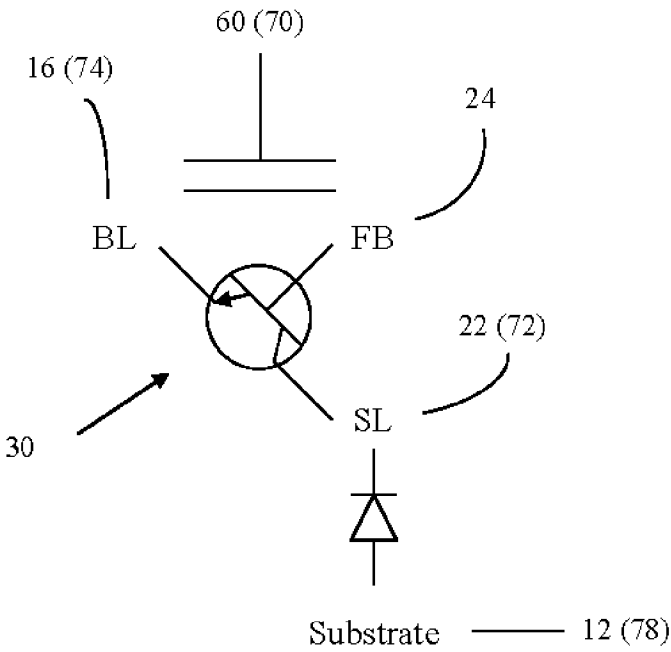


FIG. 160A

Floating Body 24 is positively charged

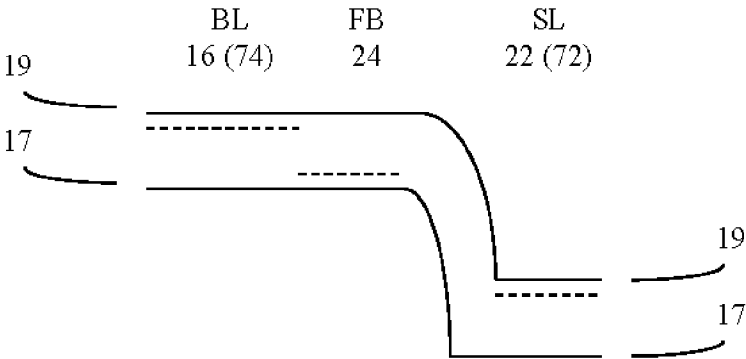


FIG. 160B

FB is neutrally charged: $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

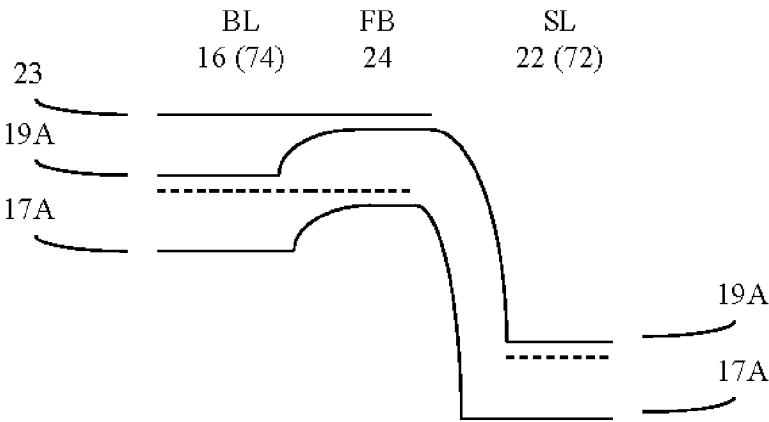


FIG. 160C

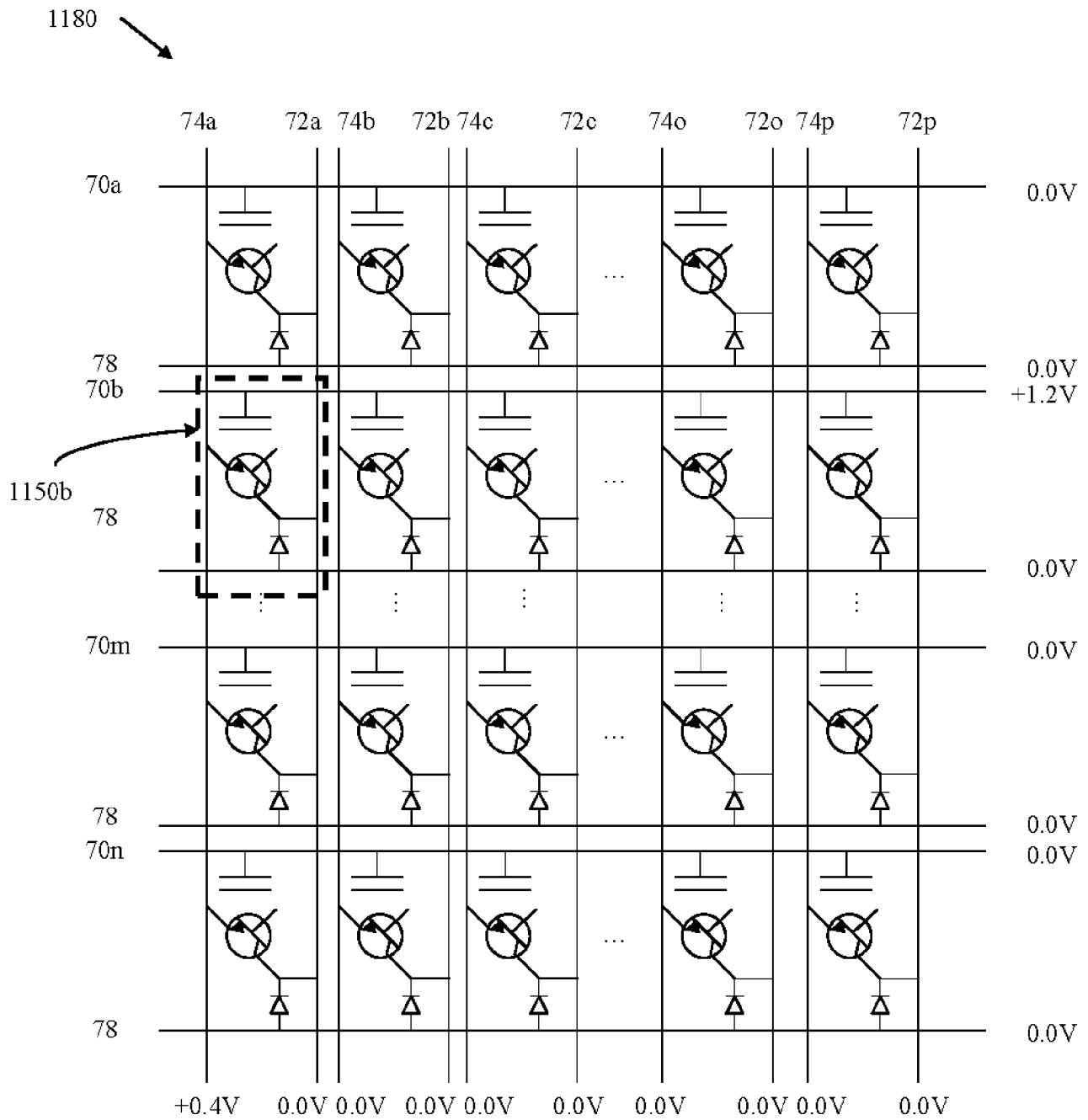


FIG. 161

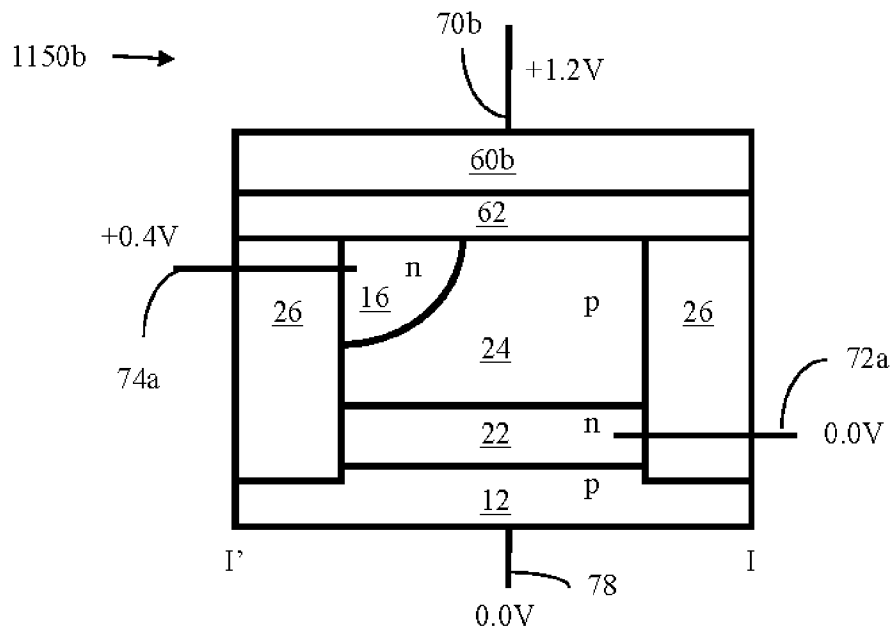


FIG. 162

1180

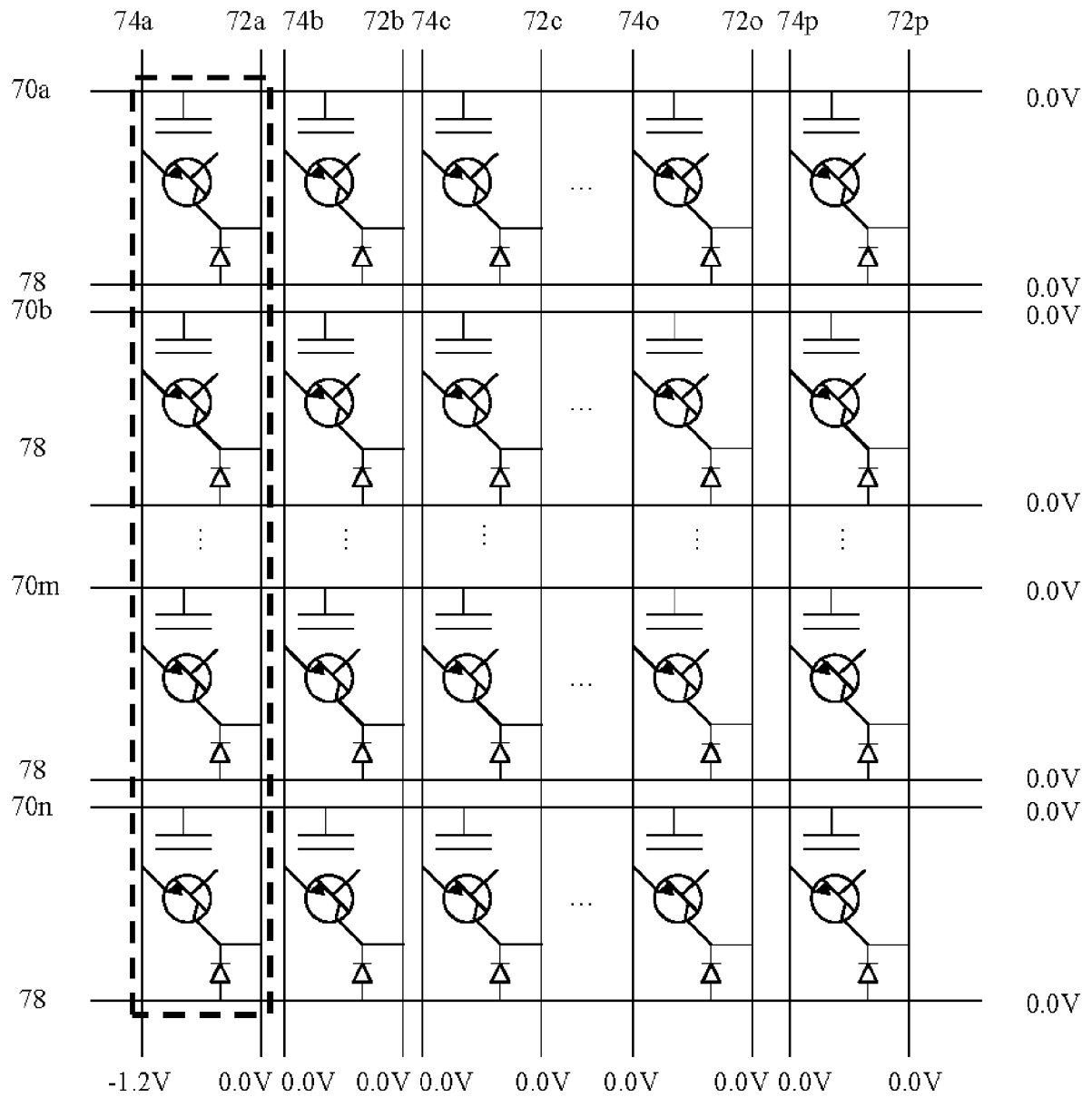


FIG. 163

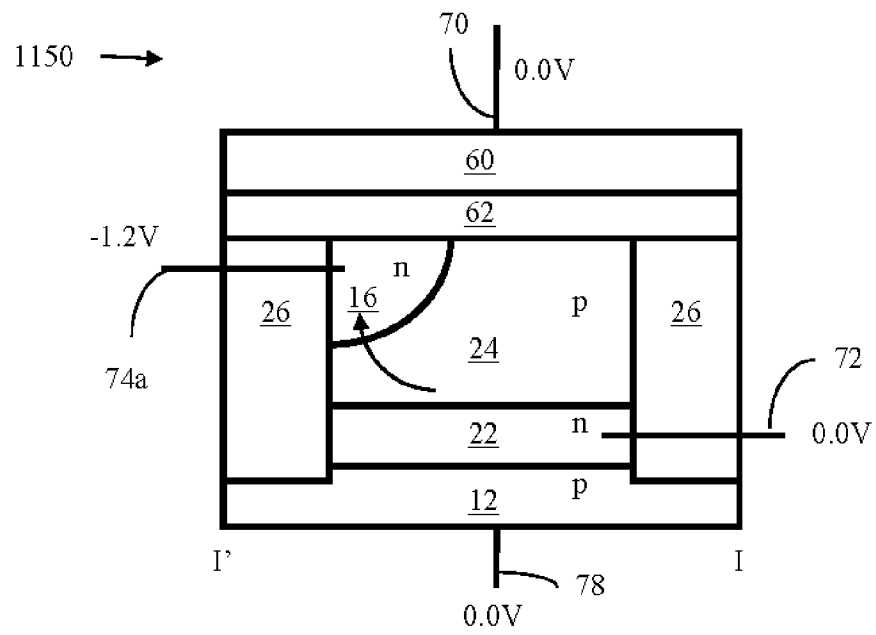


FIG. 164

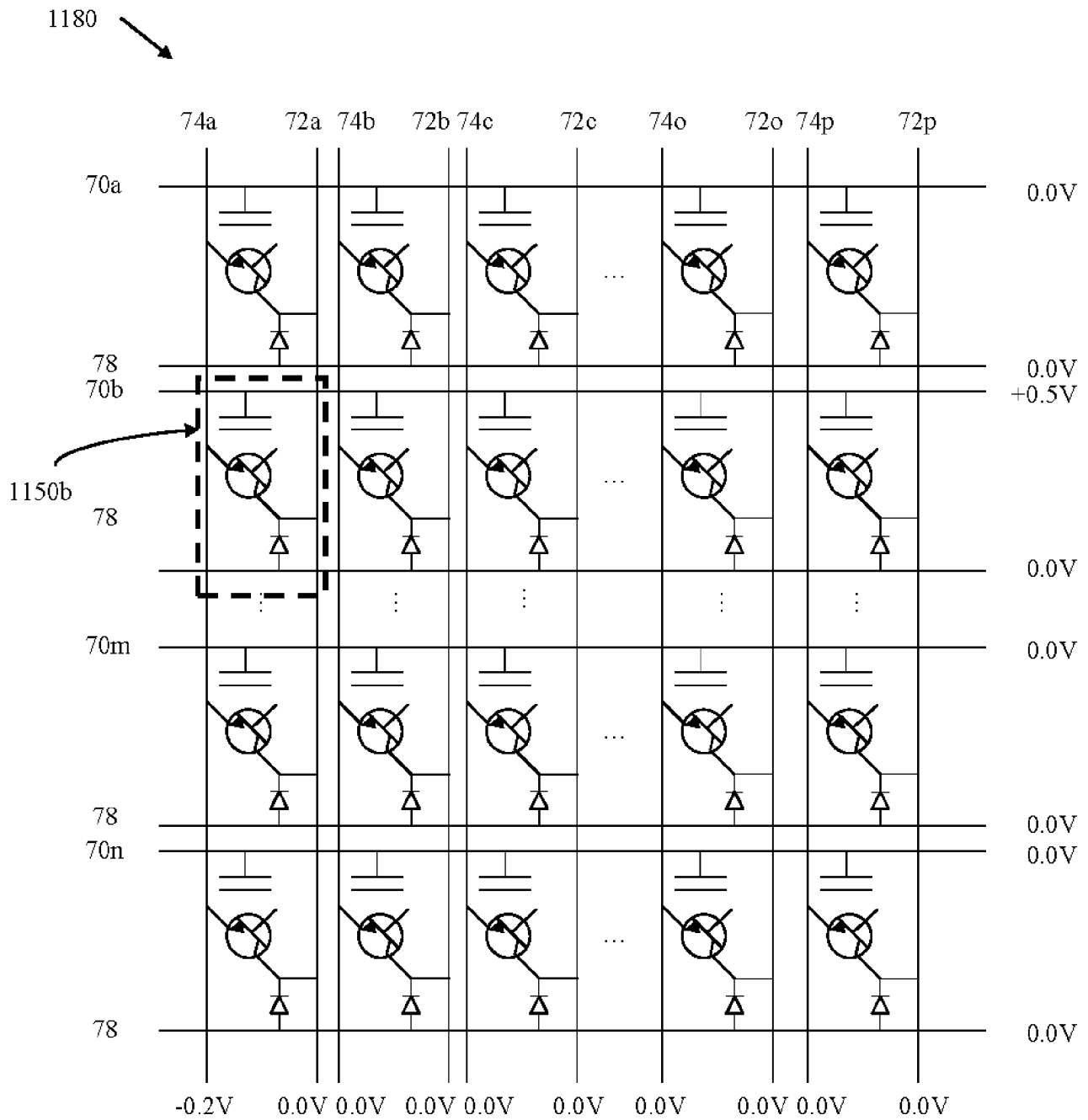


FIG. 165

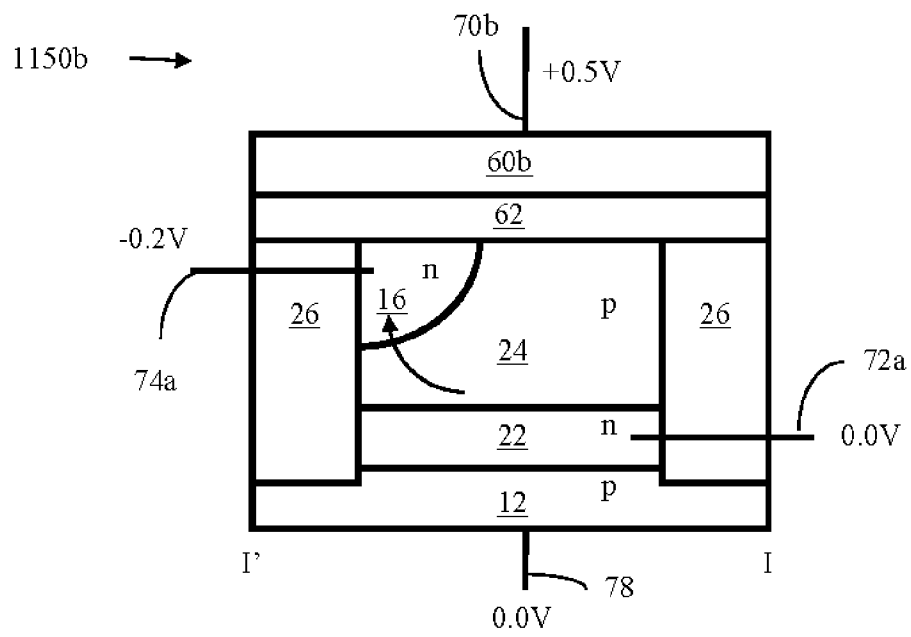


FIG. 166

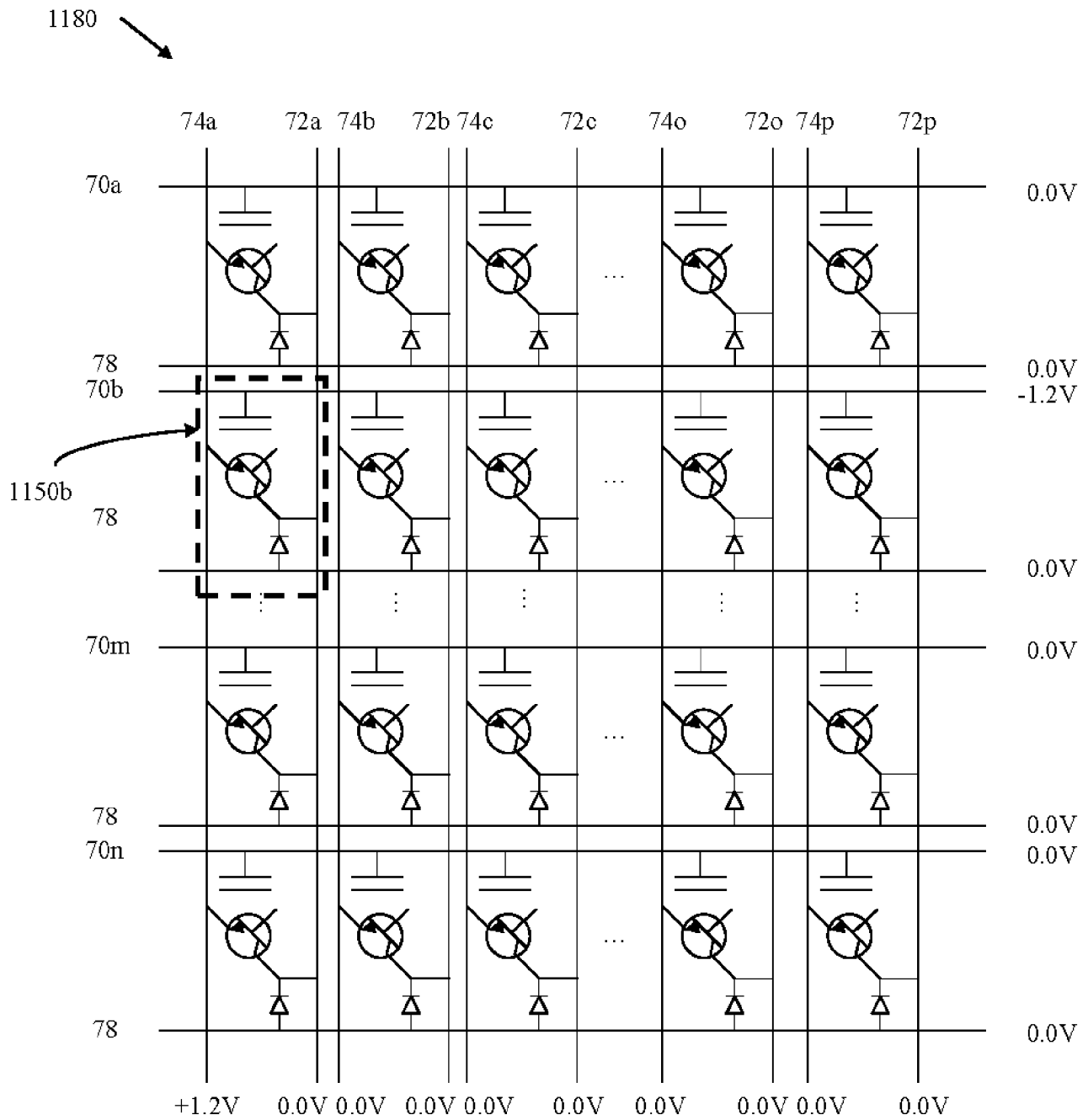


FIG. 167

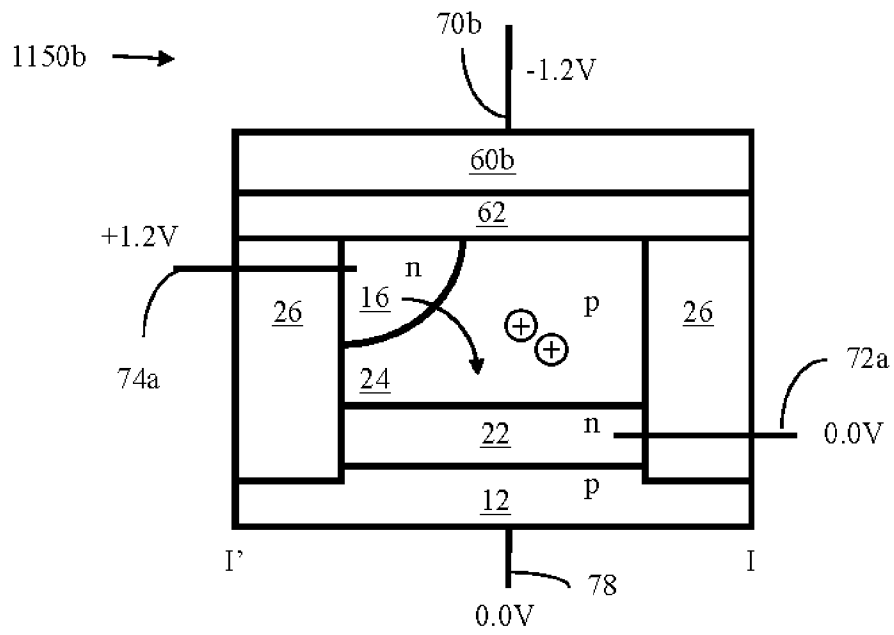


FIG. 168

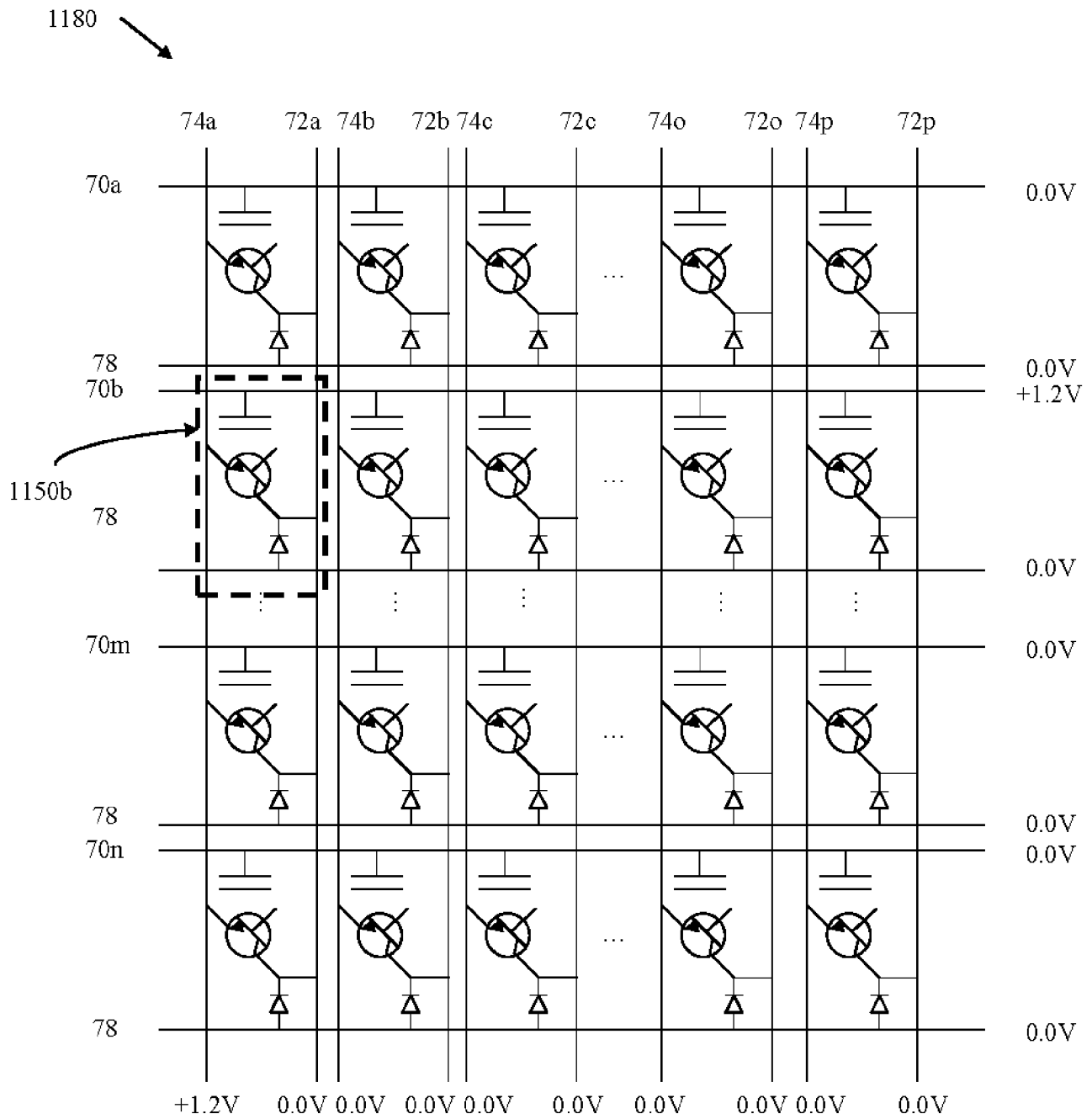


FIG. 169

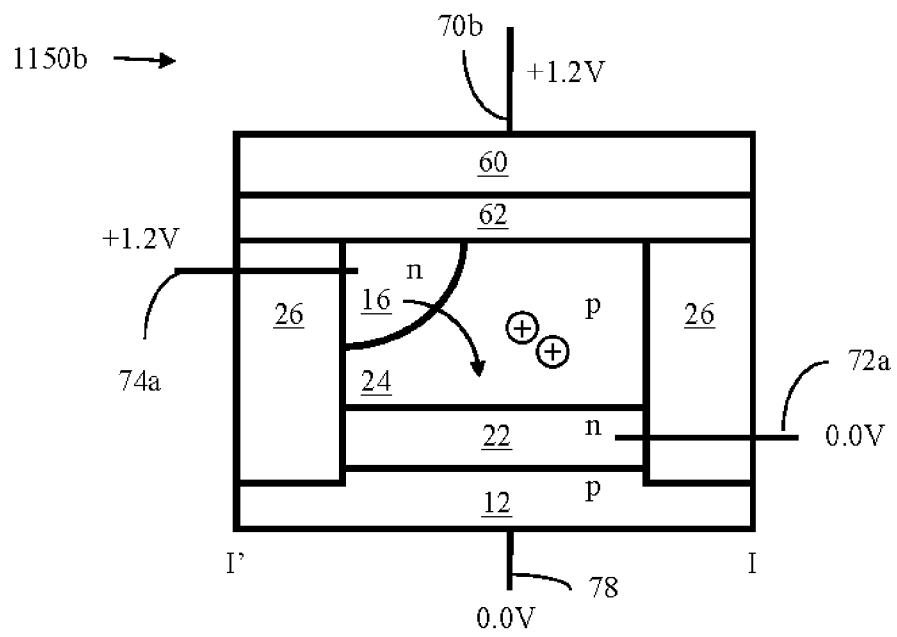


FIG. 170

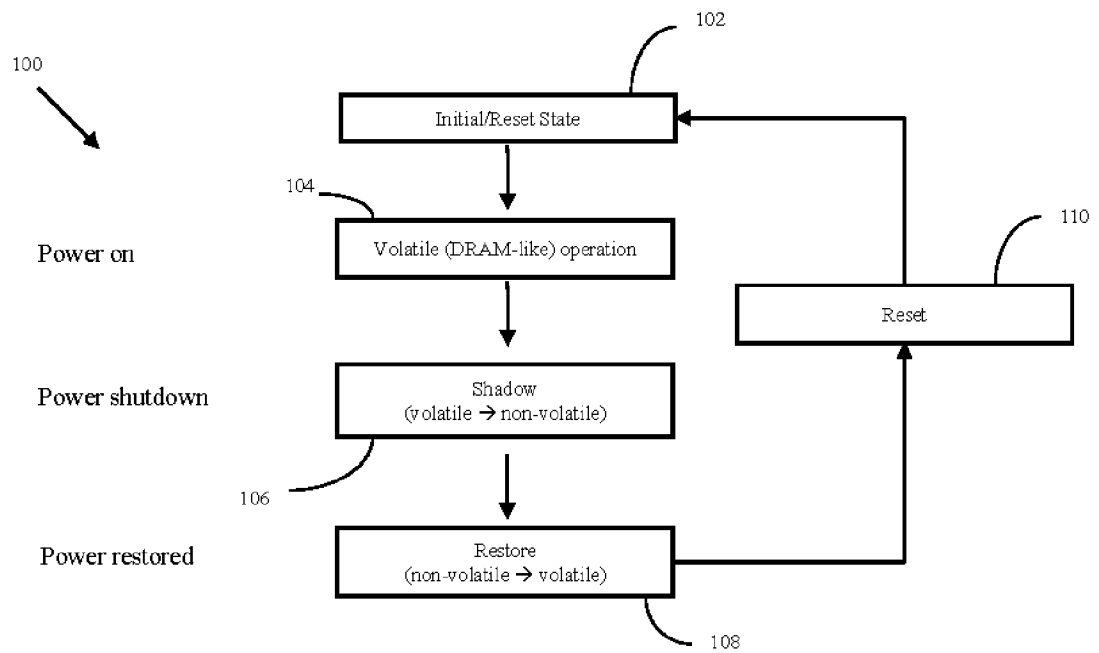


FIG. 171

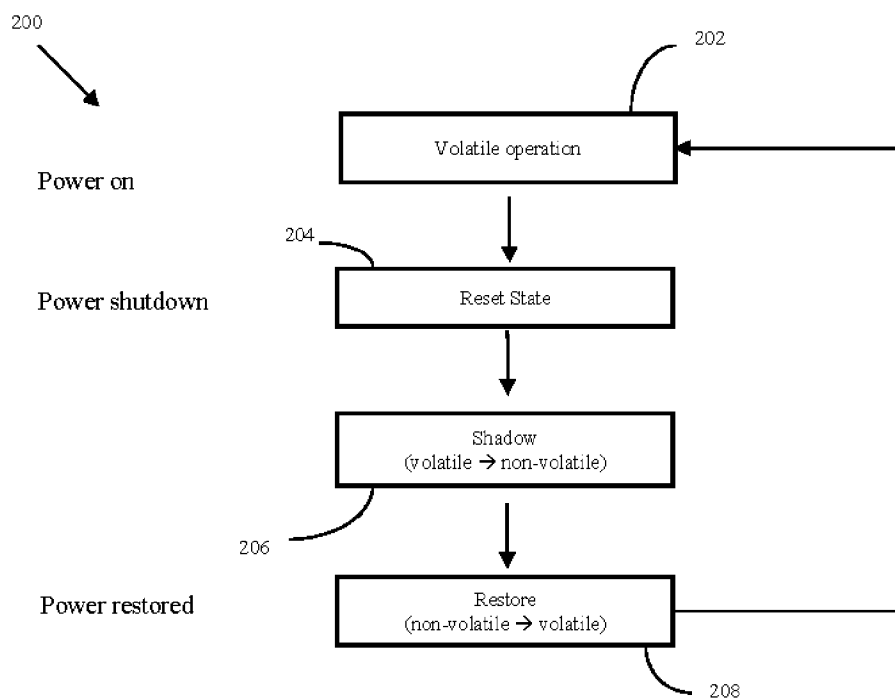


FIG. 172

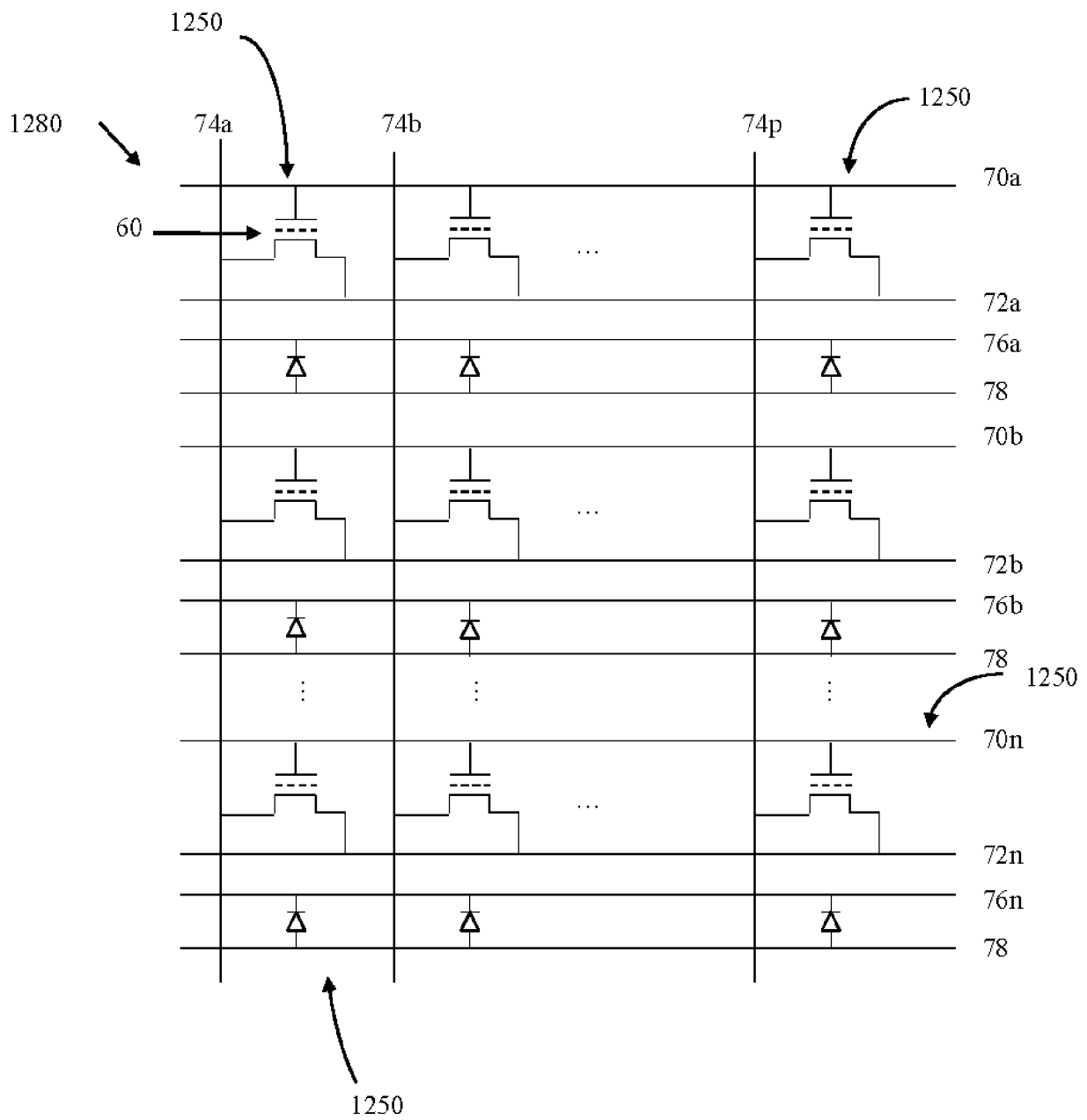


FIG. 173B

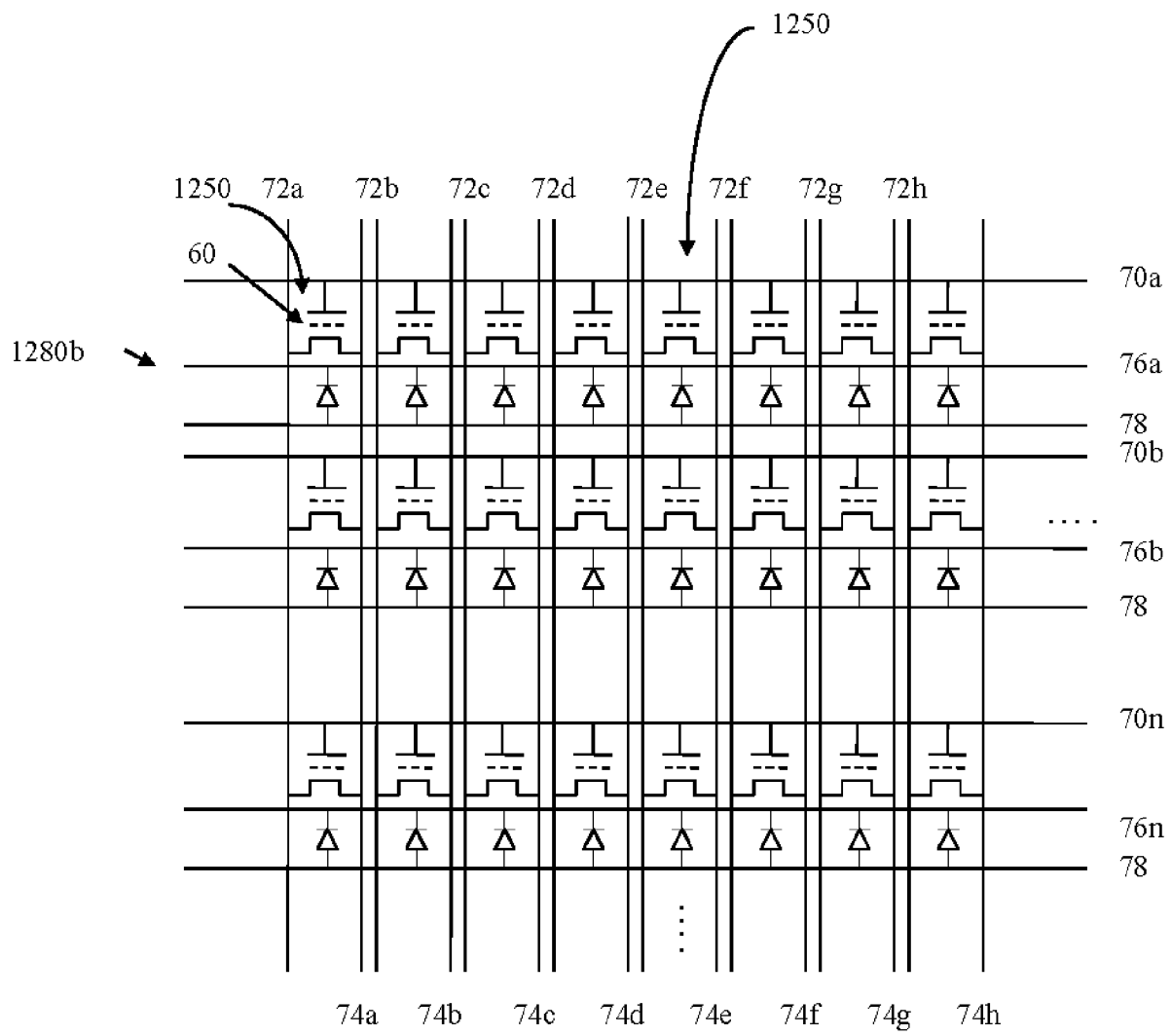


FIG. 173C

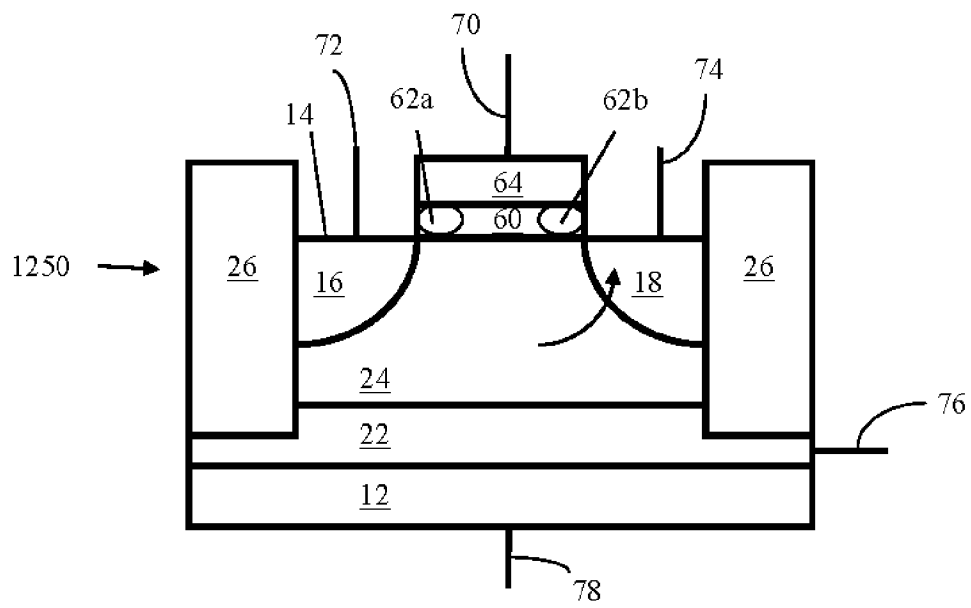


FIG. 175

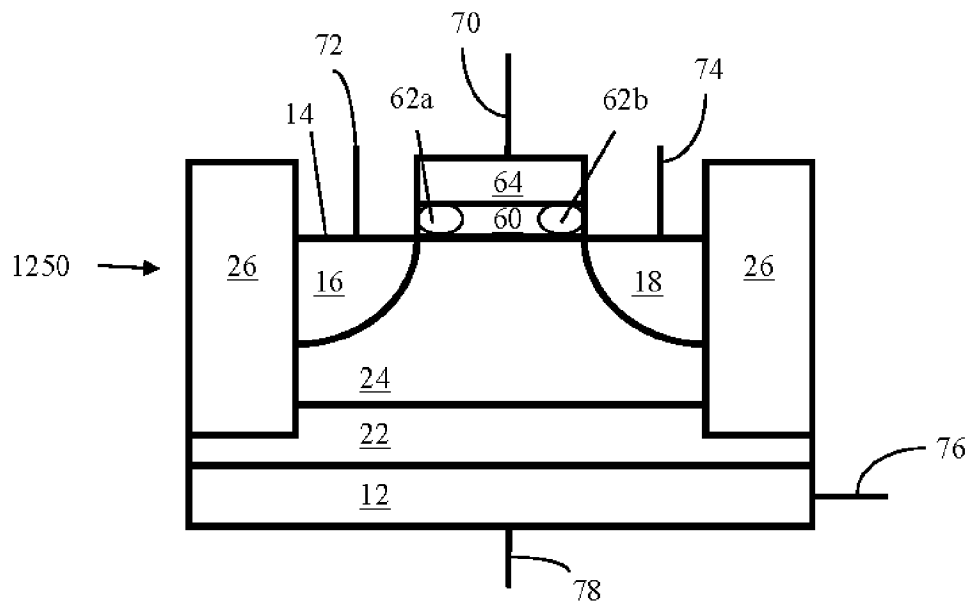


FIG. 176

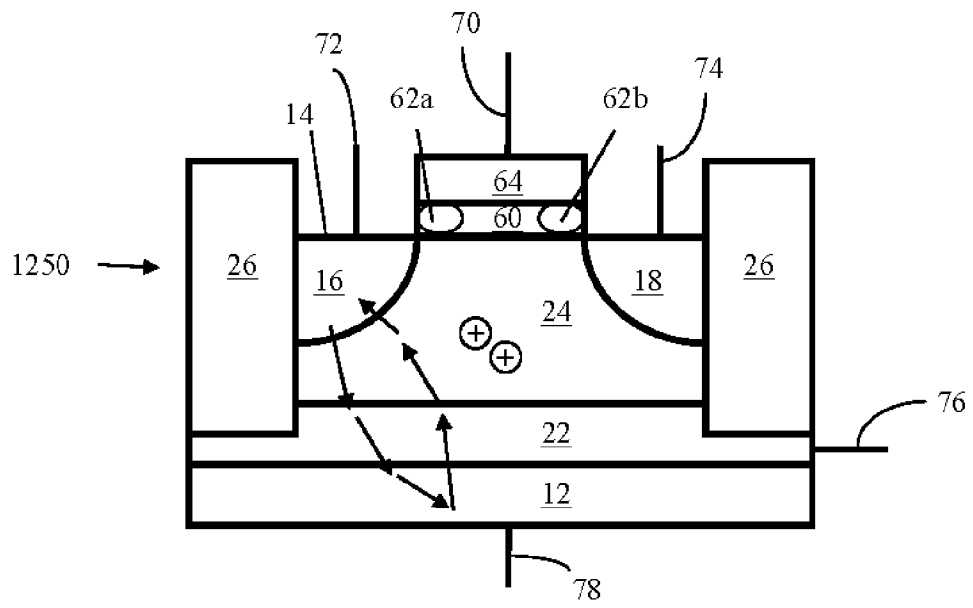


FIG. 177

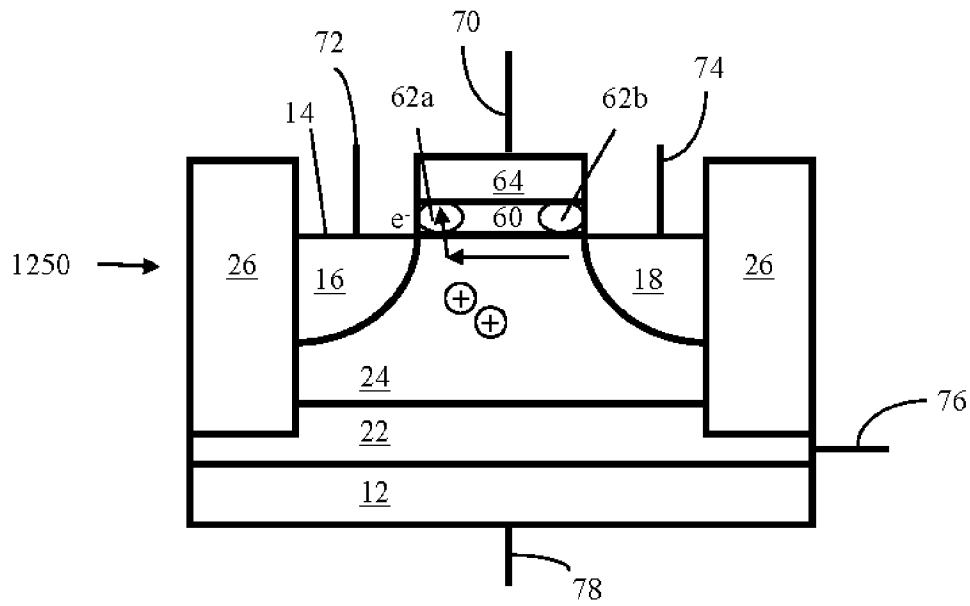


FIG. 178A

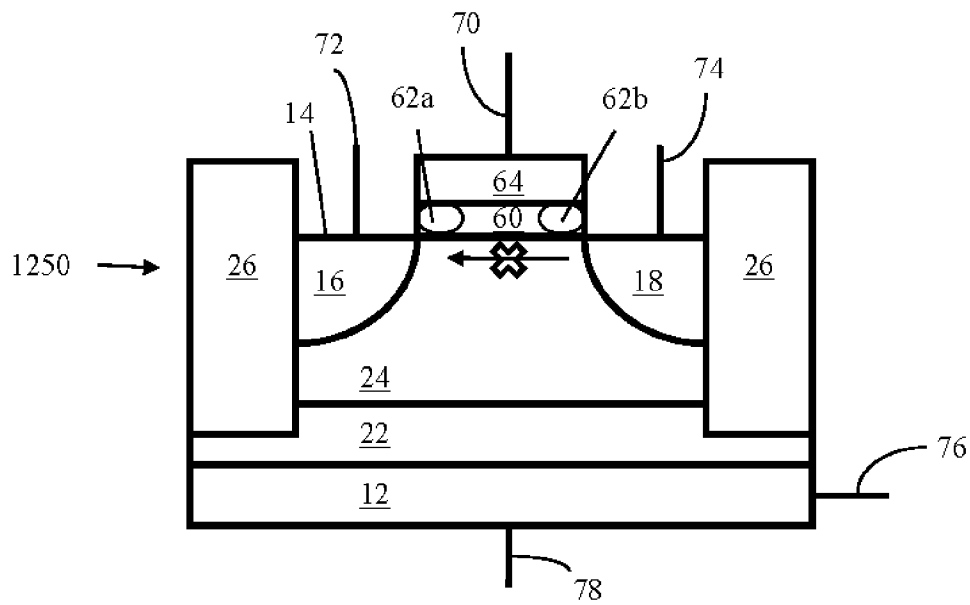


FIG. 178B

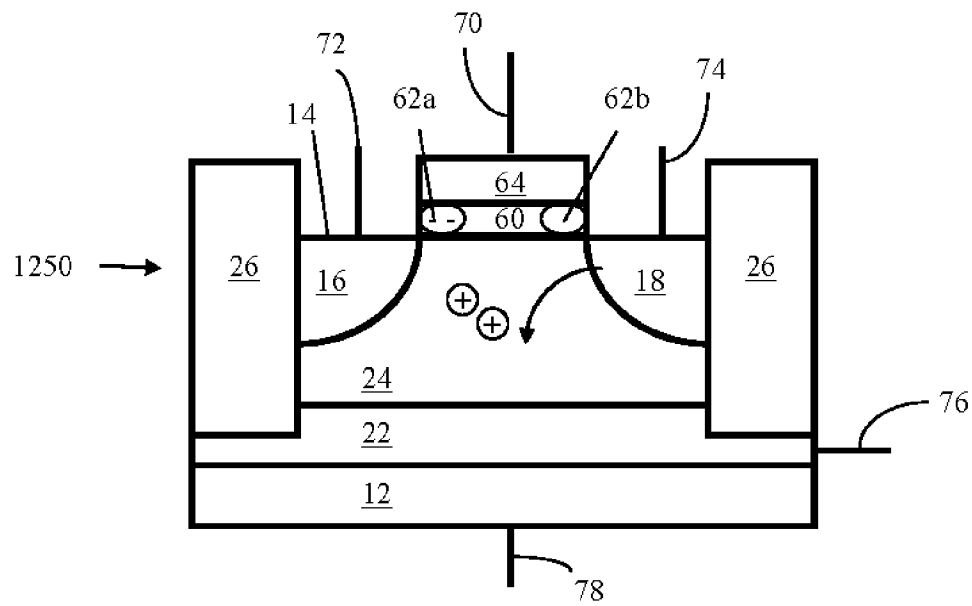


FIG. 179A

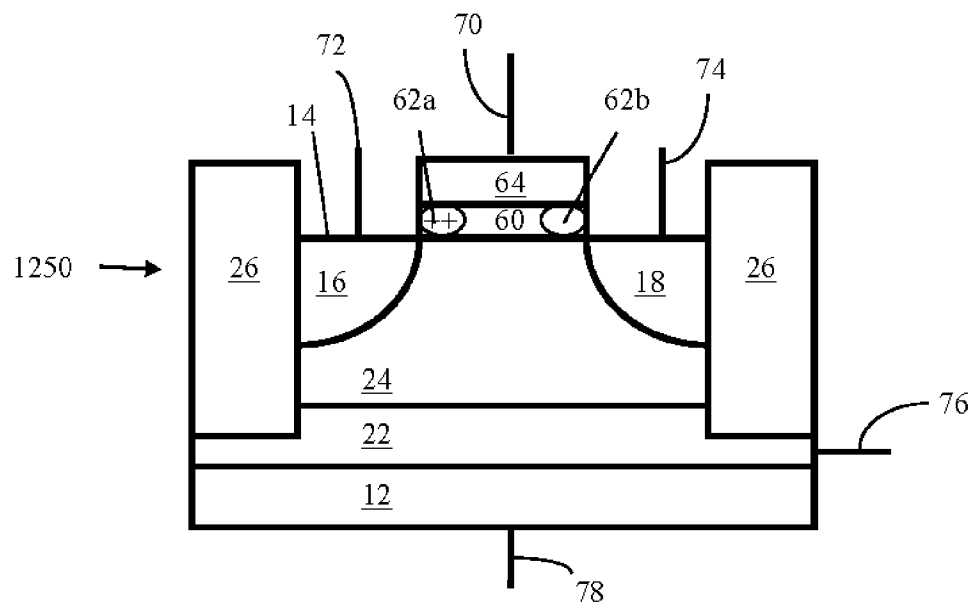


FIG. 179B

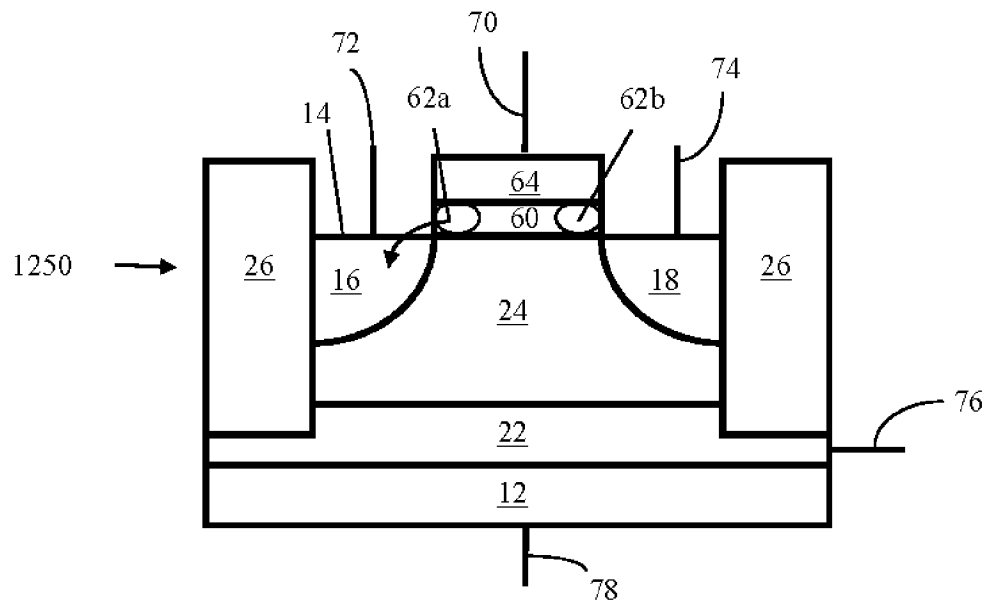


FIG. 180

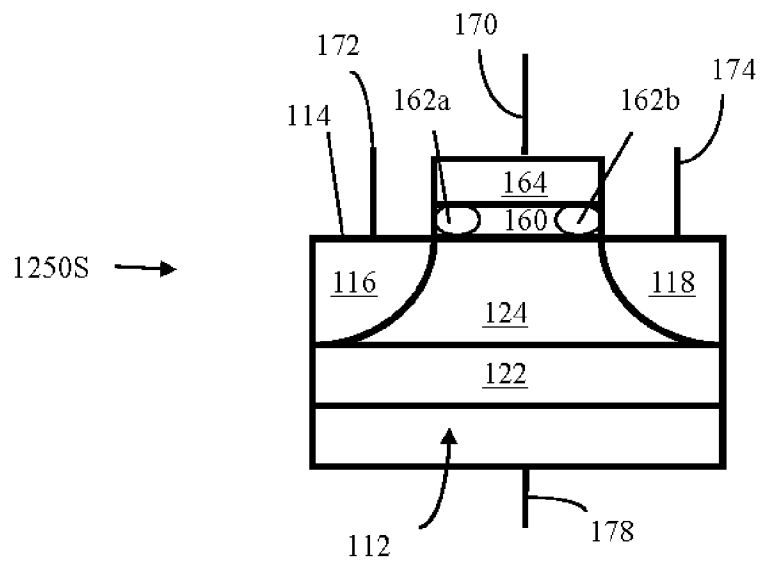


FIG. 181A

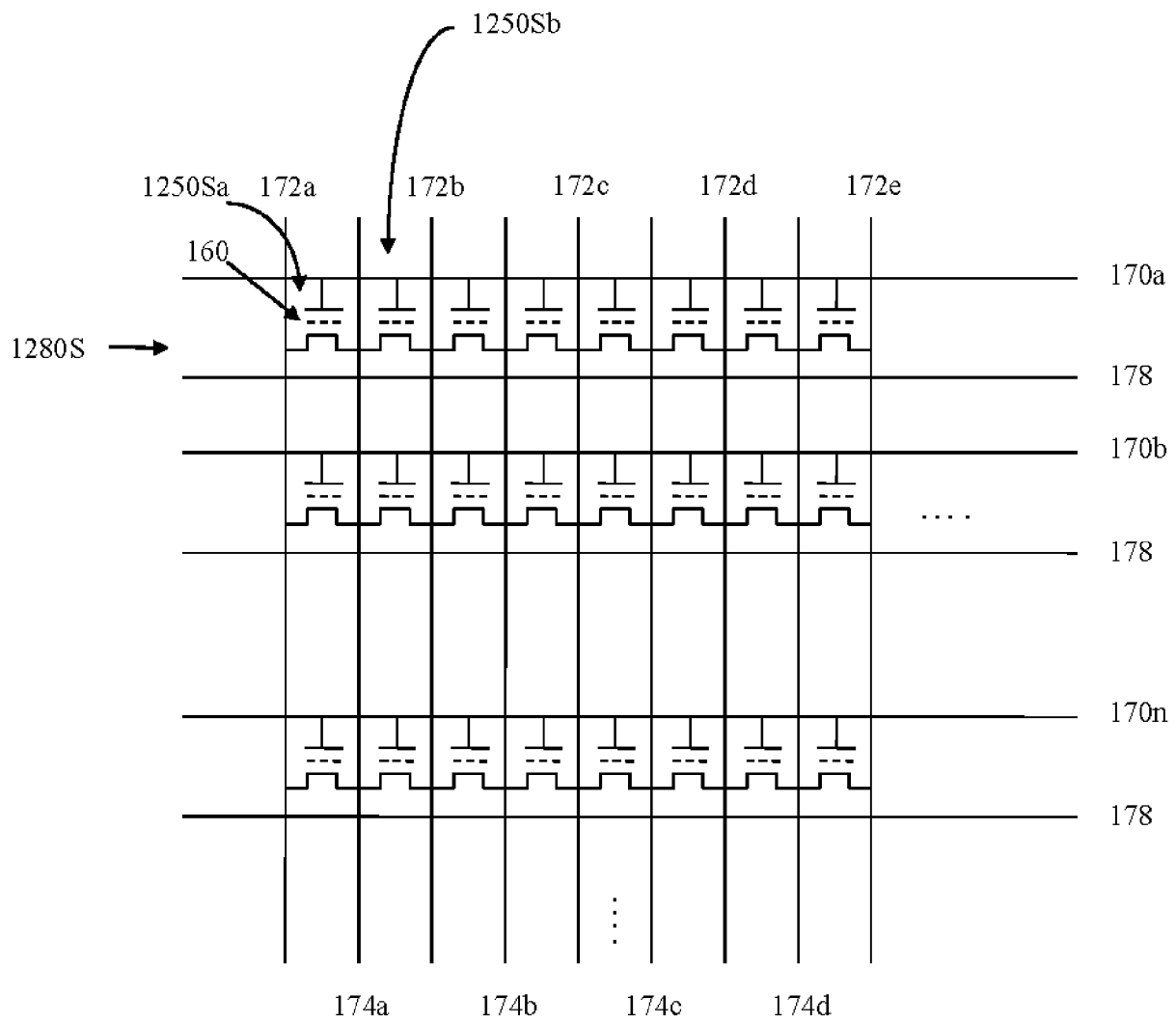


FIG. 181B

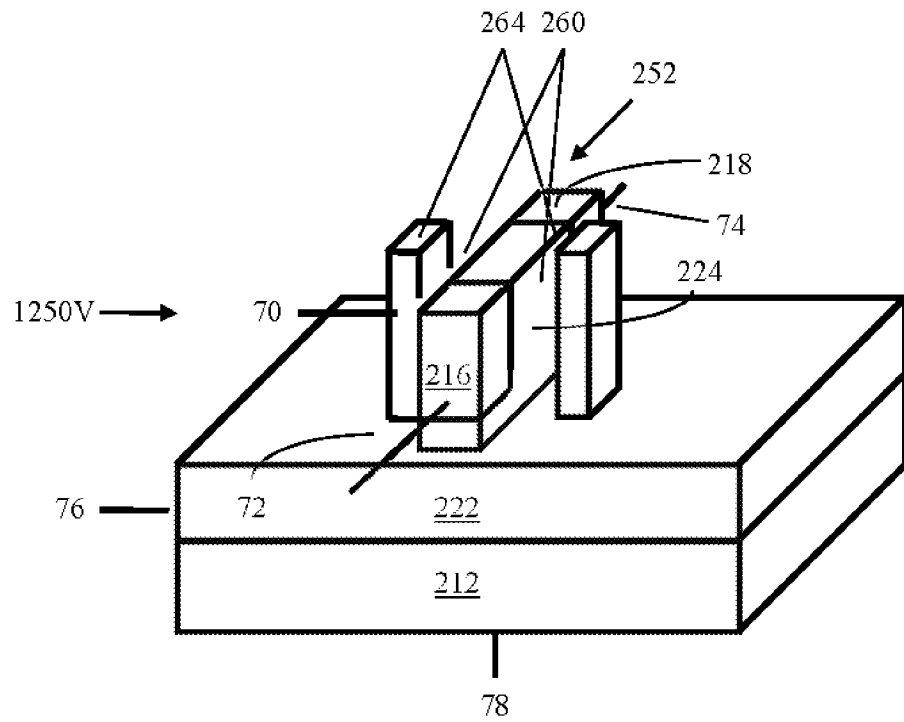


FIG. 182

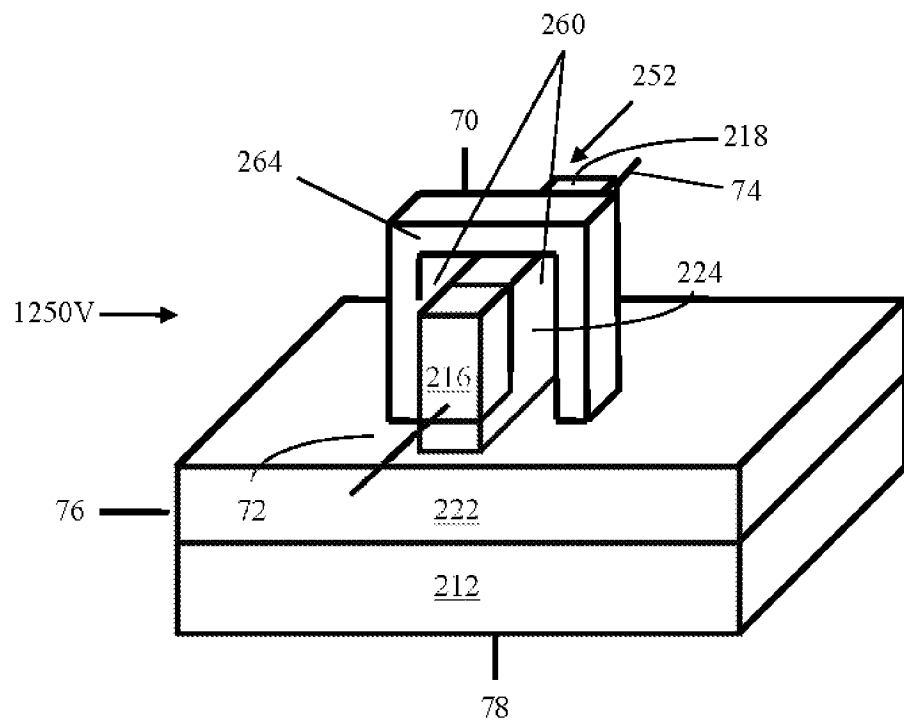


FIG. 183

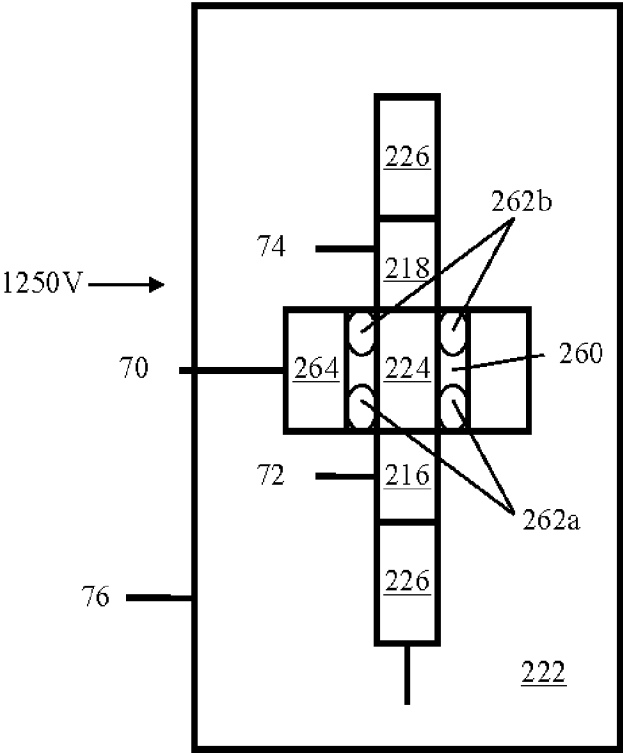
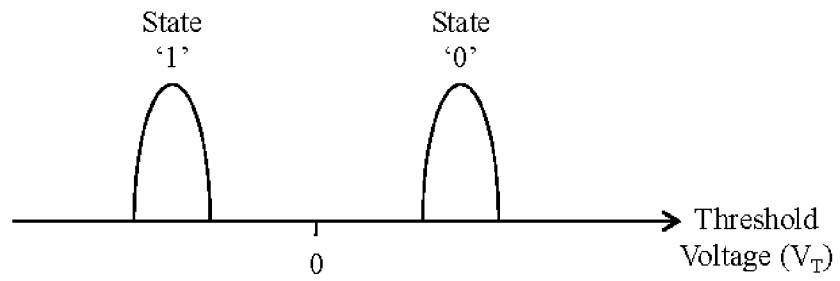
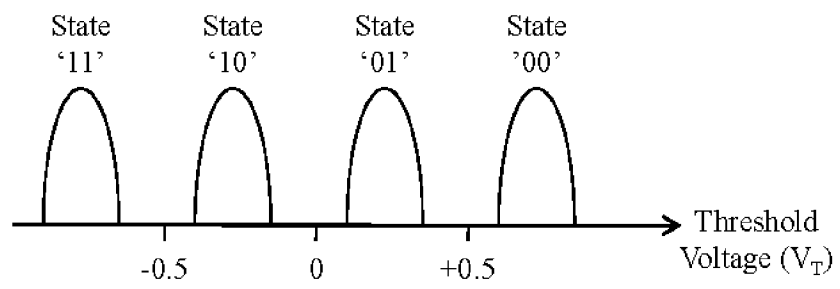


FIG. 184



Binary Cell

FIG. 185A



Multi-Level Cell

FIG. 185B

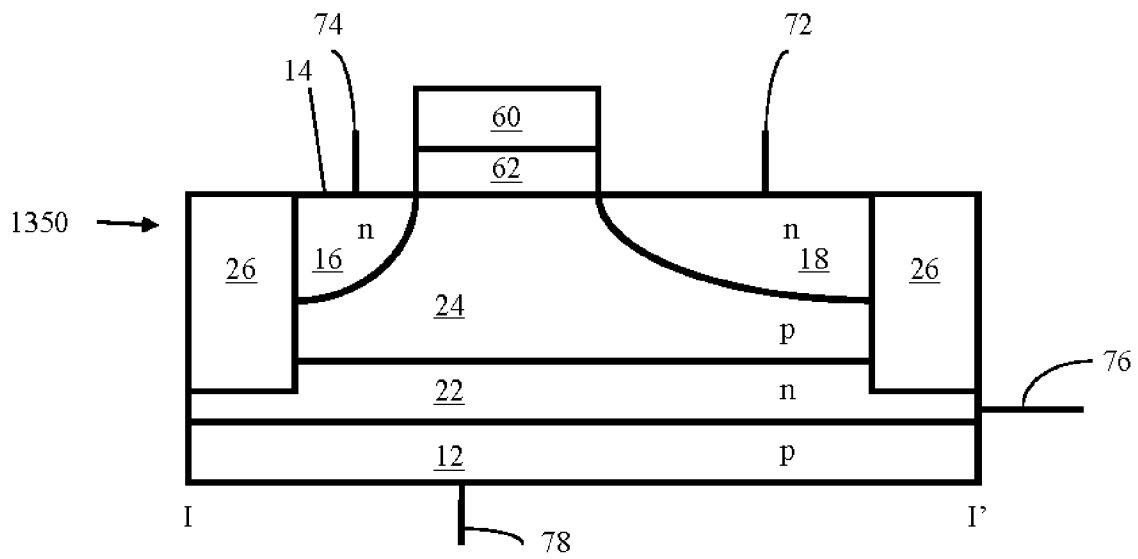


FIG. 186A

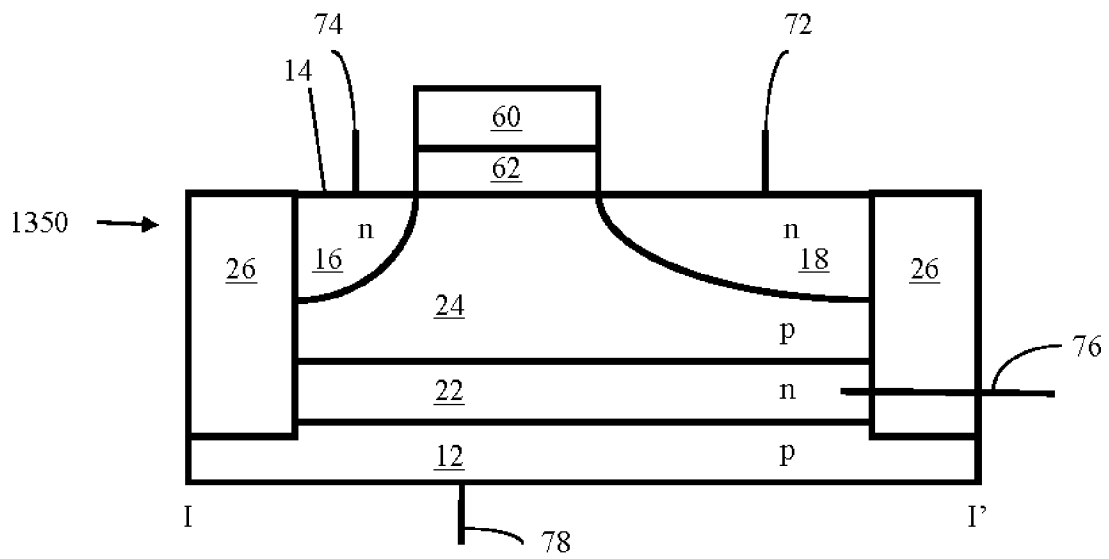


FIG. 186B

A cross-sectional view of a semiconductor device 1350. The device features a substrate 20 with a gate stack 16 (74) and a source/drain region 18 (72). A channel region 60 is defined between the gate stack and the source/drain region. A first conductive layer 24 is formed on the channel region 60. A second conductive layer 30c is formed on the first conductive layer 24. A third conductive layer 30a is formed on the second conductive layer 30c. A fourth conductive layer 30b is formed on the third conductive layer 30a. A fifth conductive layer 30d is formed on the fourth conductive layer 30b. A sixth conductive layer 30e is formed on the fifth conductive layer 30d. A seventh conductive layer 30f is formed on the sixth conductive layer 30e. An eighth conductive layer 30g is formed on the seventh conductive layer 30f. A ninth conductive layer 30h is formed on the eighth conductive layer 30g. A tenth conductive layer 30i is formed on the ninth conductive layer 30h. An eleventh conductive layer 30j is formed on the tenth conductive layer 30i. A twelfth conductive layer 30k is formed on the eleventh conductive layer 30j. A thirteenth conductive layer 30l is formed on the twelfth conductive layer 30k. A fourteenth conductive layer 30m is formed on the thirteenth conductive layer 30l. A fifteenth conductive layer 30n is formed on the fourteenth conductive layer 30m. A sixteenth conductive layer 30o is formed on the fifteenth conductive layer 30n. A seventeenth conductive layer 30p is formed on the sixteenth conductive layer 30o. An eighteenth conductive layer 30q is formed on the seventeenth conductive layer 30p. A nineteenth conductive layer 30r is formed on the eighteenth conductive layer 30q. A twentieth conductive layer 30s is formed on the nineteenth conductive layer 30r. A twenty-first conductive layer 30t is formed on the twentieth conductive layer 30s. A twenty-second conductive layer 30u is formed on the twenty-first conductive layer 30t. A twenty-third conductive layer 30v is formed on the twenty-second conductive layer 30u. A twenty-fourth conductive layer 30w is formed on the twenty-third conductive layer 30v. A twenty-fifth conductive layer 30x is formed on the twenty-fourth conductive layer 30w. A twenty-sixth conductive layer 30y is formed on the twenty-fifth conductive layer 30x. A twenty-seventh conductive layer 30z is formed on the twenty-sixth conductive layer 30y. A twenty-eighth conductive layer 30aa is formed on the twenty-seventh conductive layer 30z. A twenty-ninth conductive layer 30ab is formed on the twenty-eighth conductive layer 30aa. A thirtieth conductive layer 30ac is formed on the twenty-ninth conductive layer 30ab. A thirty-first conductive layer 30ad is formed on the thirtieth conductive layer 30ac. A thirty-second conductive layer 30ae is formed on the thirty-first conductive layer 30ad. A thirty-third conductive layer 30af is formed on the thirty-second conductive layer 30ae. A thirty-fourth conductive layer 30ag is formed on the thirty-third conductive layer 30af. A thirty-fifth conductive layer 30ah is formed on the thirty-fourth conductive layer 30ag. A thirty-sixth conductive layer 30ai is formed on the thirty-fifth conductive layer 30ah. A thirty-seventh conductive layer 30aj is formed on the thirty-sixth conductive layer 30ai. A thirty-eighth conductive layer 30ak is formed on the thirty-seventh conductive layer 30aj. A thirty-ninth conductive layer 30al is formed on the thirty-eighth conductive layer 30ak. A fortieth conductive layer 30am is formed on the thirty-ninth conductive layer 30al. A forty-first conductive layer 30an is formed on the fortieth conductive layer 30am. A forty-second conductive layer 30ao is formed on the forty-first conductive layer 30an. A forty-third conductive layer 30ap is formed on the forty-second conductive layer 30ao. A forty-fourth conductive layer 30aq is formed on the forty-third conductive layer 30ap. A forty-fifth conductive layer 30ar is formed on the forty-fourth conductive layer 30aq. A forty-sixth conductive layer 30as is formed on the forty-fifth conductive layer 30ar. A forty-seventh conductive layer 30at is formed on the forty-sixth conductive layer 30as. A forty-eighth conductive layer 30au is formed on the forty-seventh conductive layer 30at. A forty-ninth conductive layer 30av is formed on the forty-eighth conductive layer 30au. A fiftieth conductive layer 30aw is formed on the forty-ninth conductive layer 30av. A fifty-first conductive layer 30ax is formed on the fiftieth conductive layer 30aw. A fifty-second conductive layer 30ay is formed on the fifty-first conductive layer 30ax. A fifty-third conductive layer 30az is formed on the fifty-second conductive layer 30ay. A fifty-fourth conductive layer 30ba is formed on the fifty-third conductive layer 30az. A fifty-fifth conductive layer 30bb is formed on the fifty-fourth conductive layer 30ba. A fifty-sixth conductive layer 30bc is formed on the fifty-fifth conductive layer 30bb. A fifty-seventh conductive layer 30bd is formed on the fifty-sixth conductive layer 30bc. A fifty-eighth conductive layer 30be is formed on the fifty-seventh conductive layer 30bd. A fifty-ninth conductive layer 30bf is formed on the fifty-eighth conductive layer 30be. A sixtieth conductive layer 30bg is formed on the fifty-ninth conductive layer 30bf. A sixty-first conductive layer 30bh is formed on the sixtieth conductive layer 30bg. A sixty-second conductive layer 30bi is formed on the sixty-first conductive layer 30bh. A sixty-third conductive layer 30bj is formed on the sixty-second conductive layer 30bi. A sixty-fourth conductive layer 30bk is formed on the sixty-third conductive layer 30bj. A sixty-fifth conductive layer 30bl is formed on the sixty-fourth conductive layer 30bk. A sixty-sixth conductive layer 30bm is formed on the sixty-fifth conductive layer 30bl. A sixty-seventh conductive layer 30bn is formed on the sixty-sixth conductive layer 30bm. A sixty-eighth conductive layer 30bo is formed on the sixty-seventh conductive layer 30bn. A sixty-ninth conductive layer 30bp is formed on the sixty-eighth conductive layer 30bo. A seventieth conductive layer 30bq is formed on the sixty-ninth conductive layer 30bp. A seventy-first conductive layer 30br is formed on the seventieth conductive layer 30bq. A seventy-second conductive layer 30bs is formed on the seventy-first conductive layer 30br. A seventy-third conductive layer 30bt is formed on the seventy-second conductive layer 30bs. A seventy-fourth conductive layer 30bu is formed on the seventy-third conductive layer 30bt. A seventy-fifth conductive layer 30bv is formed on the seventy-fourth conductive layer 30bu. A seventy-sixth conductive layer 30bw is formed on the seventy-fifth conductive layer 30bv. A seventy-seventh conductive layer 30bx is formed on the seventy-sixth conductive layer 30bw. A seventy-eighth conductive layer 30by is formed on the seventy-seventh conductive layer 30bx. A seventy-ninth conductive layer 30bz is formed on the seventy-eighth conductive layer 30by. An eightieth conductive layer 30ca is formed on the seventy-ninth conductive layer 30bz. An eighty-first conductive layer 30cb is formed on the eightieth conductive layer 30ca. An eighty-second conductive layer 30cc is formed on the eighty-first conductive layer 30cb. An eighty-third conductive layer 30cd is formed on the eighty-second conductive layer 30cc. An eighty-fourth conductive layer 30ce is formed on the eighty-third conductive layer 30cd. An eighty-fifth conductive layer 30cf is formed on the eighty-fourth conductive layer 30ce. An eighty-sixth conductive layer 30cg is formed on the eighty-fifth conductive layer 30cf. An eighty-seventh conductive layer 30ch is formed on the eighty-sixth conductive layer 30cg. An eighty-eighth conductive layer 30ci is formed on the eighty-seventh conductive layer 30ch. An eighty-ninth conductive layer 30cj is formed on the eighty-eighth conductive layer 30ci. A ninetieth conductive layer 30ck is formed on the eighty-ninth conductive layer 30cj. A hundredth conductive layer 30cl is formed on the ninetieth conductive layer 30ck. A hundred and first conductive layer 30cm is formed on the hundredth conductive layer 30cl. A hundred and second conductive layer 30cn is formed on the hundred and first conductive layer 30cm. A hundred and third conductive layer 30co is formed on the hundred and second conductive layer 30cn. A hundred and fourth conductive layer 30cp is formed on the hundred and third conductive layer 30co. A hundred and fifth conductive layer 30cq is formed on the hundred and fourth conductive layer 30cp. A hundred and sixth conductive layer 30cr is formed on the hundred and fifth conductive layer 30cq. A hundred and seventh conductive layer 30cs is formed on the hundred and sixth conductive layer 30cr. A hundred and eighth conductive layer 30ct is formed on the hundred and seventh conductive layer 30cs. A hundred and ninth conductive layer 30cu is formed on the hundred and eighth conductive layer 30ct. A hundred and tenth conductive layer 30cv is formed on the hundred and ninth conductive layer 30cu. A hundred and eleventh conductive layer 30cw is formed on the hundred and tenth conductive layer 30cv. A hundred and twelfth conductive layer 30cx is formed on the hundred and eleventh conductive layer 30cw. A hundred and thirteenth conductive layer 30cy is formed on the hundred and twelfth conductive layer 30cx. A hundred and fourteenth conductive layer 30cz is formed on the hundred and thirteenth conductive layer 30cy. A hundred and fifteenth conductive layer 30da is formed on the hundred and fourteenth conductive layer 30cz. A hundred and sixteenth conductive layer 30db is formed on the hundred and fifteenth conductive layer 30da. A hundred and seventeenth conductive layer 30dc is formed on the hundred and sixteenth conductive layer 30db. A hundred and eighteenth conductive layer 30dd is formed on the hundred and seventeenth conductive layer 30dc. A hundred and nineteenth conductive layer 30de is formed on the hundred and eighteenth conductive layer 30dd. A hundred and twentieth conductive layer 30df is formed on the hundred and nineteenth conductive layer 30de. A hundred and twenty-first conductive layer 30dg is formed on the hundred and twentieth conductive layer 30df. A hundred and twenty-second conductive layer 30dh is formed on the hundred and twenty-first conductive layer 30dg. A hundred and twenty-third conductive layer 30di is formed on the hundred and twenty-second conductive layer 30dh. A hundred and twenty-fourth conductive layer 30dj is formed on the hundred and twenty-third conductive layer 30di. A hundred and twenty-fifth conductive layer 30dk is formed on the hundred and twenty-fourth conductive layer 30dj. A hundred and twenty-sixth conductive layer 30dl is formed on the hundred and twenty-fifth conductive layer 30dk. A hundred and twenty-seventh conductive layer 30dm is formed on the hundred and twenty-sixth conductive layer 30dl. A hundred and twenty-eighth conductive layer 30dn is formed on the hundred and twenty-seventh conductive layer 30dm. A hundred and twenty-ninth conductive layer 30do is formed on the hundred and twenty-eighth conductive layer 30dn. A hundred and thirtieth conductive layer 30dp is formed on the hundred and twenty-ninth conductive layer 30do. A hundred and thirty-first conductive layer 30dq is formed on the hundred and thirtieth conductive layer 30dp. A hundred and thirty-second conductive layer 30dr is formed on the hundred and thirty-first conductive layer 30dq. A hundred and thirty-third conductive layer 30ds is formed on the hundred and thirty-second conductive layer 30dr. A hundred and thirty-fourth conductive layer 30dt is formed on the hundred and thirty-third conductive layer 30ds. A hundred and thirty-fifth conductive layer 30du is formed on the hundred and thirty-fourth conductive layer 30dt. A hundred and thirty-sixth conductive layer 30dv is formed on the hundred and thirty-fifth conductive layer 30du. A hundred and thirty-seventh conductive layer 30dw is formed on the hundred and thirty-sixth conductive layer 30dv. A hundred and thirty-eighth conductive layer 30dx is formed on the hundred and thirty-seventh conductive layer 30dw. A hundred and thirty-ninth conductive layer 30dy is formed on the hundred and thirty-eighth conductive layer 30dx. A hundred and fortieth conductive layer 30dz is formed on the hundred and thirty-ninth conductive layer 30dy. A hundred and forty-first conductive layer 30ea is formed on the hundred and fortieth conductive layer 30dz. A hundred and forty-second conductive layer 30eb is formed on the hundred and forty-first conductive layer 30ea. A hundred and forty-third conductive layer 30ec is formed on the hundred and forty-second conductive layer 30eb. A hundred and forty-fourth conductive layer 30ed is formed on the hundred and forty-third conductive layer 30ec. A hundred and forty-fifth conductive layer 30ee is formed on the hundred and forty-fourth conductive layer 30ed. A hundred and forty-sixth conductive layer 30ef is formed on the hundred and forty-fifth conductive layer 30ee. A hundred and forty-seventh conductive layer 30ef is formed on the hundred and forty-sixth conductive layer 30ef. A hundred and forty-eighth conductive layer 30ef is formed on the hundred and forty-seventh conductive layer 30ef. A hundred and forty-ninth conductive layer 30ef is formed on the hundred and forty-eighth conductive layer 30ef. A hundred and fiftieth conductive layer 30ef is formed on the hundred and forty-ninth conductive layer 30ef. A hundred and fifty-first conductive layer 30ef is formed on the hundred and fiftieth conductive layer 30ef. A hundred and fifty-second conductive layer 30ef is formed on the hundred and fifty-first conductive layer 30ef. A hundred and fifty-third conductive layer 30ef is formed on the hundred and fifty-second conductive layer 30ef. A hundred and fifty-fourth conductive layer 30ef is formed on the hundred and fifty-third conductive layer 30ef. A hundred and fifty-fifth conductive layer 30ef is formed on the hundred and fifty-fourth conductive layer 30ef. A hundred and fifty-sixth conductive layer 30ef is formed on the hundred and fifty-fifth conductive layer 30ef. A hundred and fifty-seventh conductive layer 30ef is formed on the hundred and fifty-sixth conductive layer 30ef. A hundred and fifty-eighth conductive layer 30ef is formed on the hundred and fifty-seventh conductive layer 30ef. A hundred and fifty-ninth conductive layer 30ef is formed on the hundred and fifty-eighth conductive layer 30ef. A hundred and sixtieth conductive layer 30ef is formed on the hundred and fifty-ninth conductive layer 30ef. A hundred and sixty-first conductive layer 30ef is formed on the hundred and sixtyth conductive layer 30ef. A hundred and sixty-second conductive layer 30ef is formed on the hundred

FIG. 186D

Exemplary Memory Array 1380 with
Representative Memory Cells 1350a, 1350b, 1350c
and 1350d

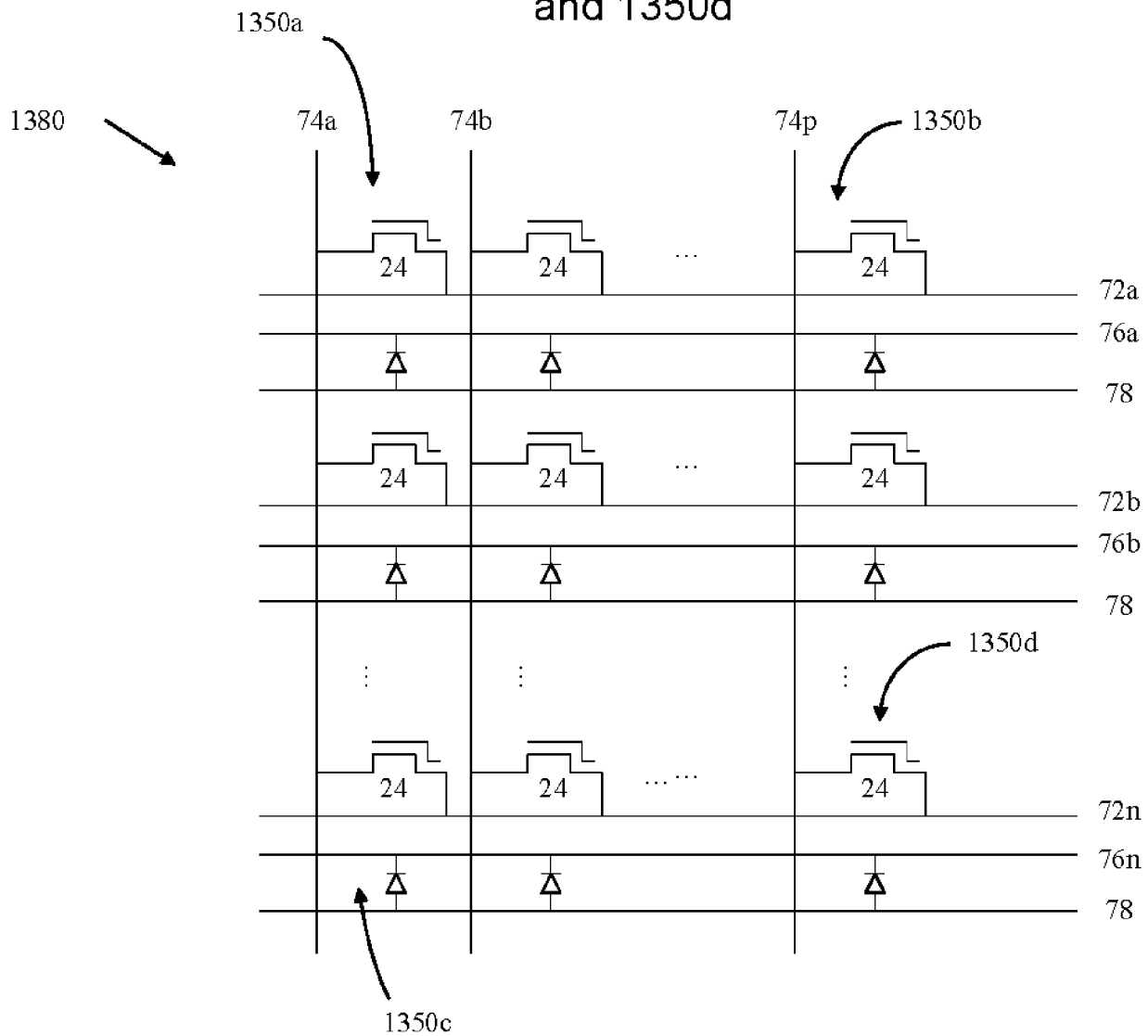


FIG. 186E

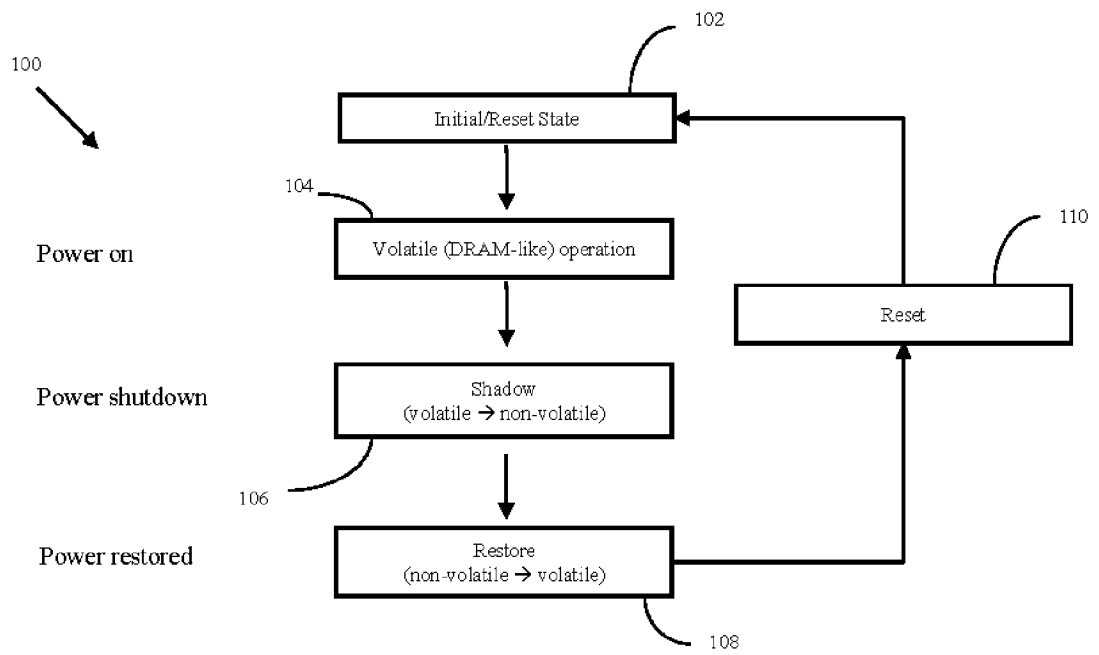


FIG. 187

Array Hold Operation
(All Memory Cells 1350)

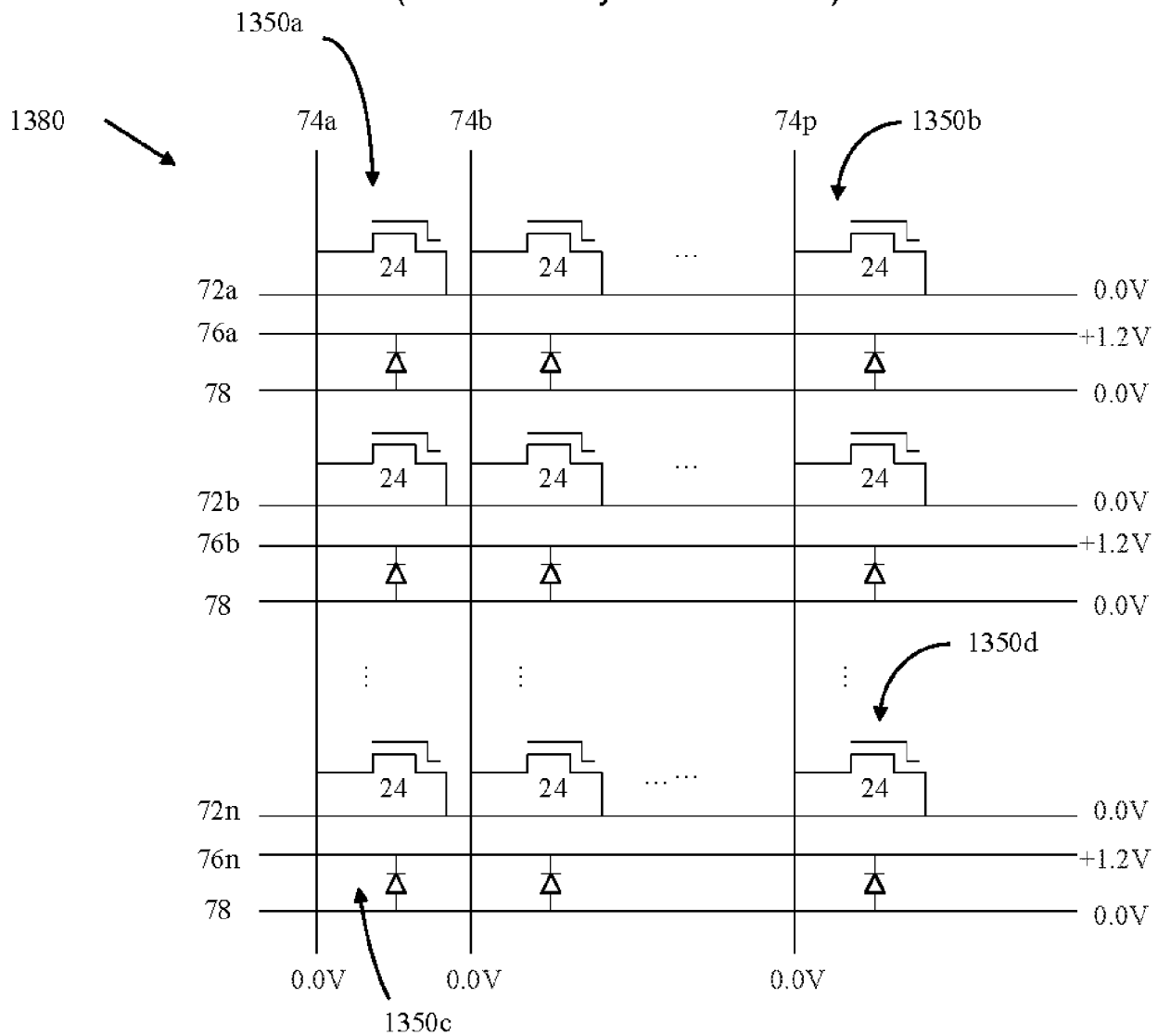


FIG. 188

Floating Body 24 is positively charged and $V(\text{BL } 16) = 0.0\text{V}$

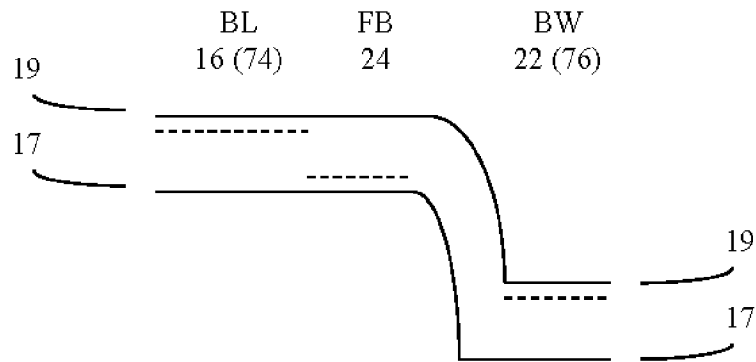


FIG. 189A

FB is neutrally charged; and $V(\text{BL } 16) = V(\text{FB } 24) = 0\text{V}$

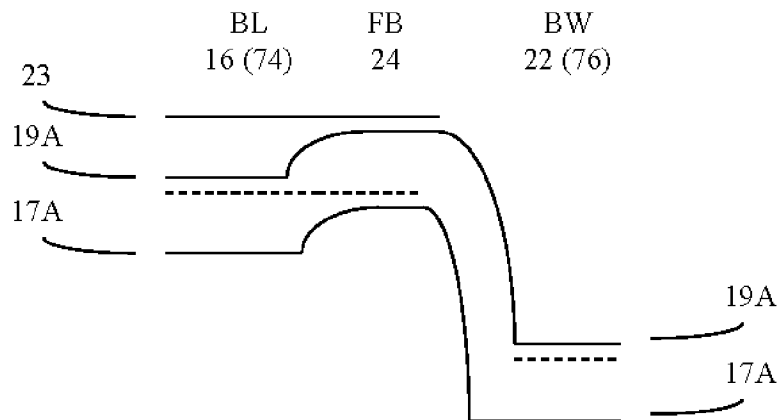


FIG. 189B

Read Operation, Active Bit Line High
(Memory Cell 1350a)

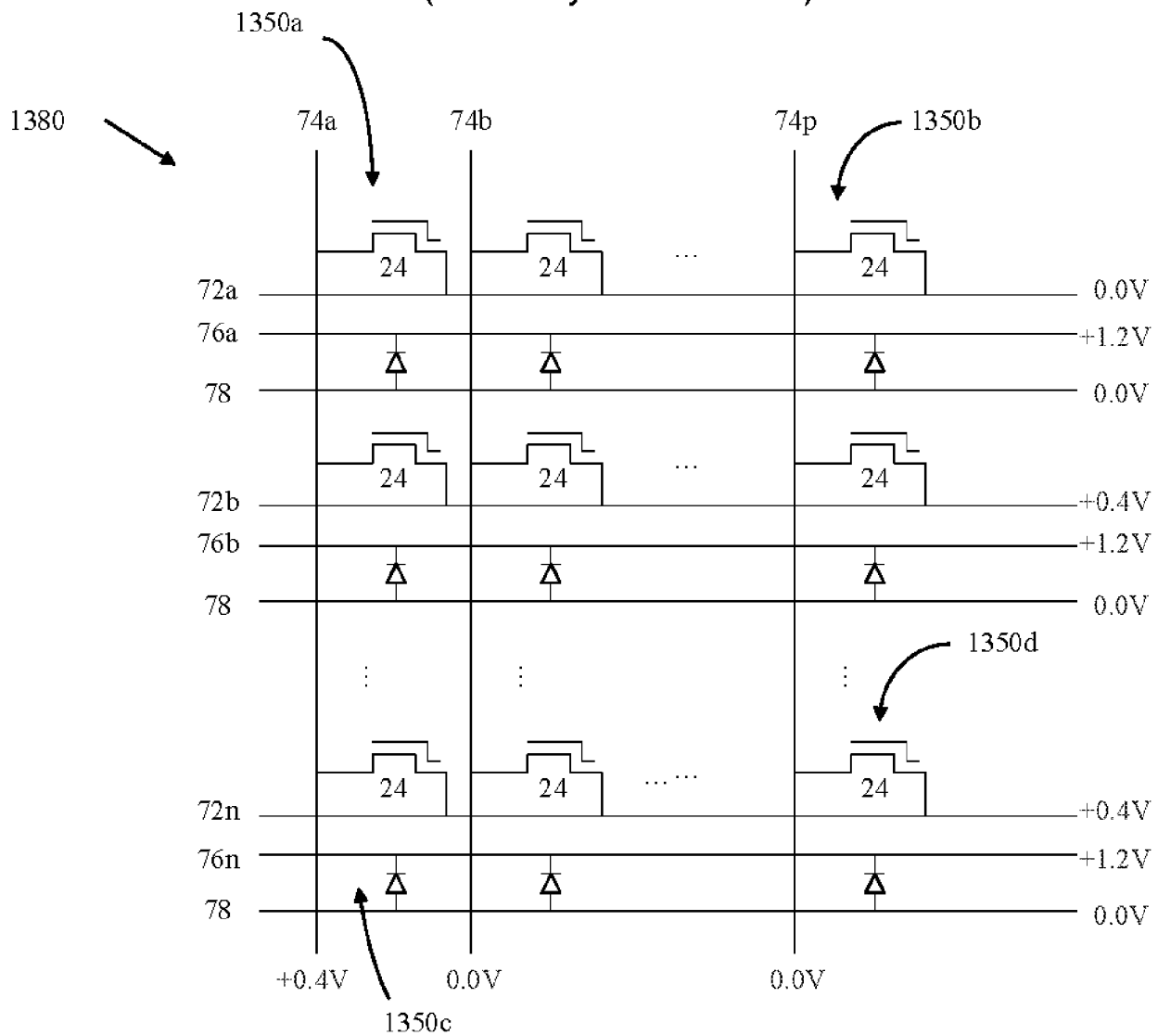


FIG. 190A

Read Operation, Active Source Line High (Memory Cell 1350a)

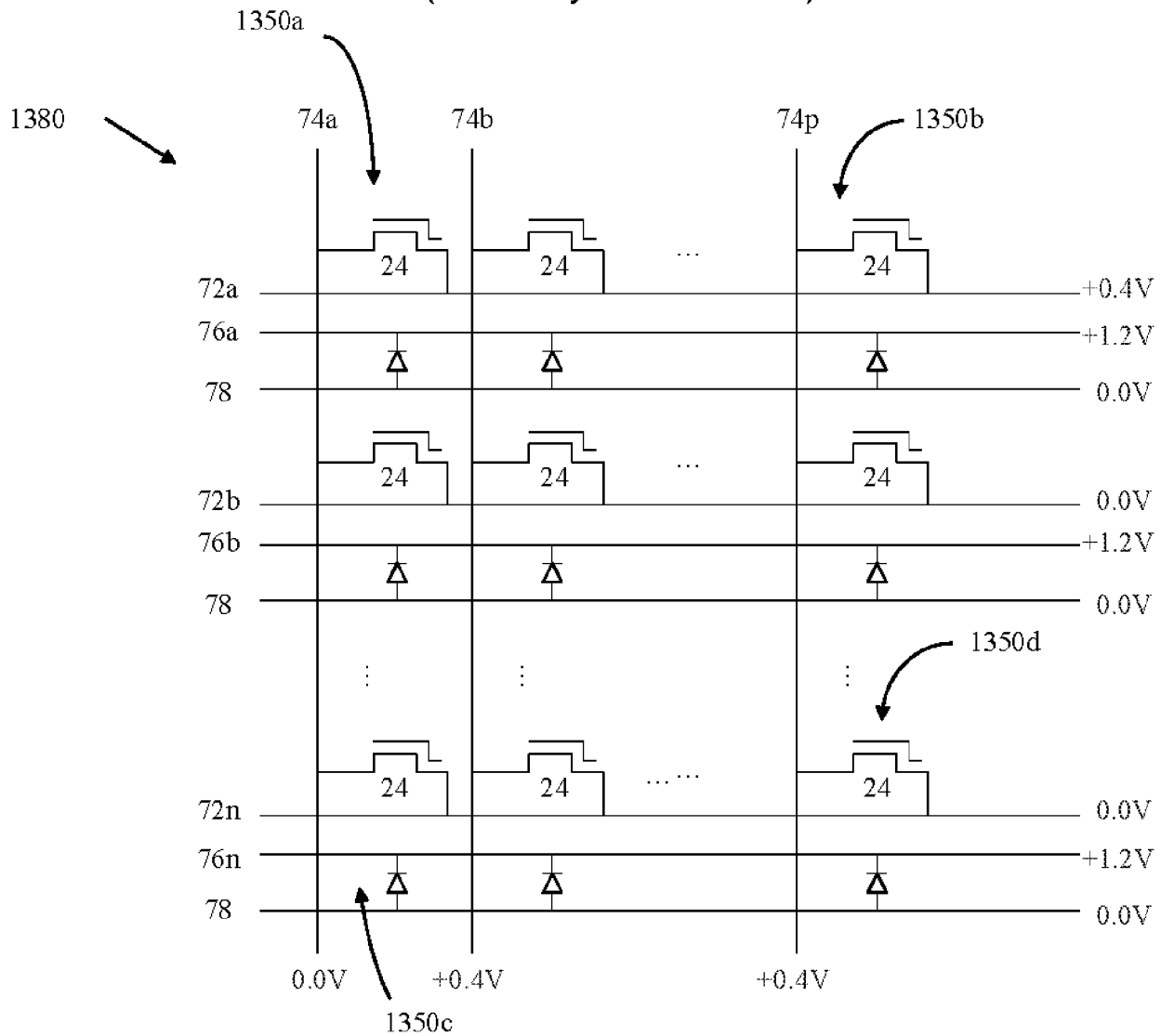


FIG. 190B

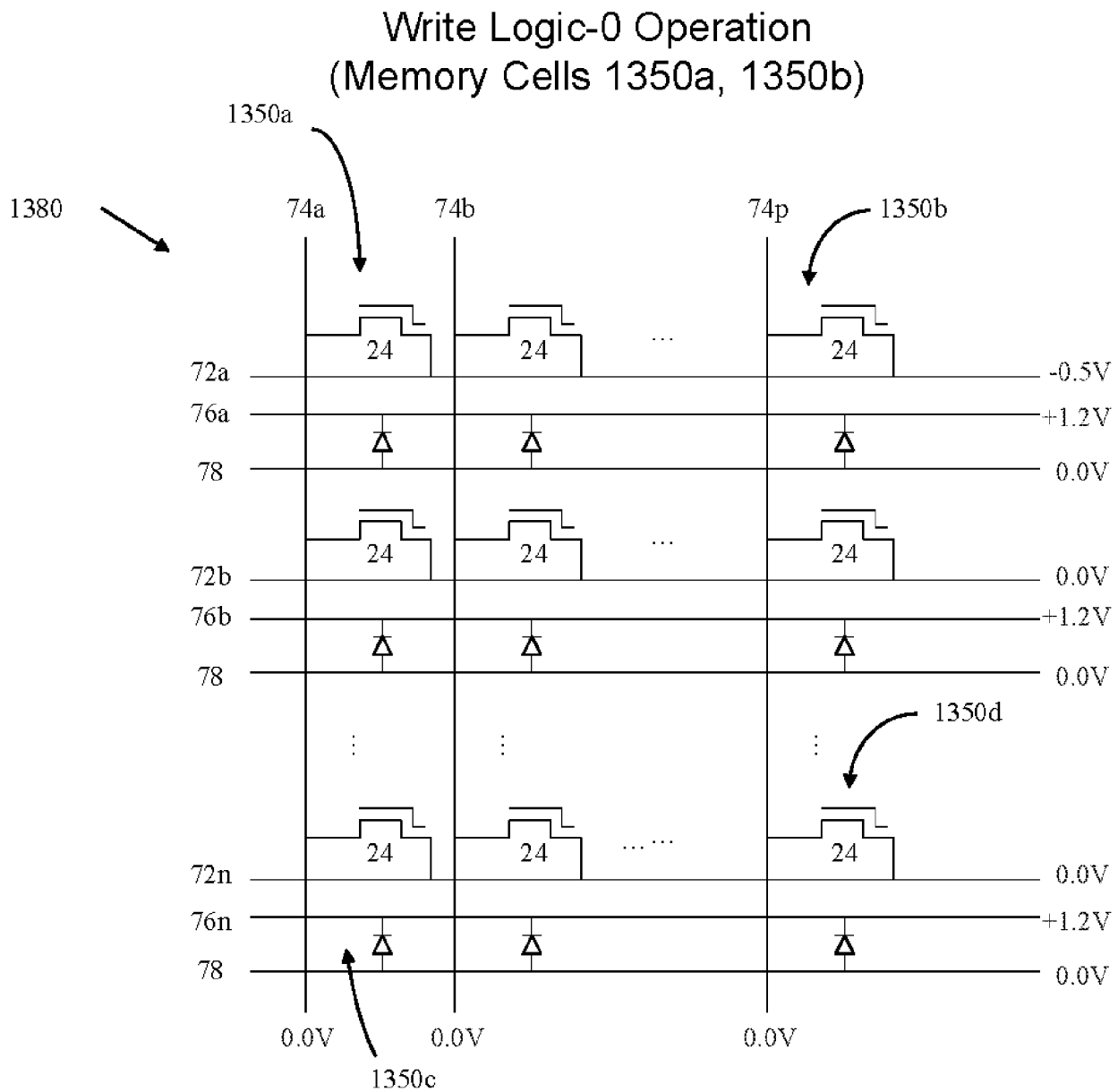


FIG. 191A

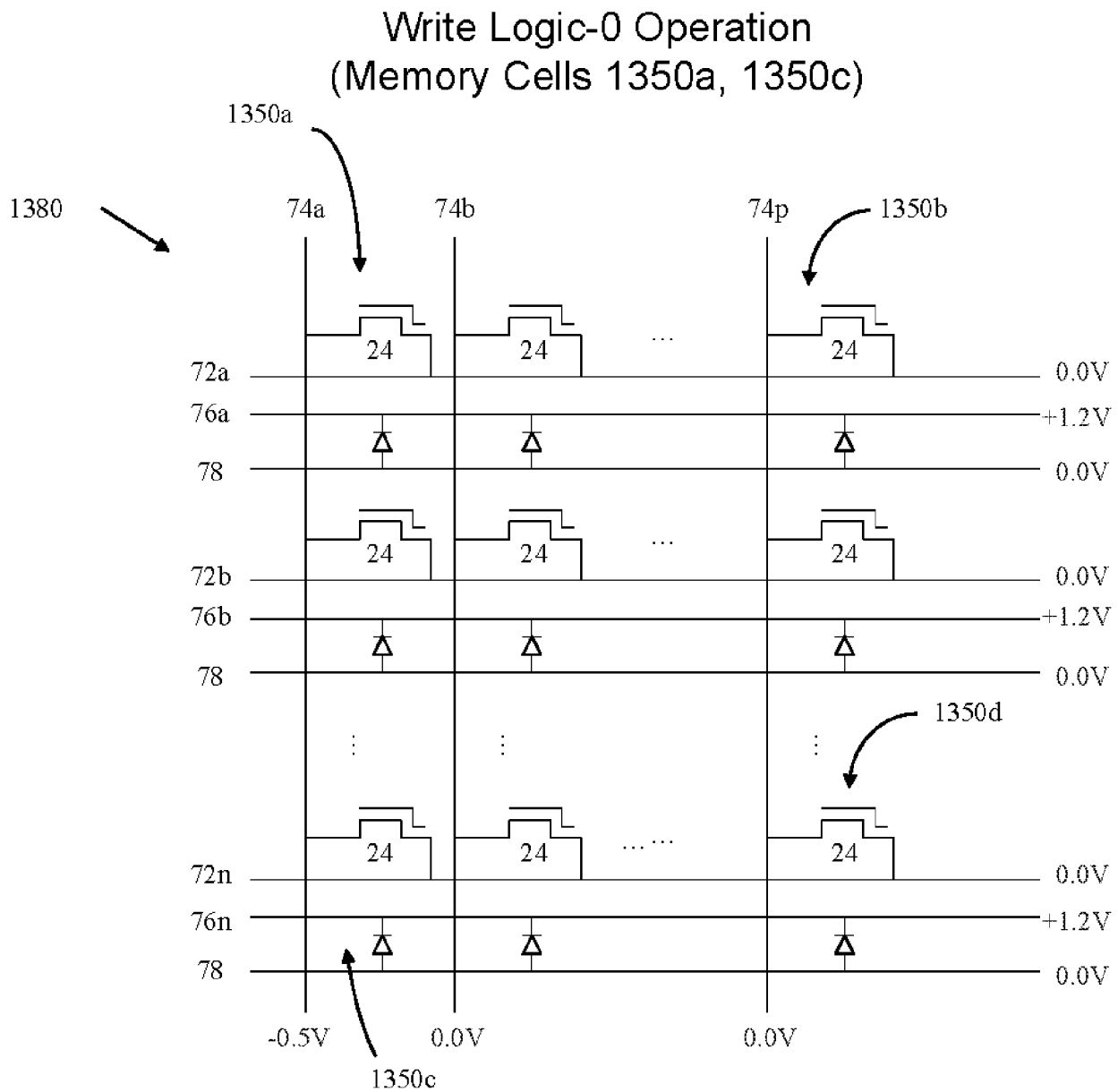


FIG. 191B

Write Logic-1 Operation, Active Bit Line High (Memory Cell 1350a)

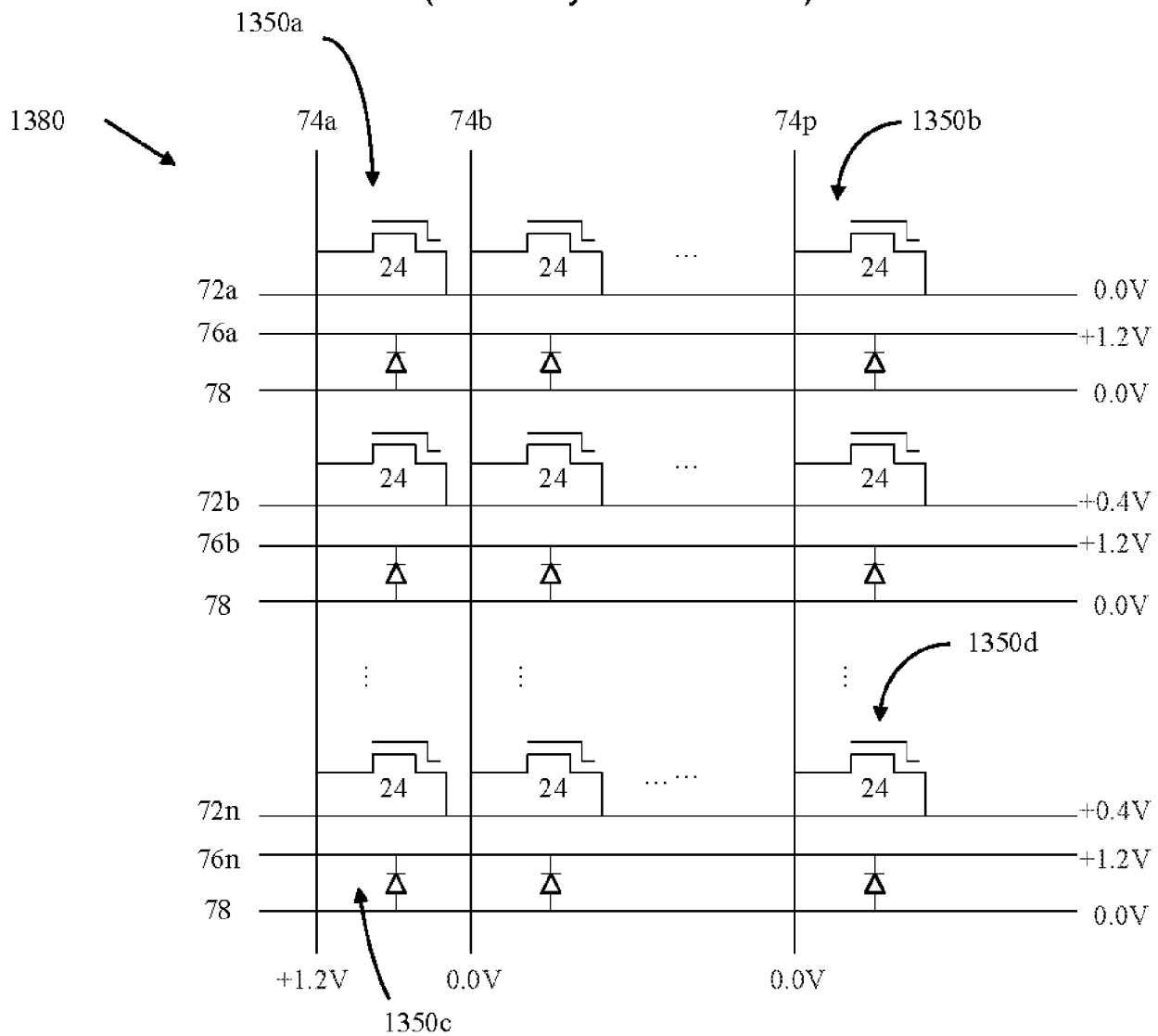


FIG. 192A

Write Logic-1 Operation, Active Source Line High (Memory Cell 1350a)

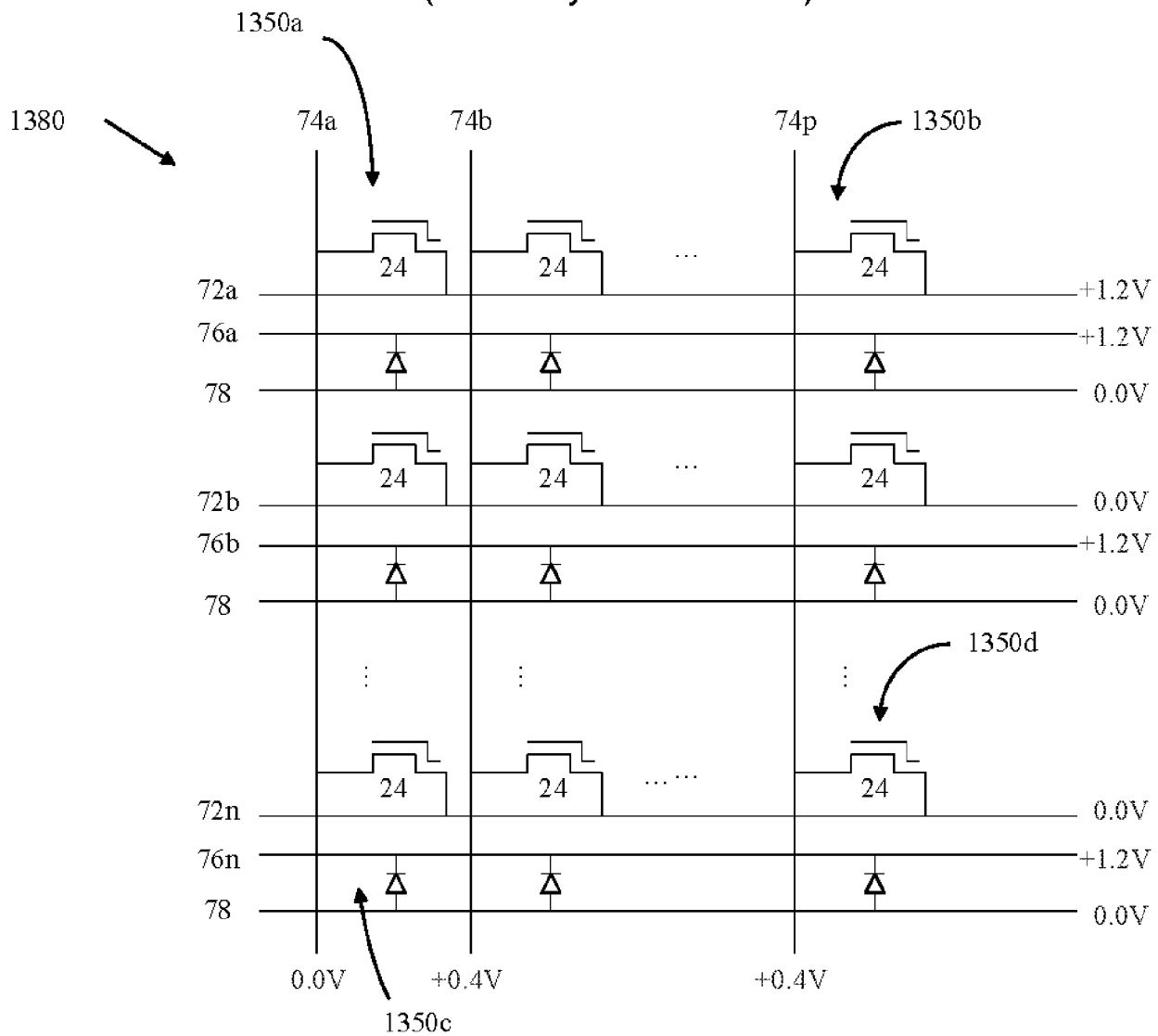


FIG. 192B

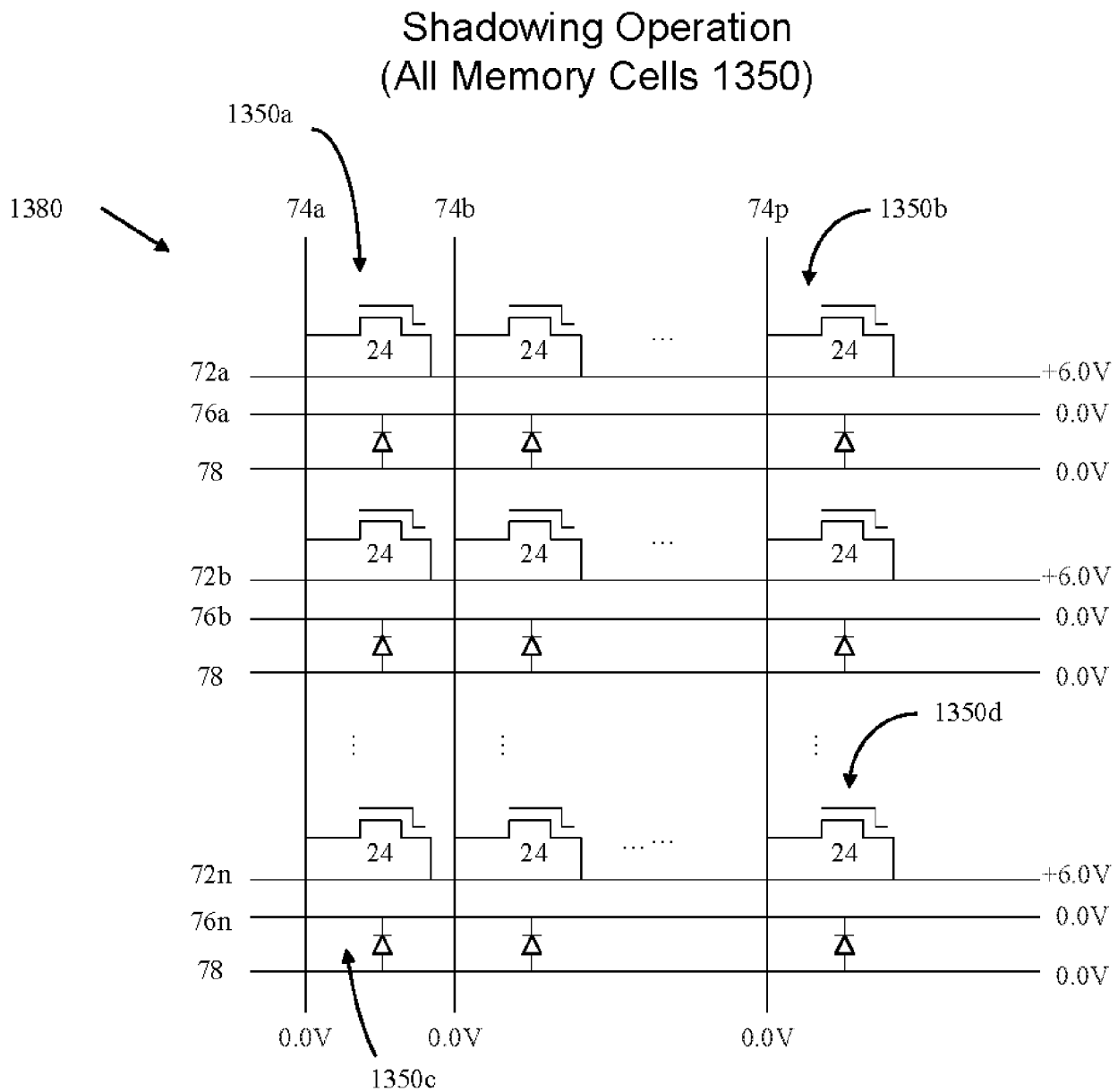


FIG. 193A

Restore Operation (All Memory Cells 1350)

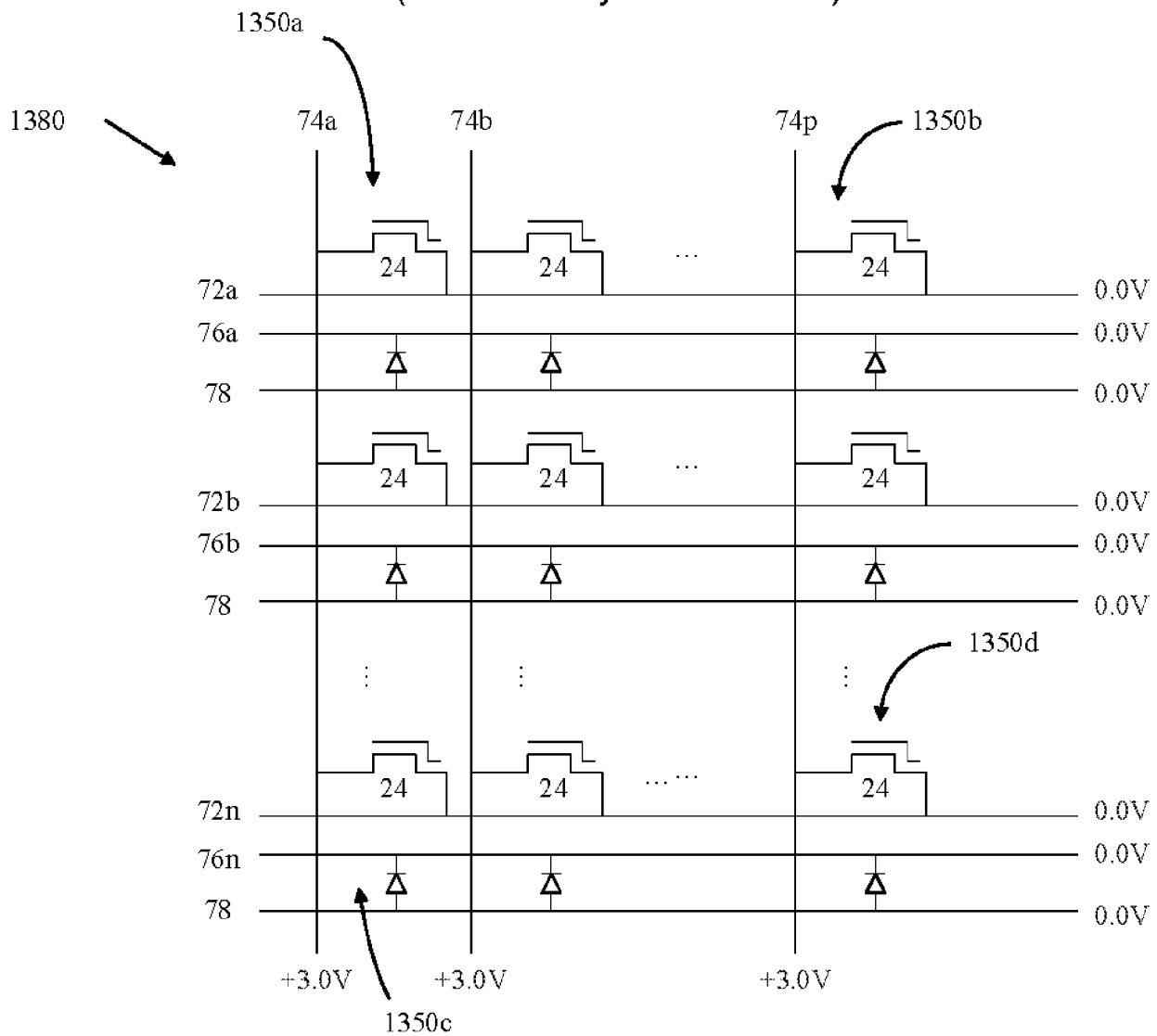


FIG. 194A

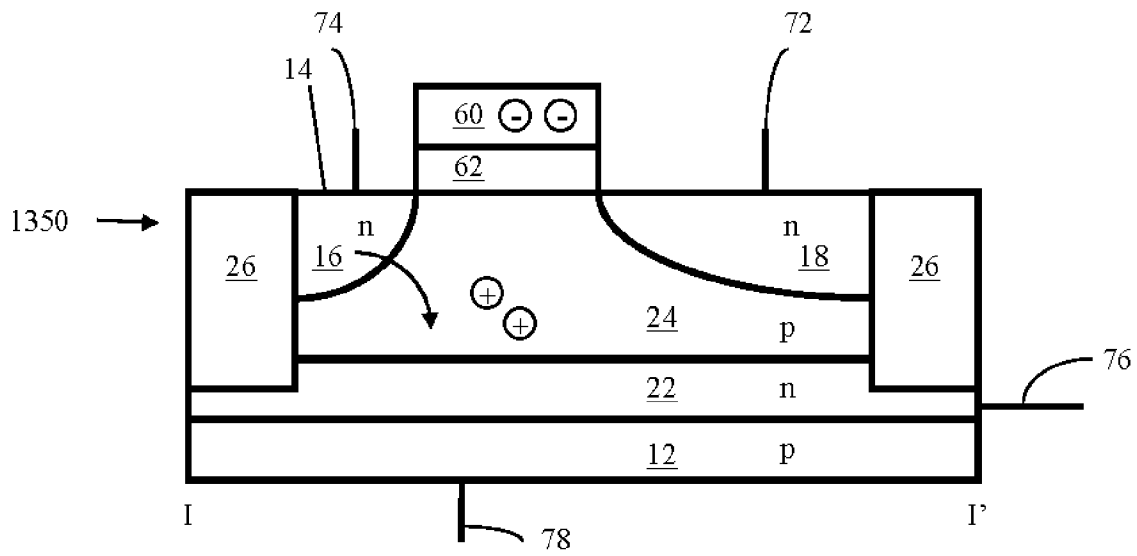


FIG. 194B

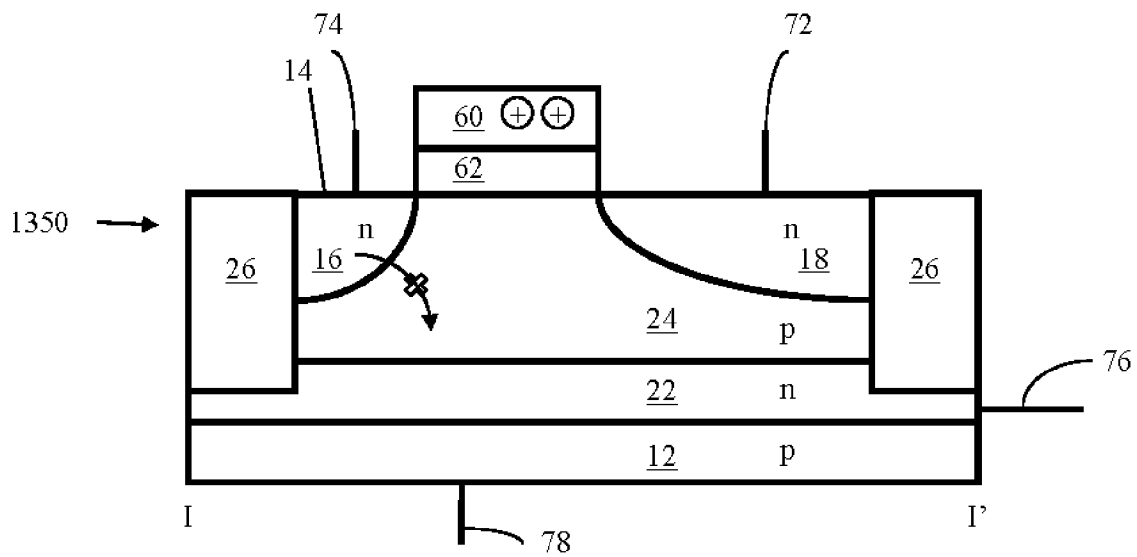


FIG. 194C

Reset Operation (All Memory Cells 1350)

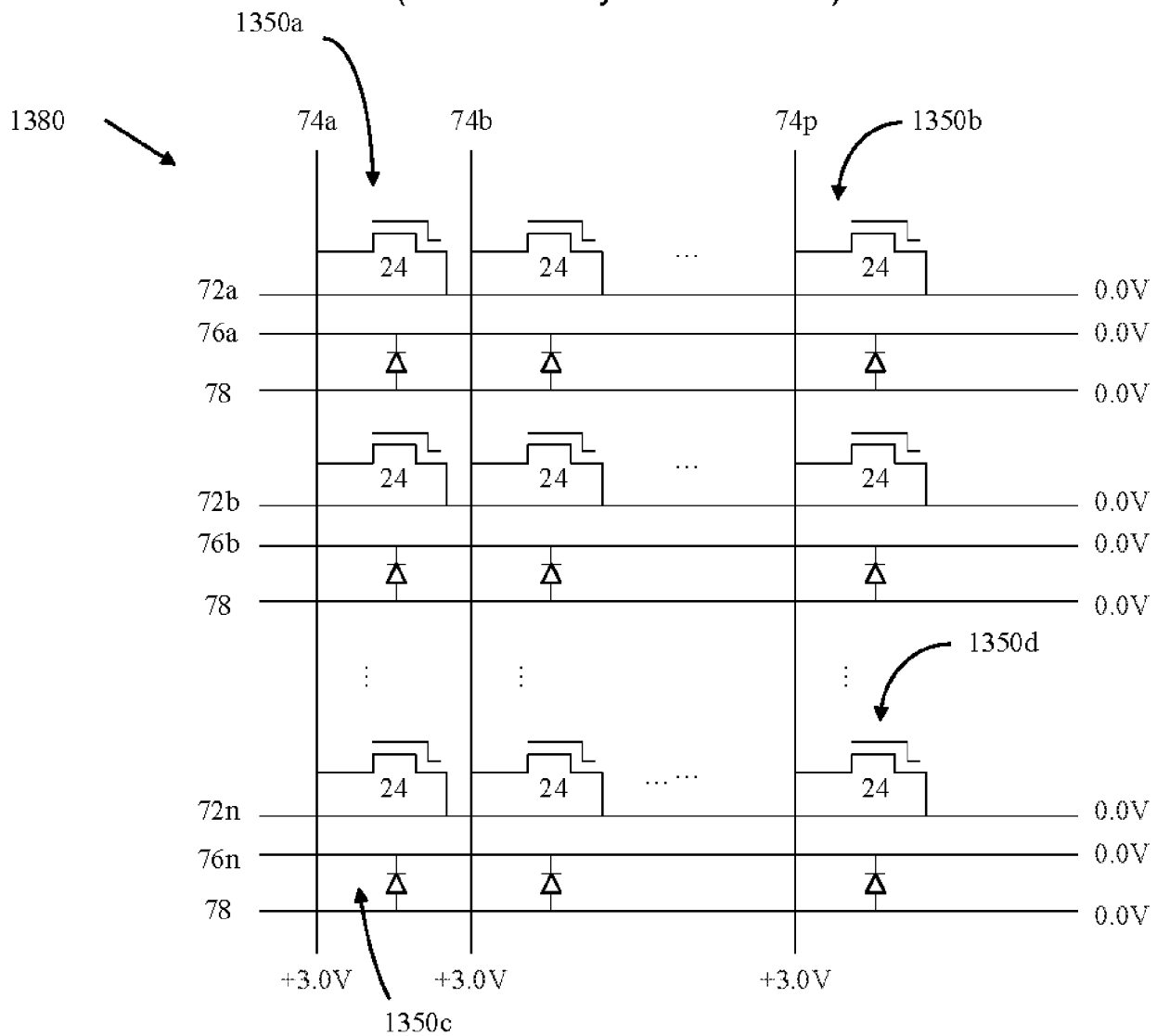


FIG. 195

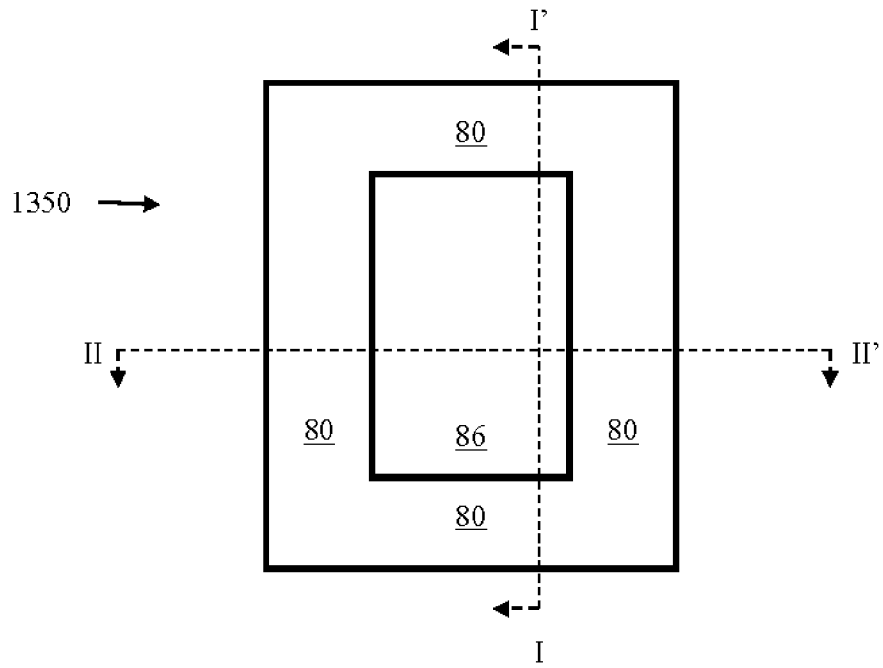


FIG. 196A

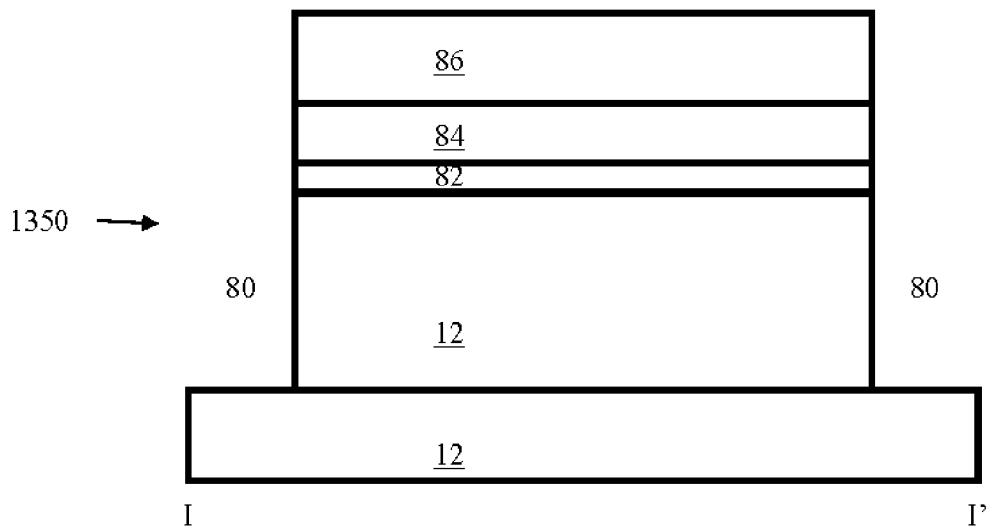


FIG. 196B

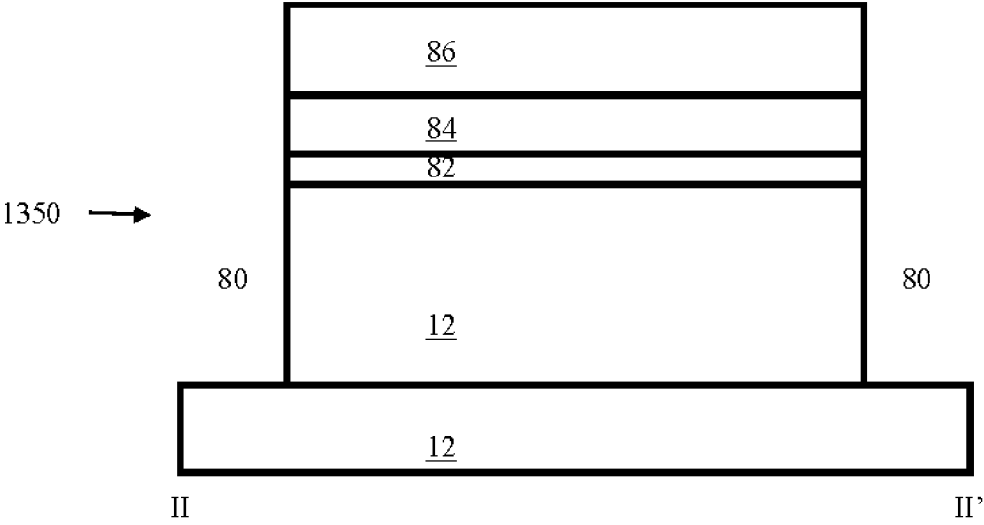


FIG. 196C

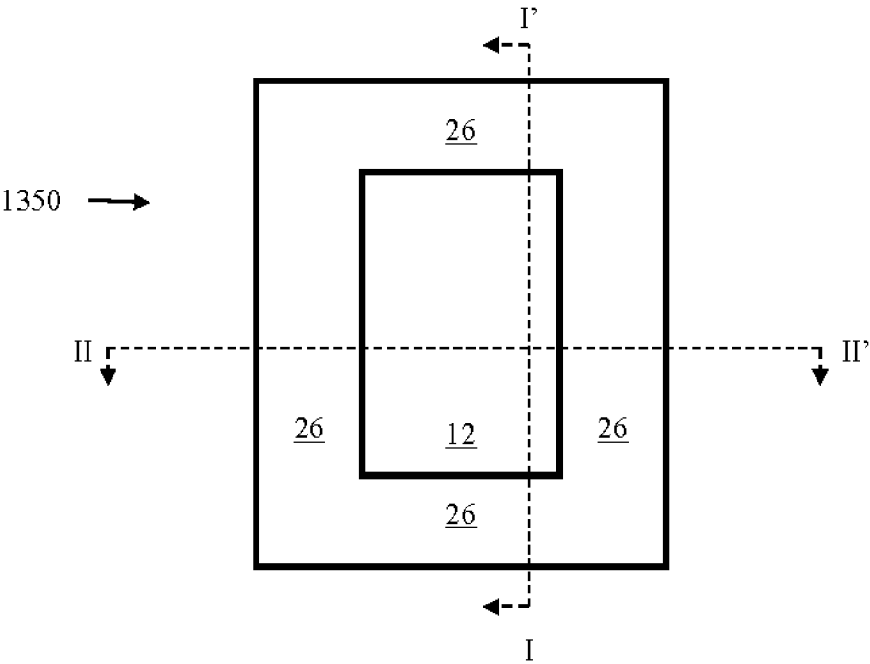


FIG. 196D

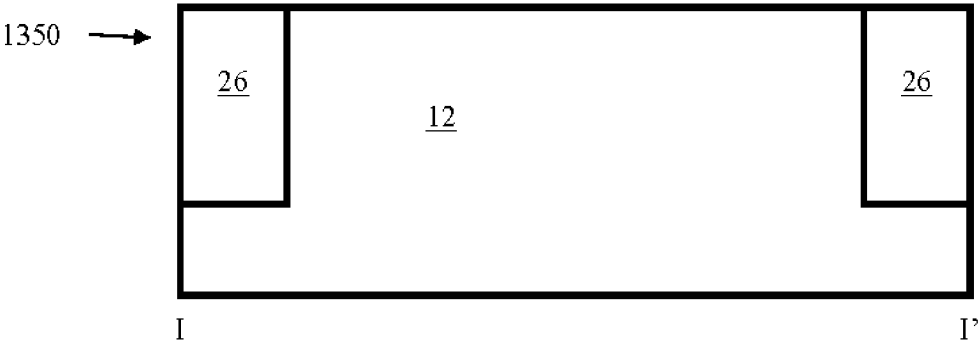


FIG. 196E

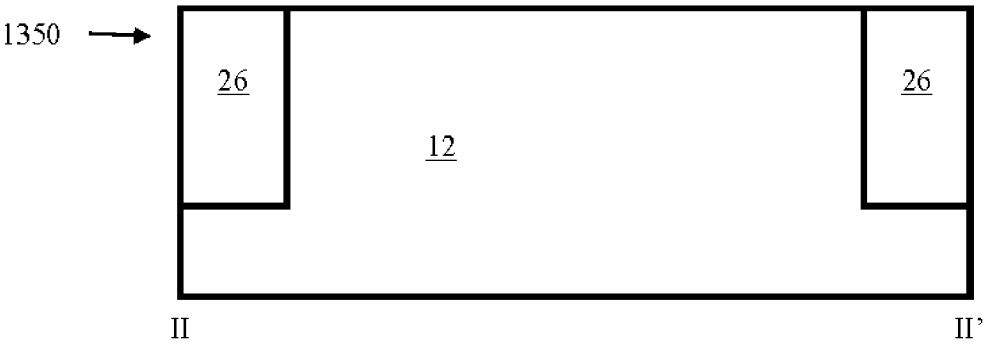


FIG. 196F

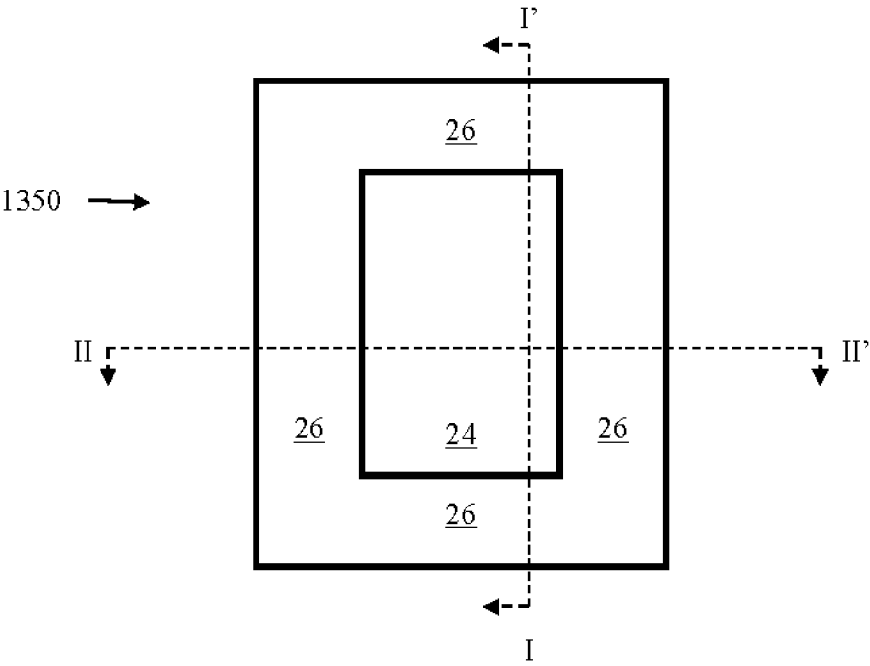


FIG. 196G

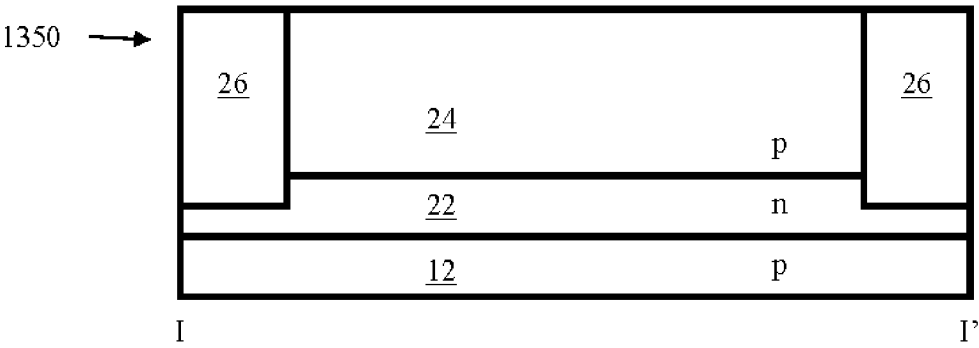


FIG. 196H

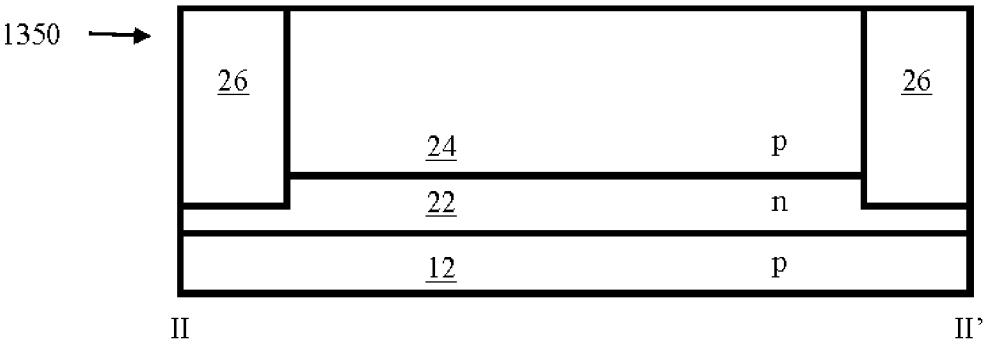


FIG. 196I

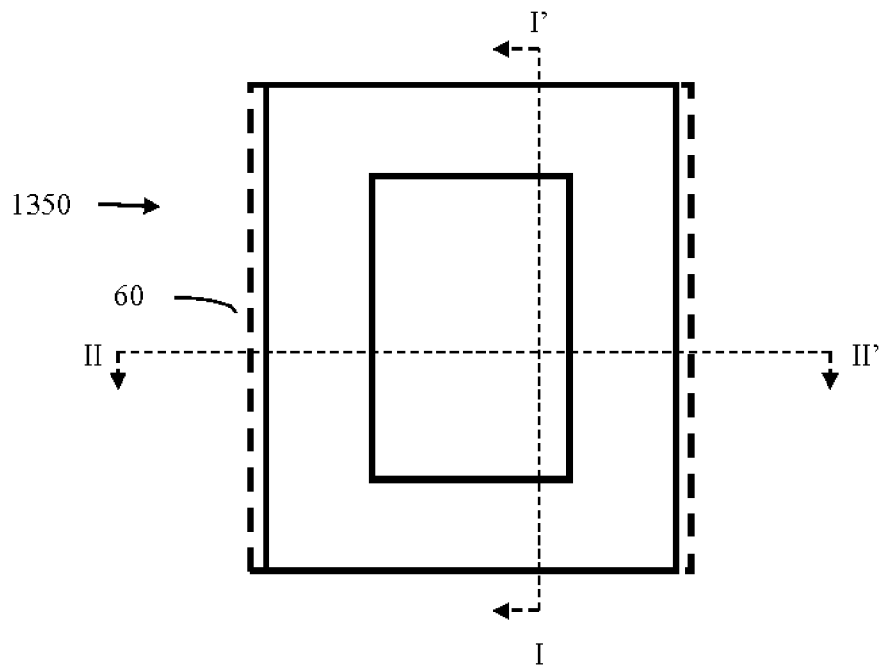


FIG. 196J

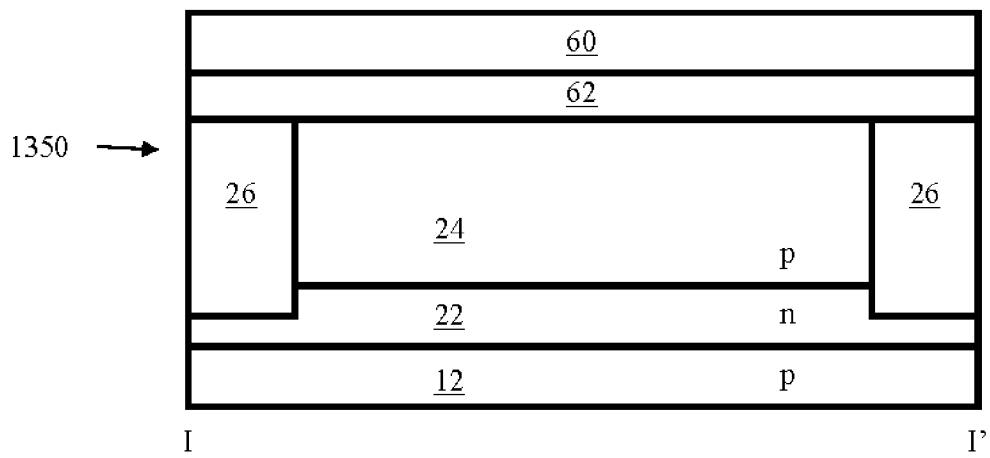


FIG. 196K

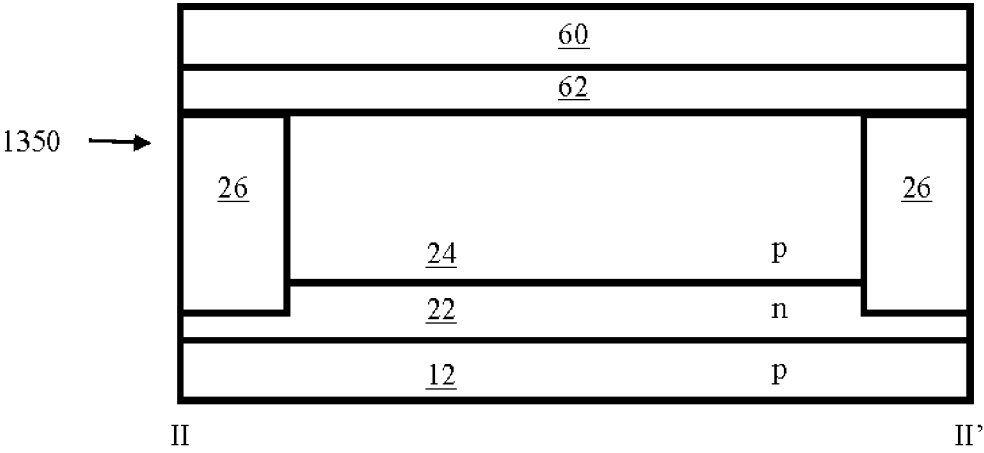


FIG. 196L

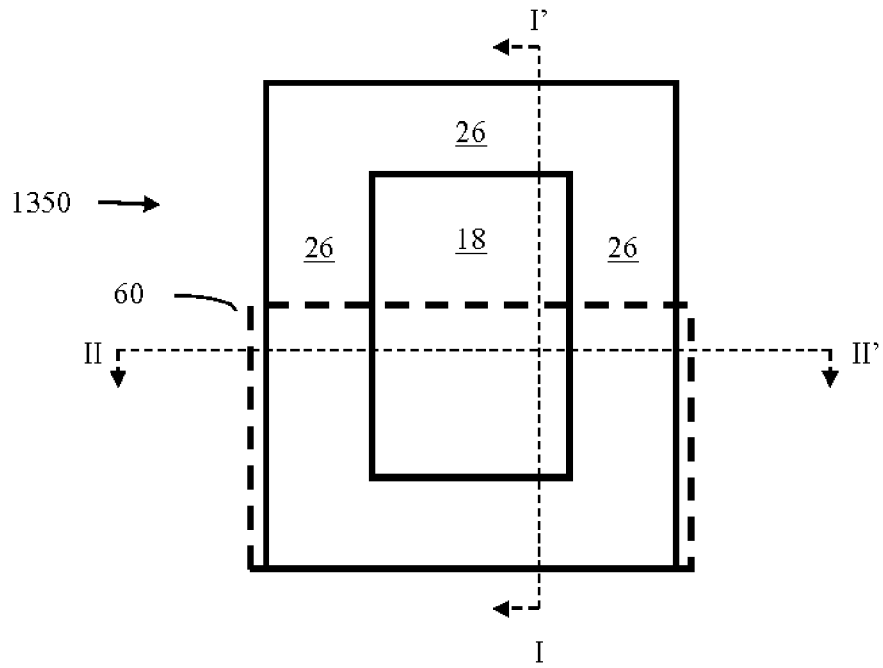


FIG. 196M

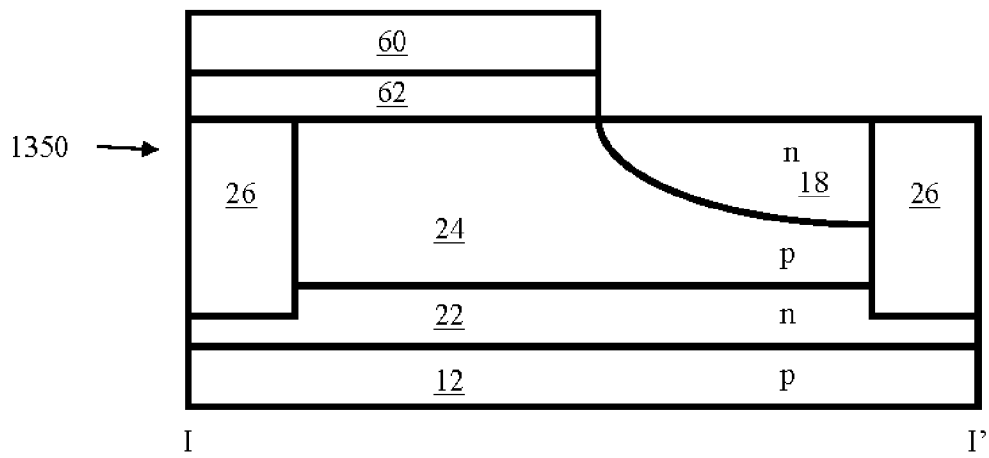


FIG. 196N

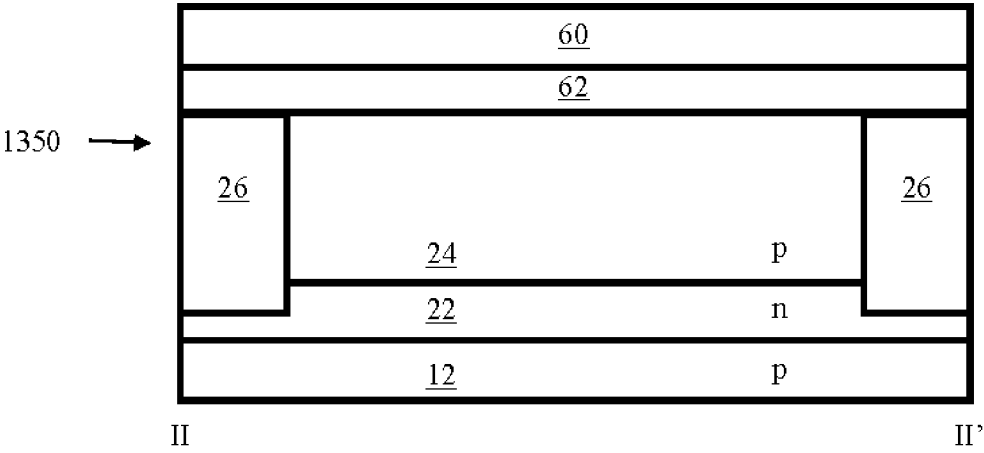


FIG. 196O

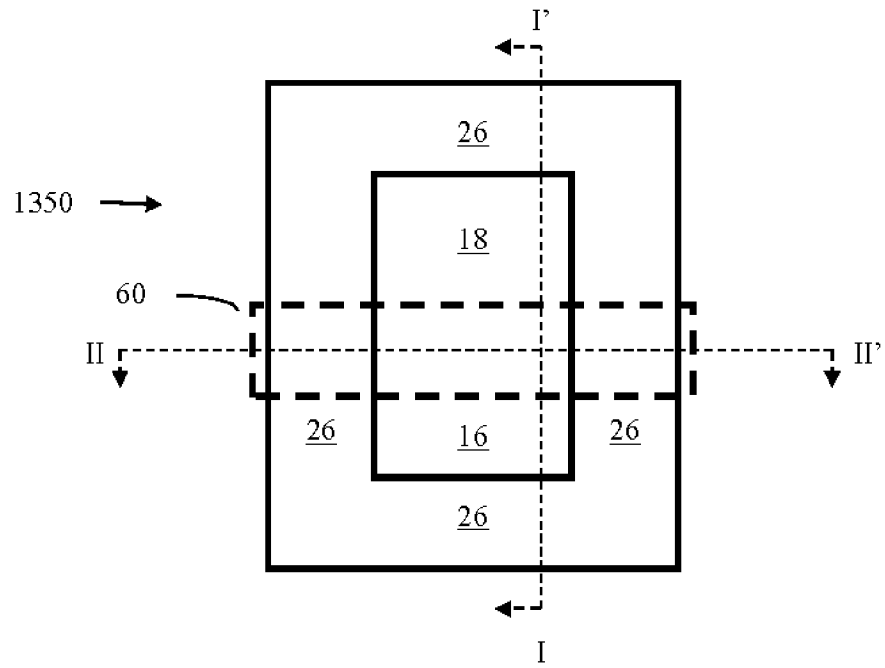


FIG. 196P

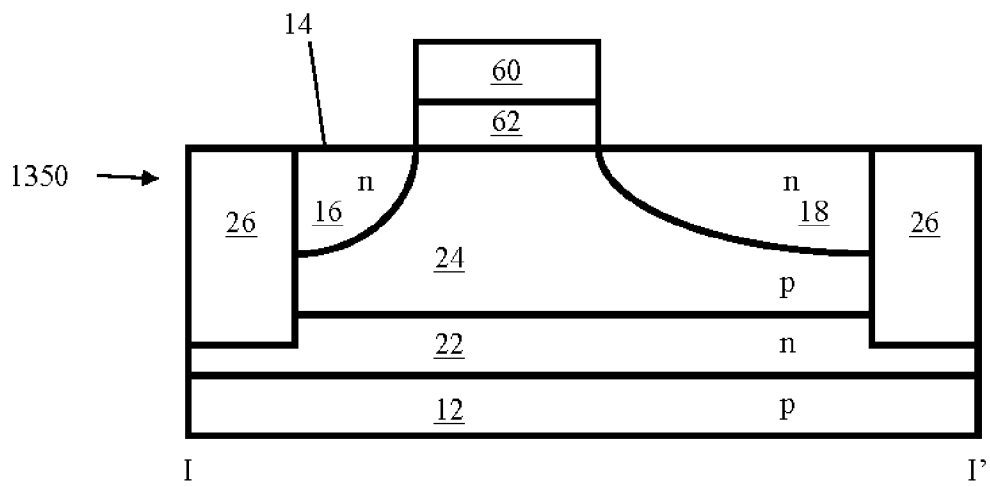


FIG. 196Q

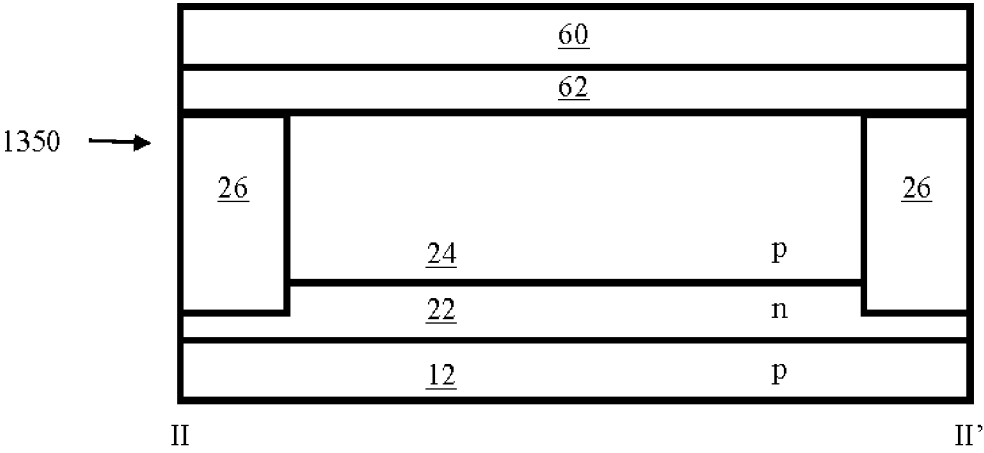


FIG. 196R

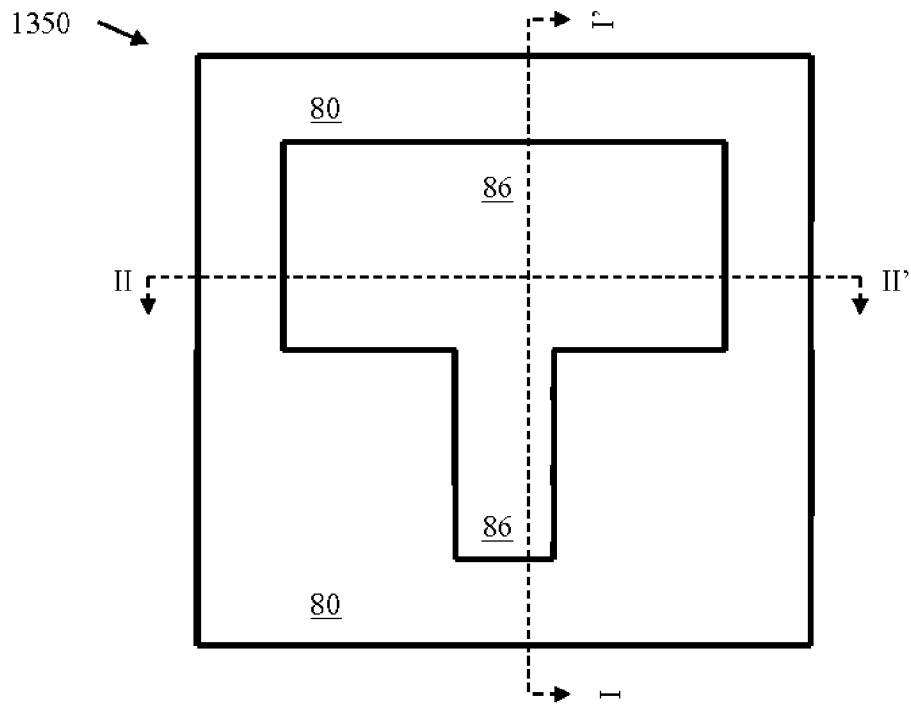


FIG. 197A

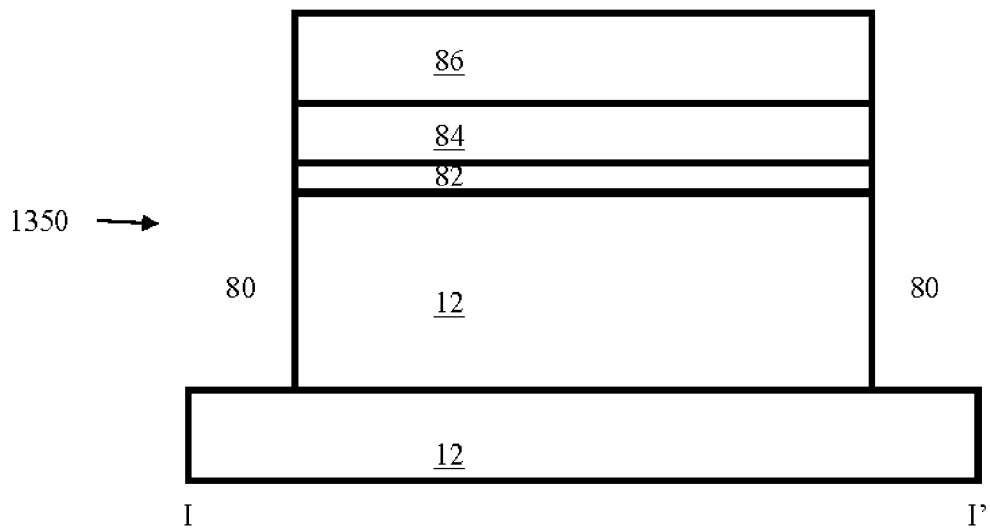


FIG. 197B

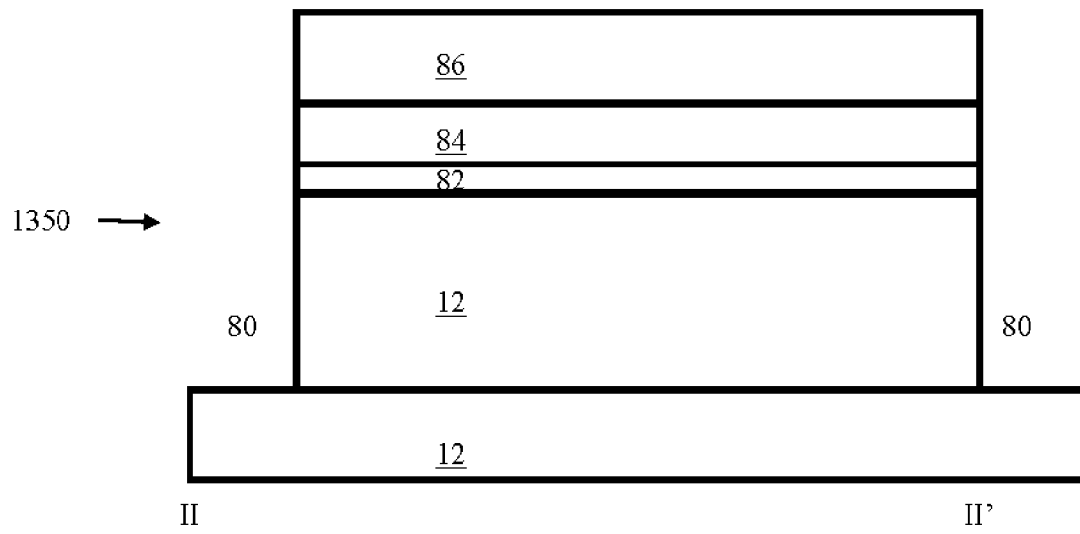


FIG. 197C

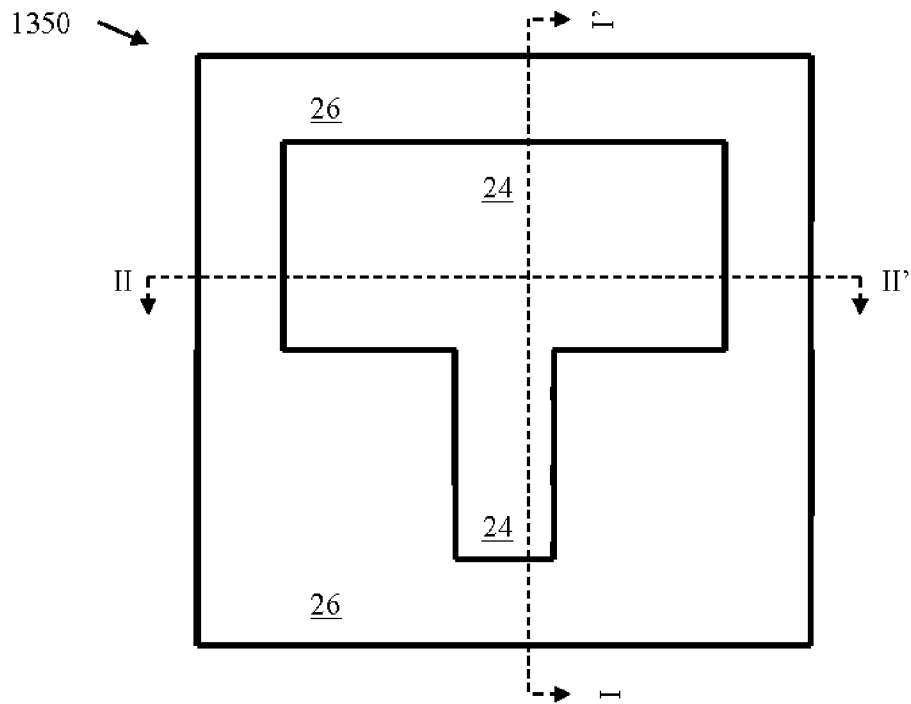


FIG. 197D

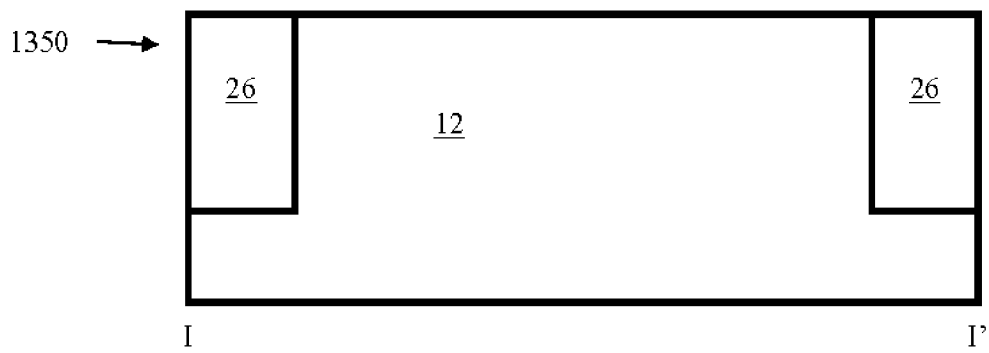


FIG. 197E

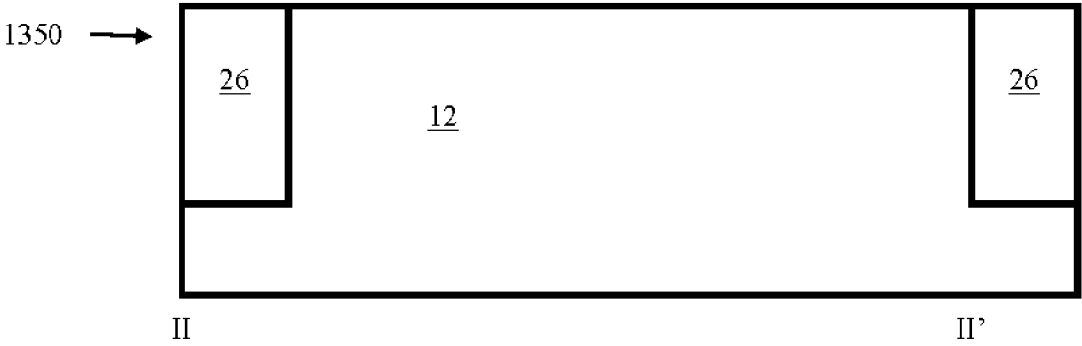


FIG. 197F

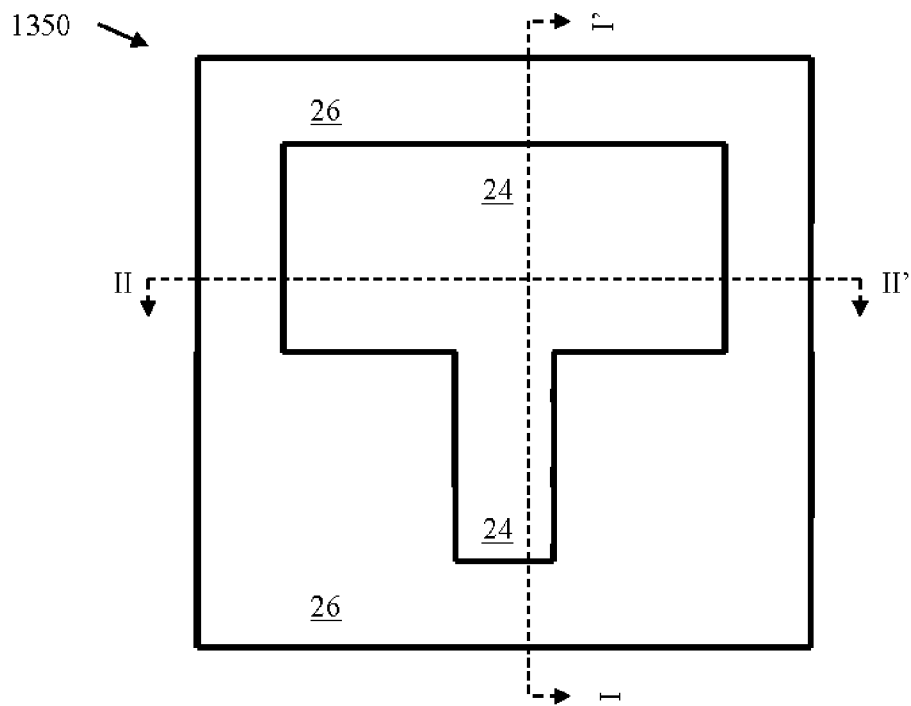


FIG. 197G

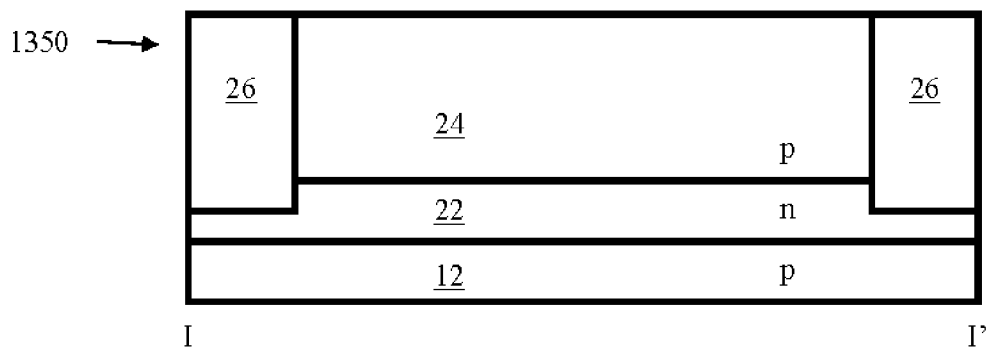


FIG. 197H

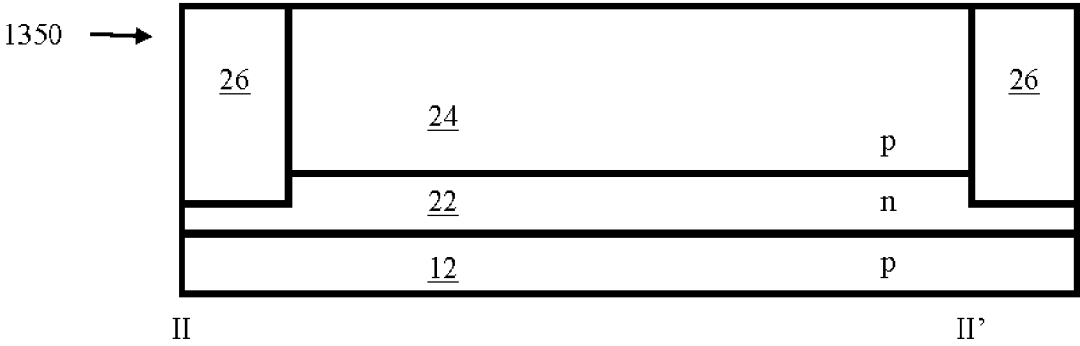


FIG. 197I

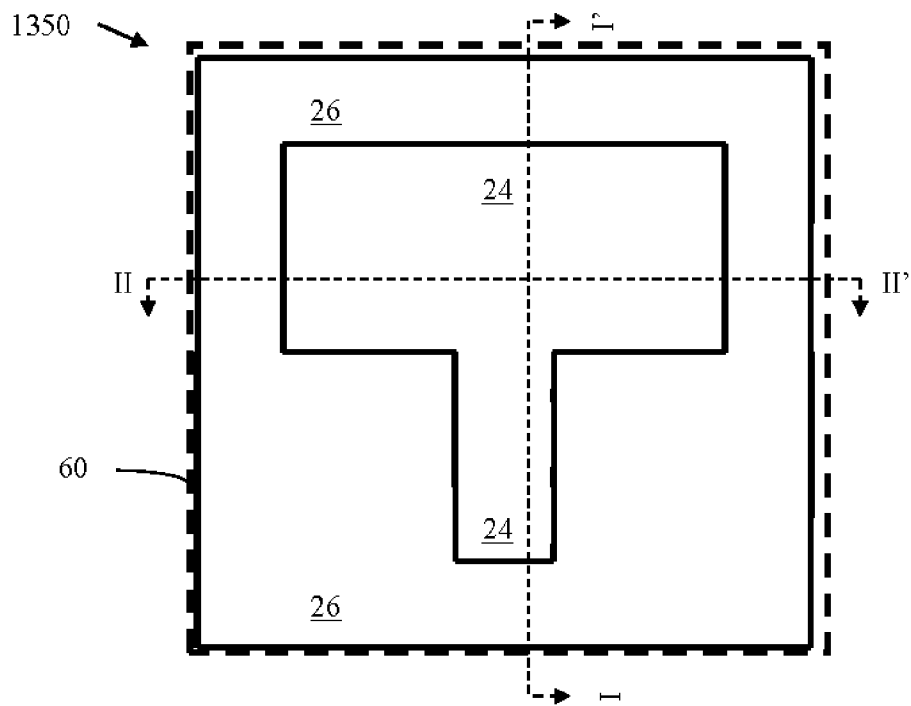


FIG. 197J

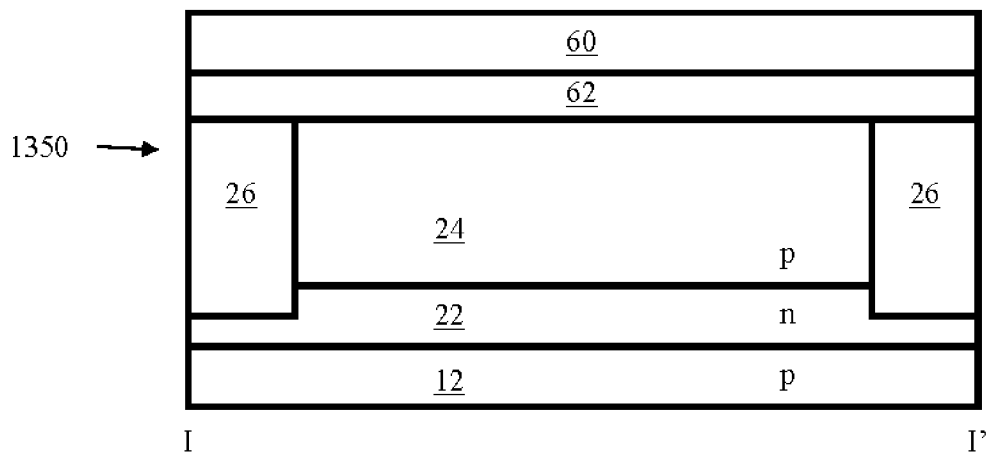


FIG. 197K

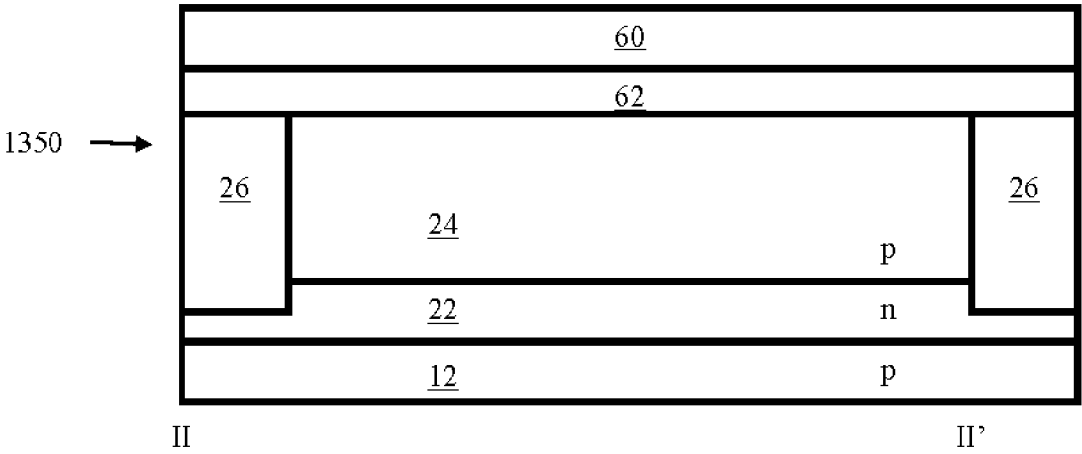


FIG. 197L

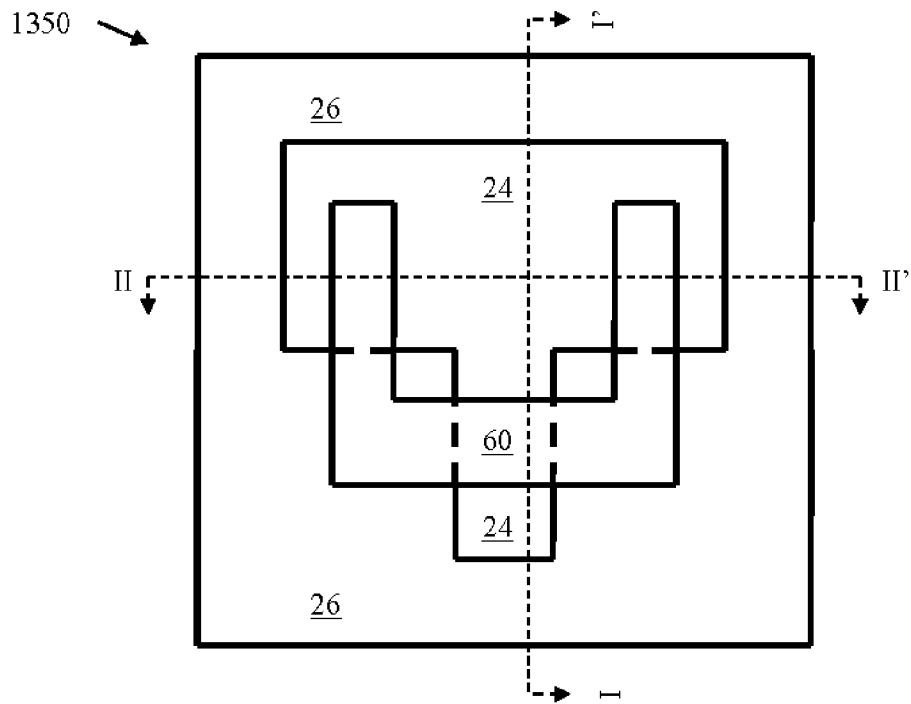


FIG. 197M

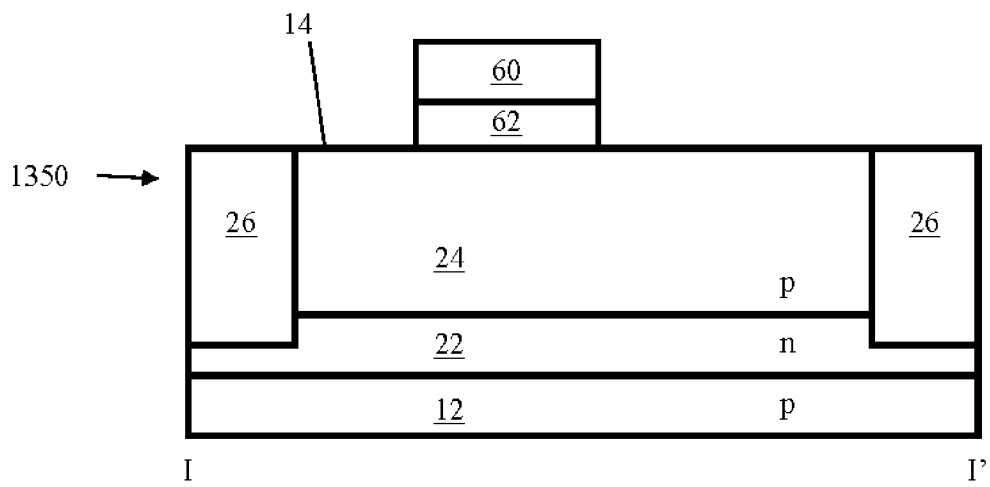


FIG. 197N

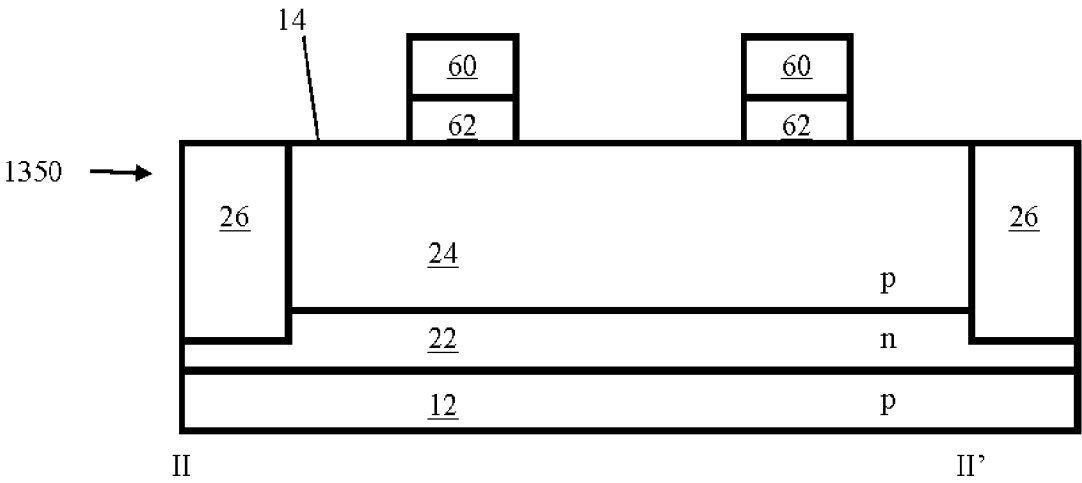


FIG. 197O

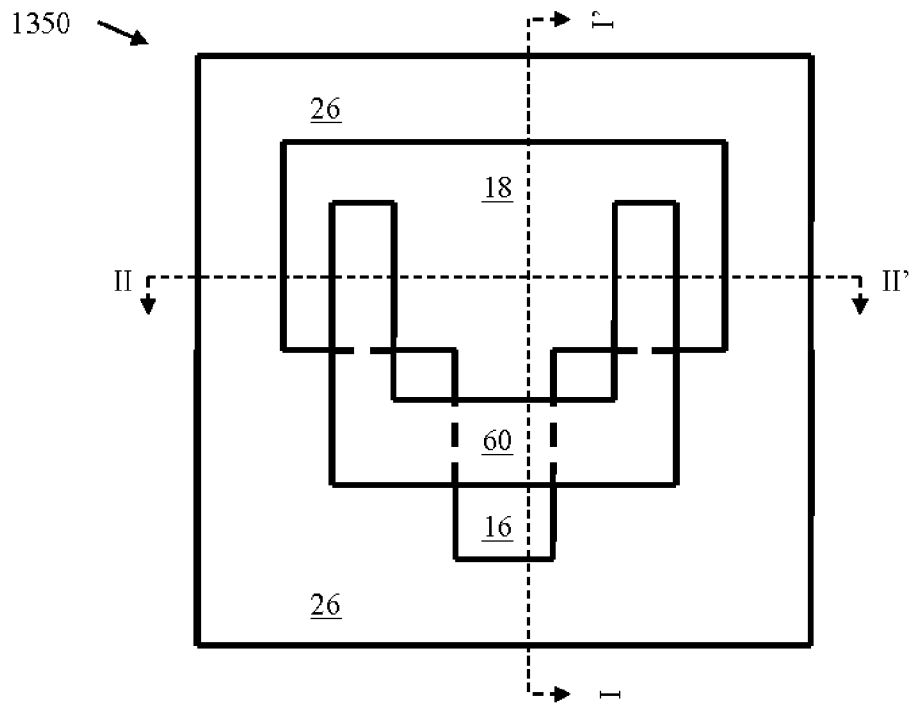


FIG. 197P

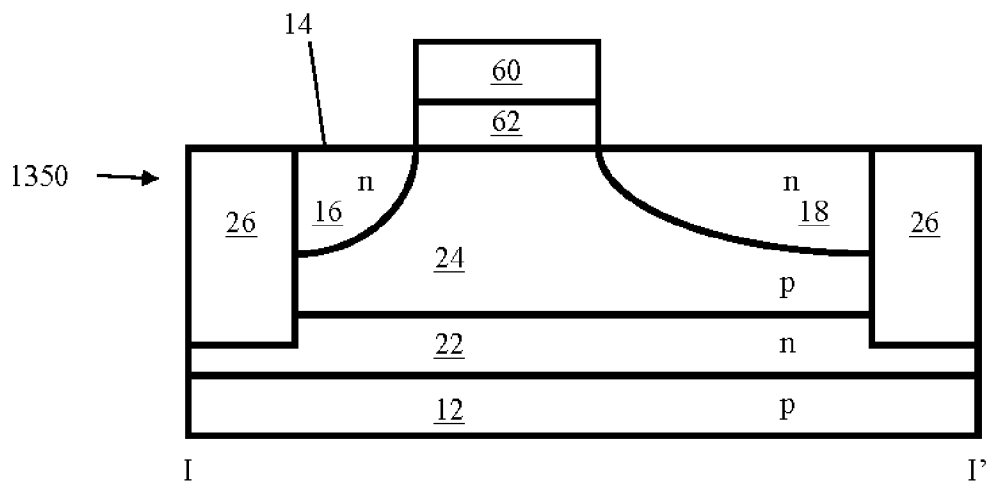


FIG. 197Q

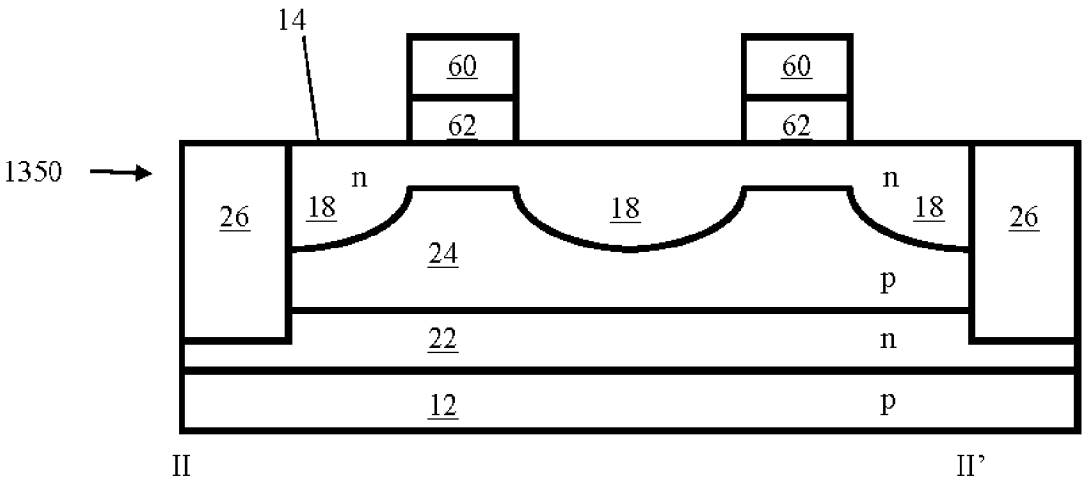


FIG. 197R

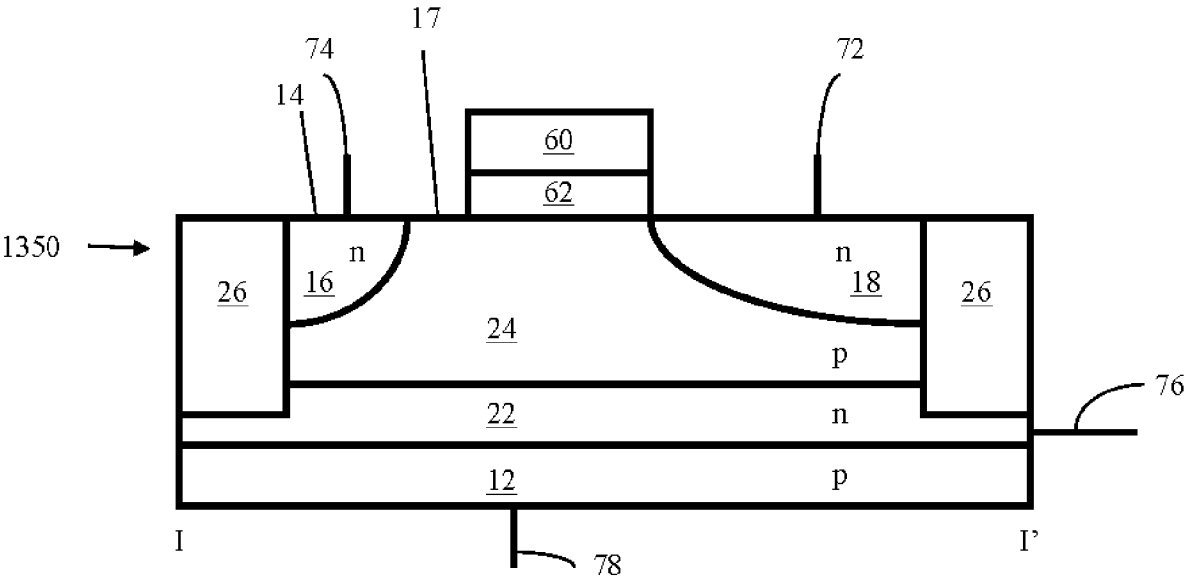


FIG. 198

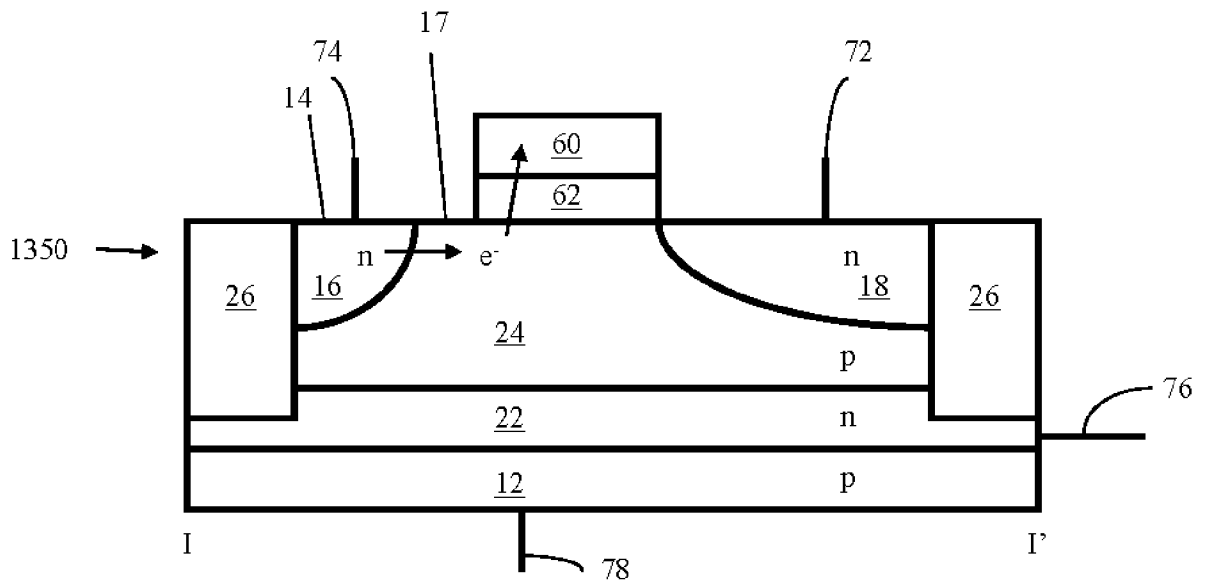


FIG. 199A

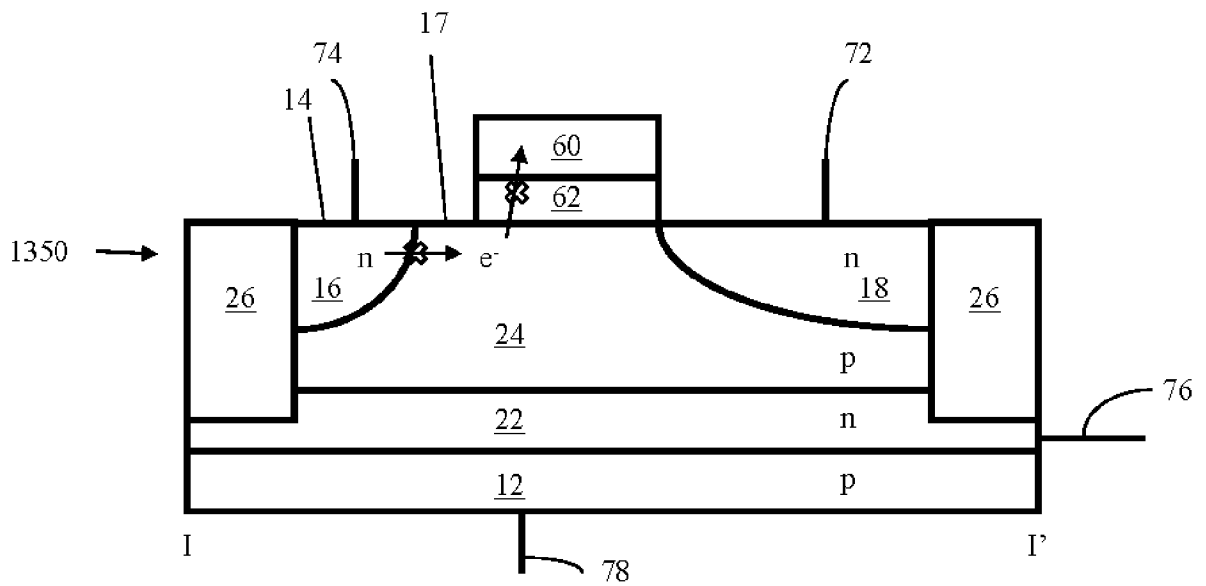


FIG. 199B

Restore Operation (All Memory Cells 1350)

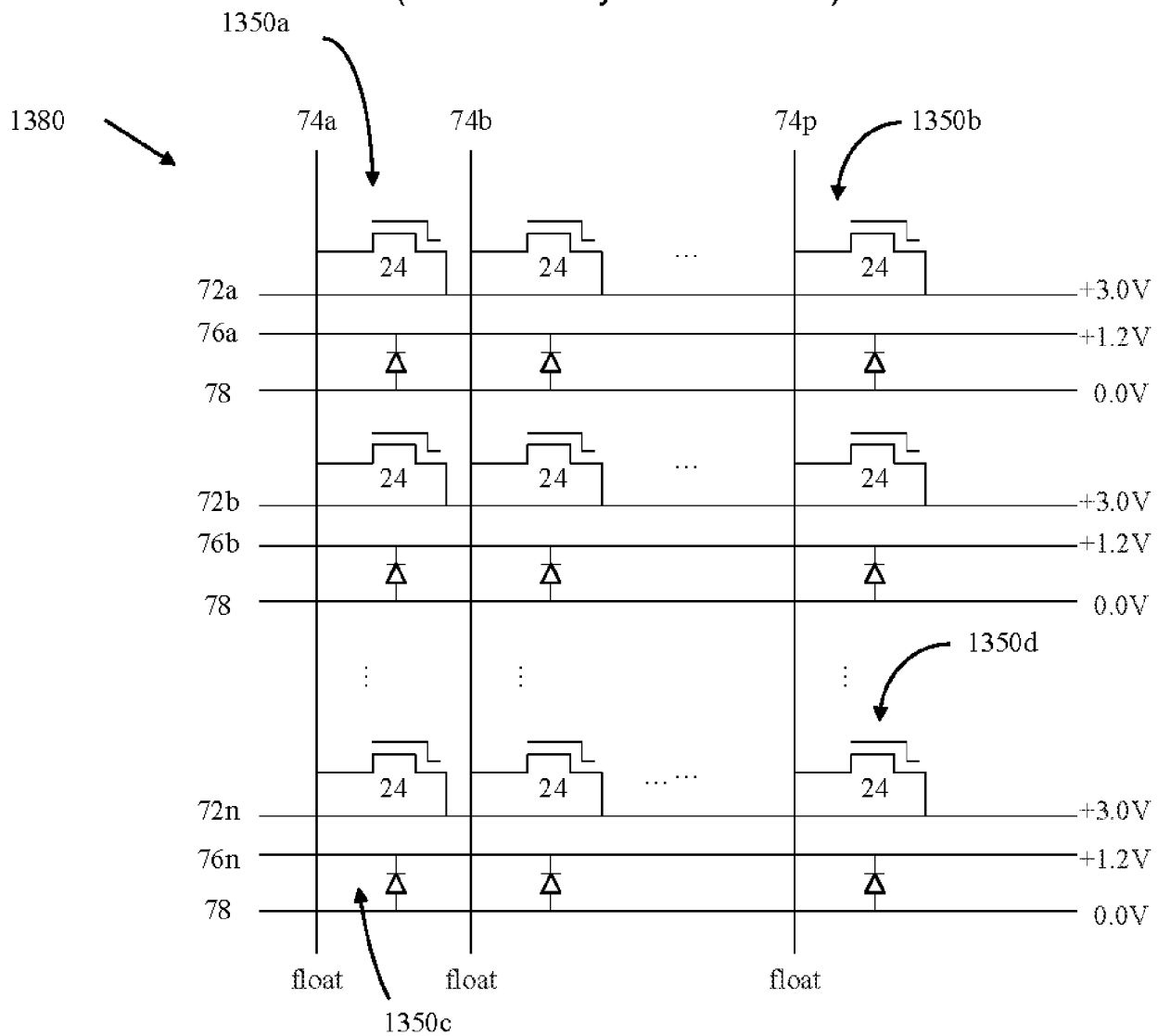


FIG. 200A

Reset Operation (All Memory Cells 1350)

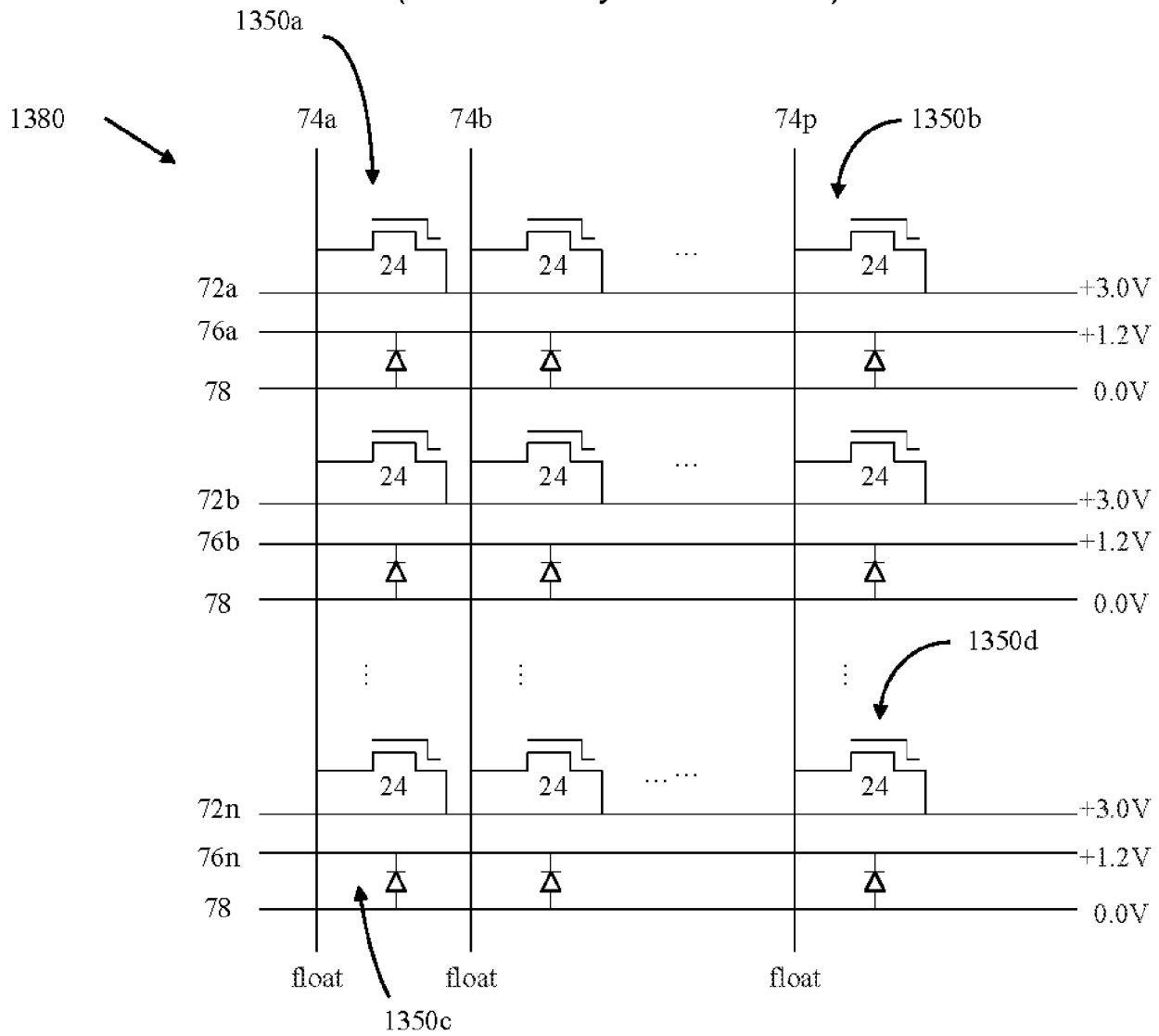


FIG. 201

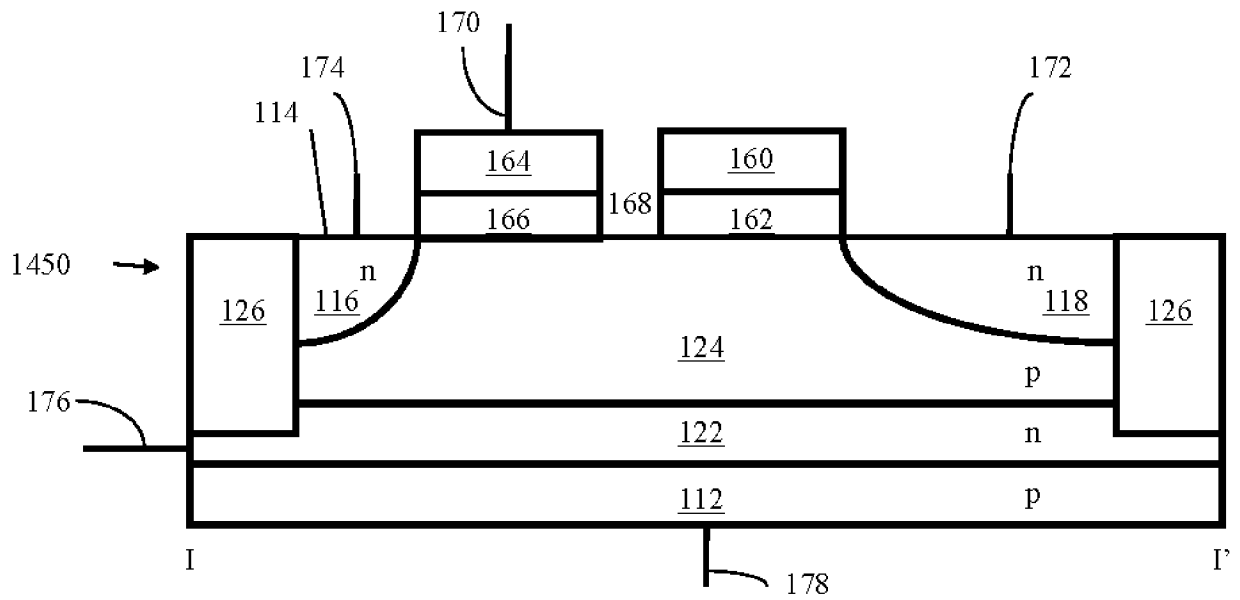


FIG. 202A

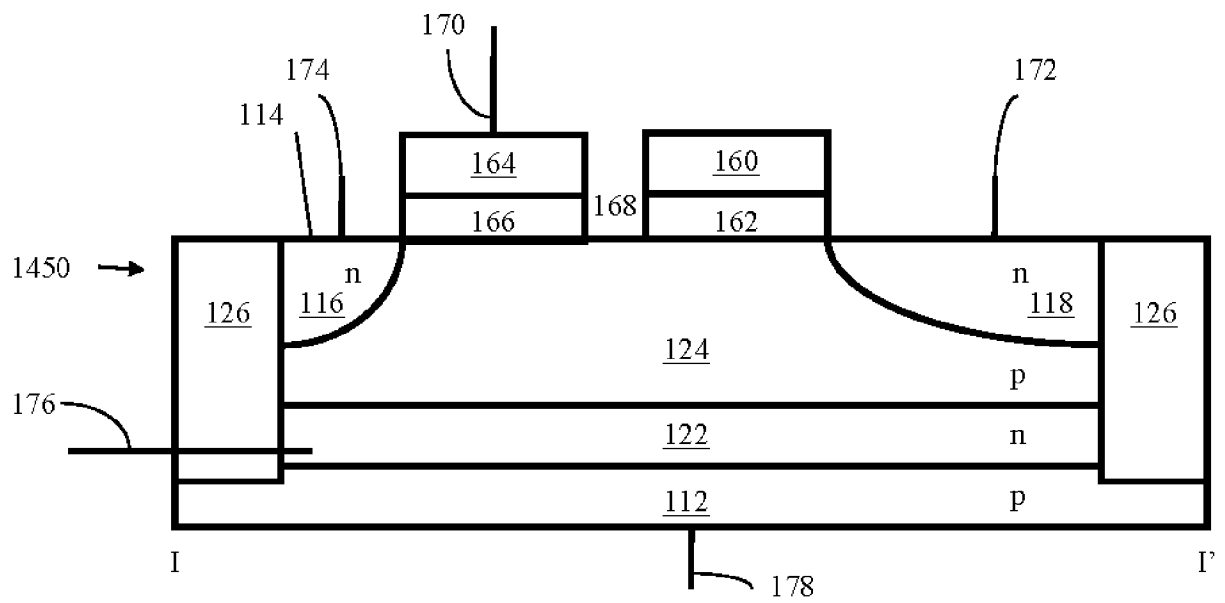


FIG. 202B

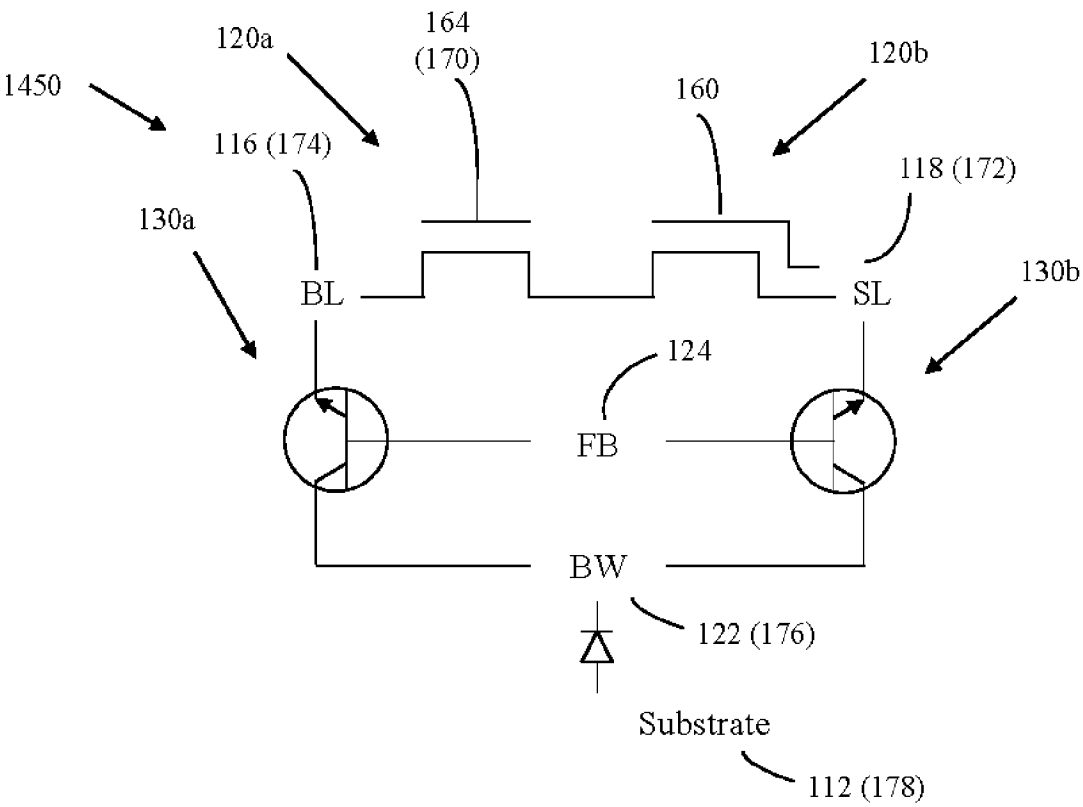


FIG. 203

Exemplary Memory Array 1480 with
Representative Memory Cells 1450a, 1450b, 1450c
and 1450d

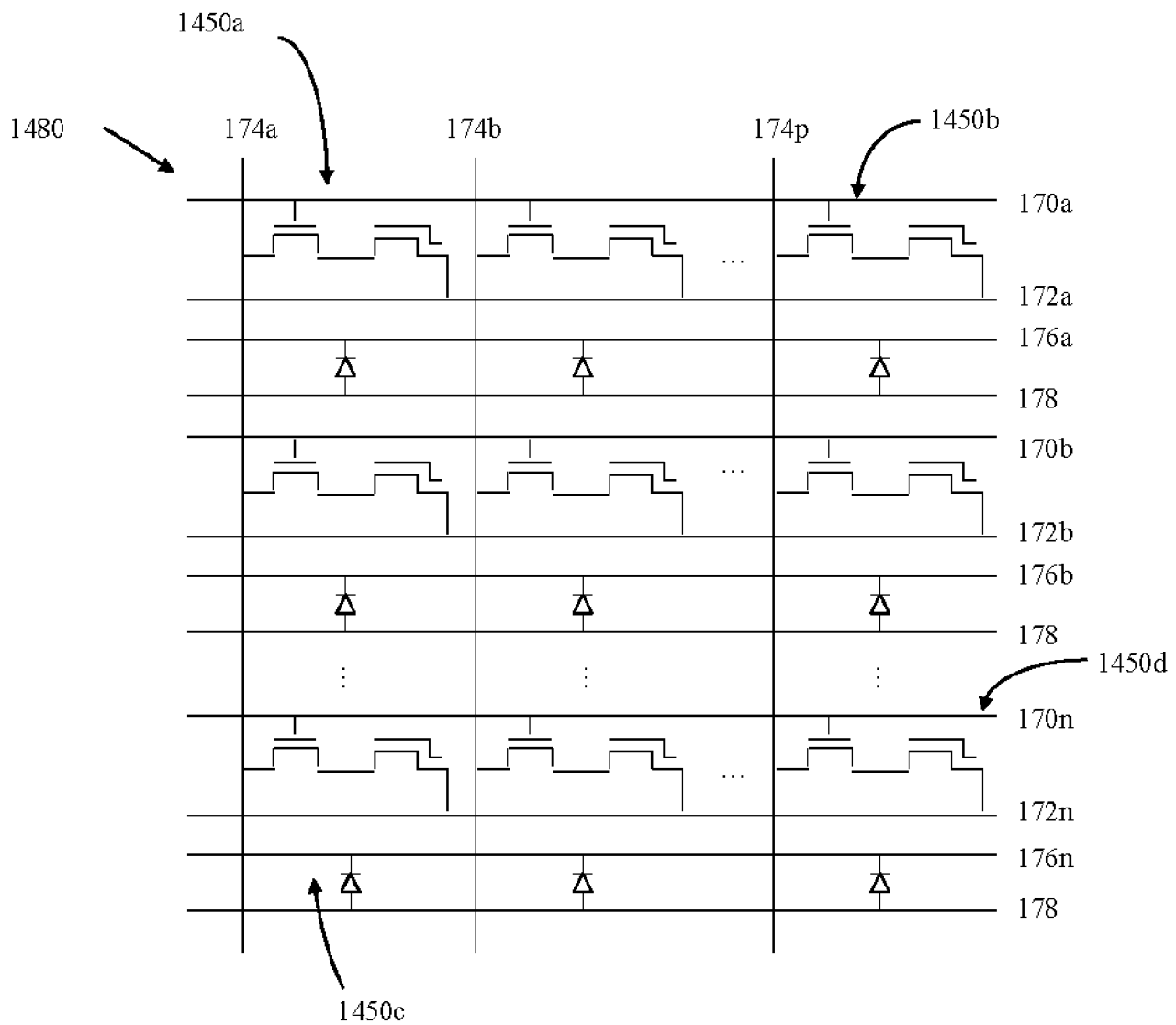


FIG. 204

Array Hold Operation (All Memory Cells 1450)

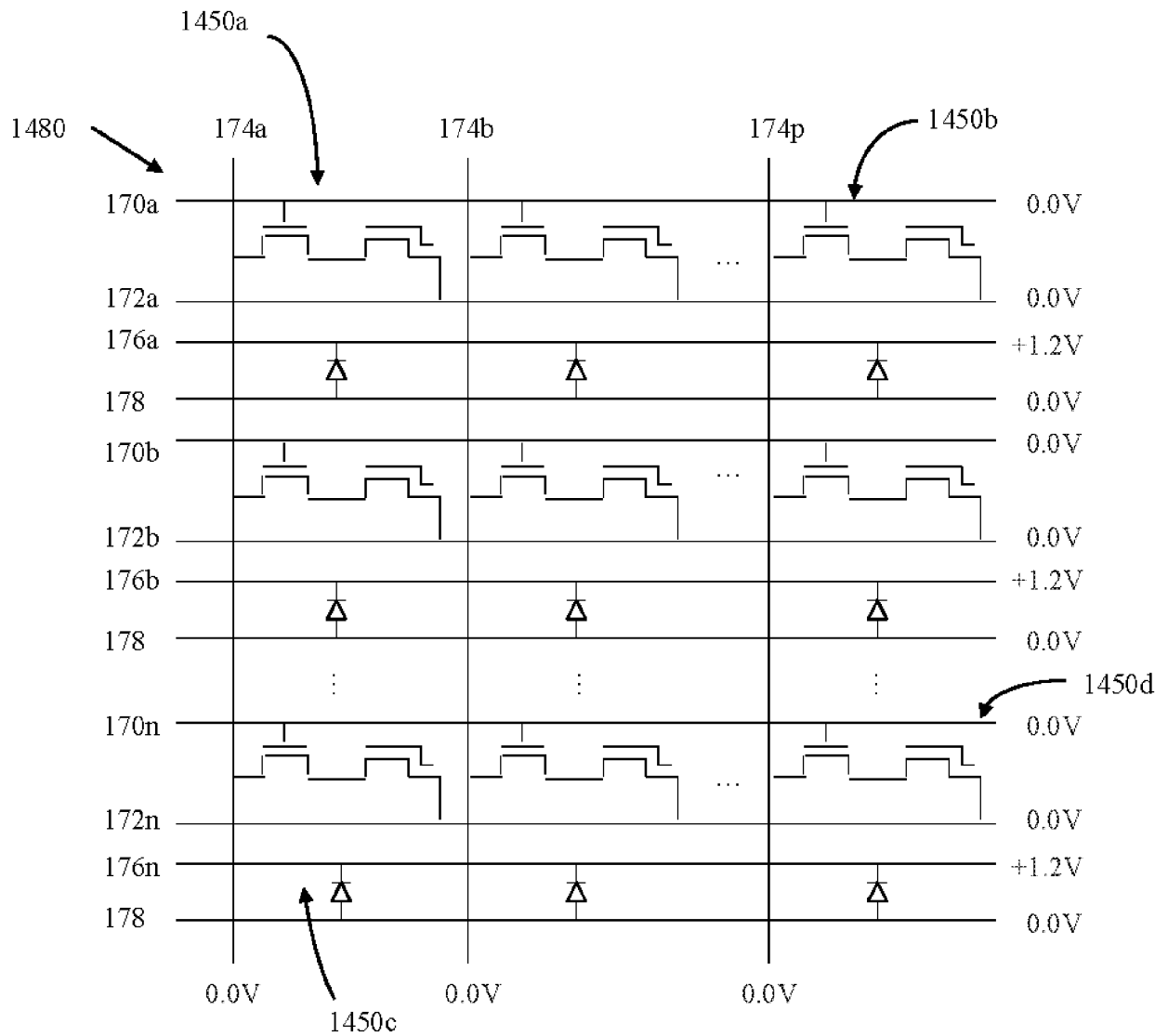


FIG. 205

Read Operation (Memory Cell 1450a)

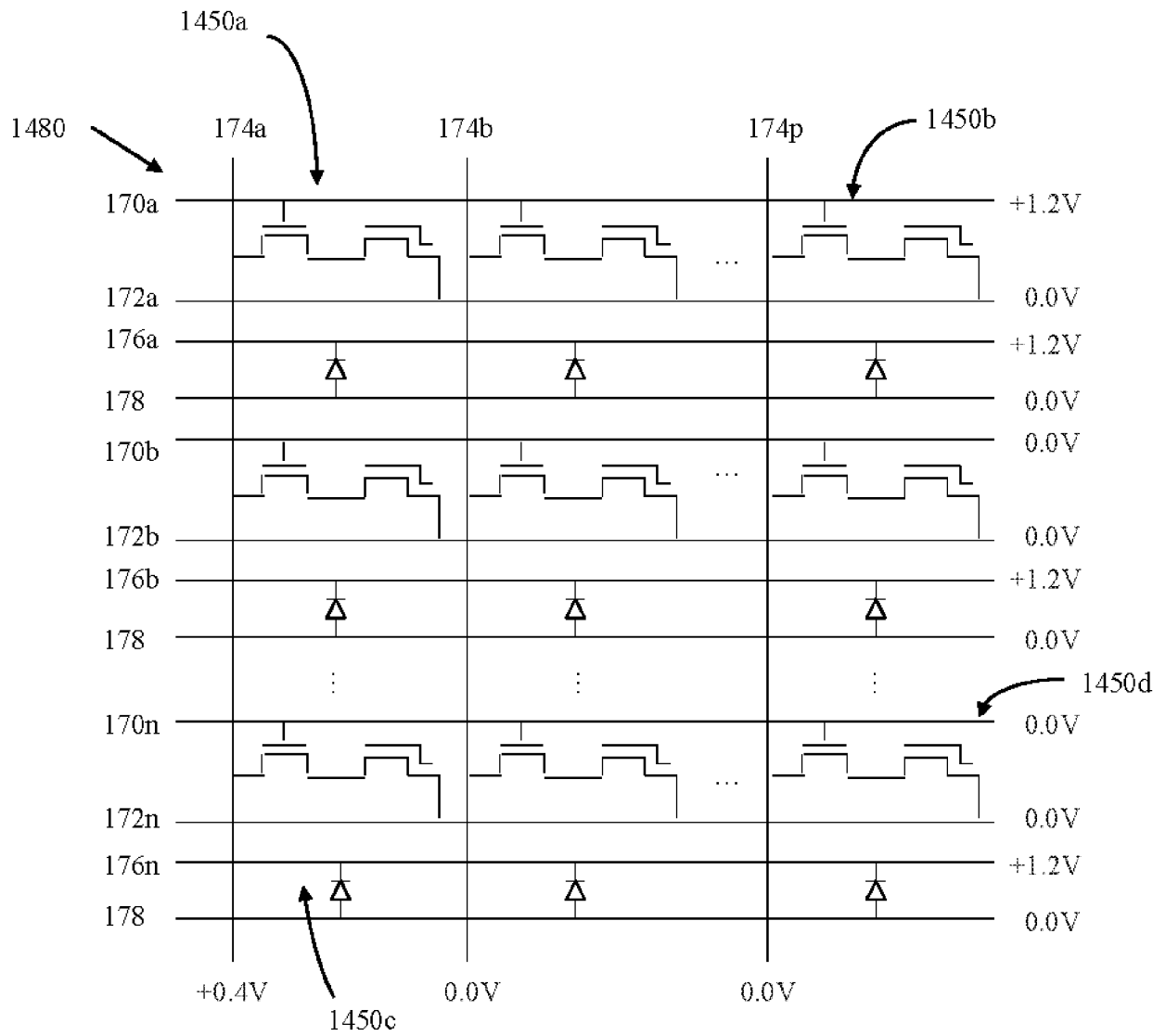


FIG. 206

Write Logic-0 Operation (Memory Cells 1450a, 1450b)

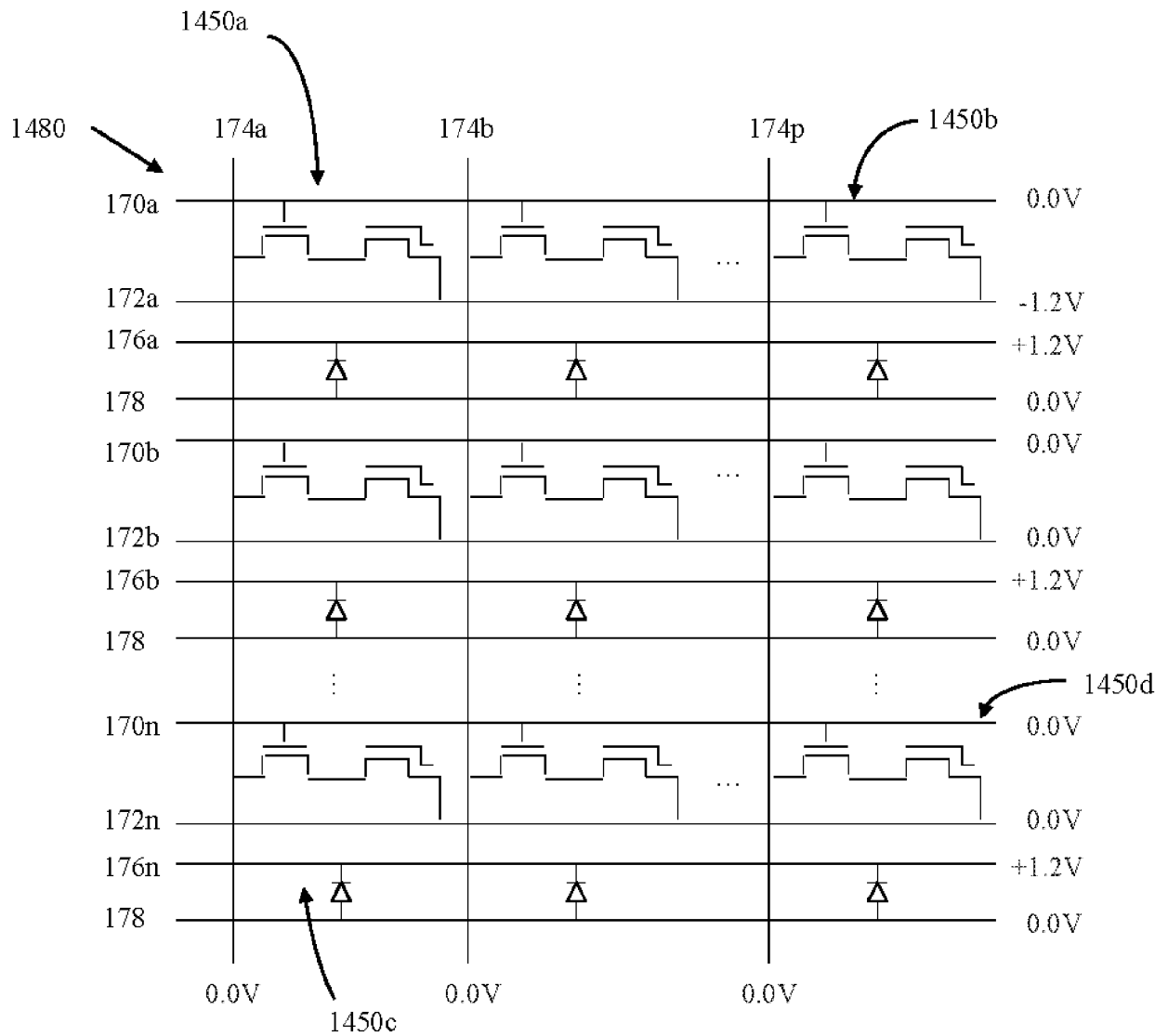


FIG. 207A

Write Logic-0 Operation (Memory Cells 1450a, 1450c)

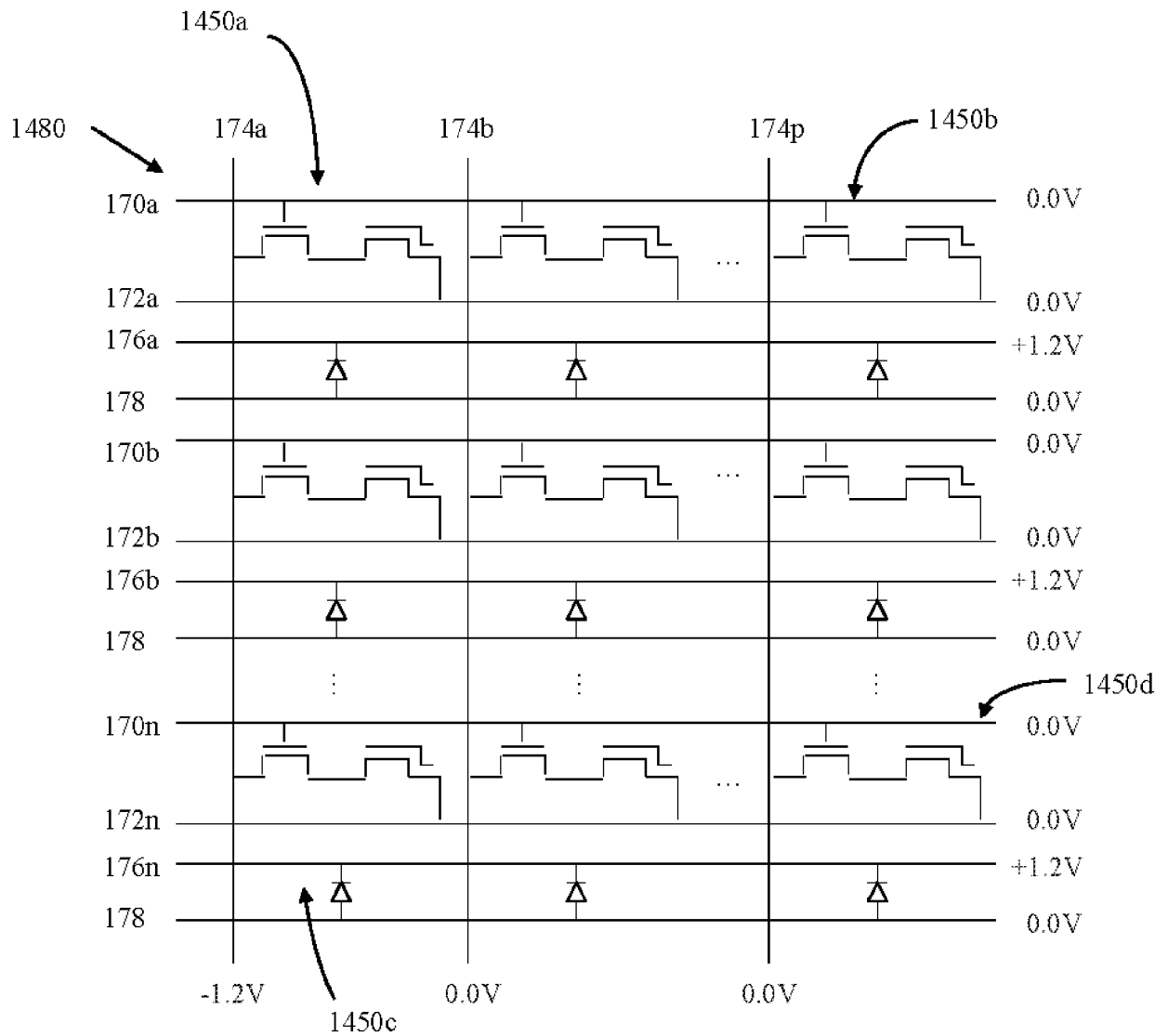


FIG. 207B

Write Logic-0 Operation (Memory Cell 1450a)

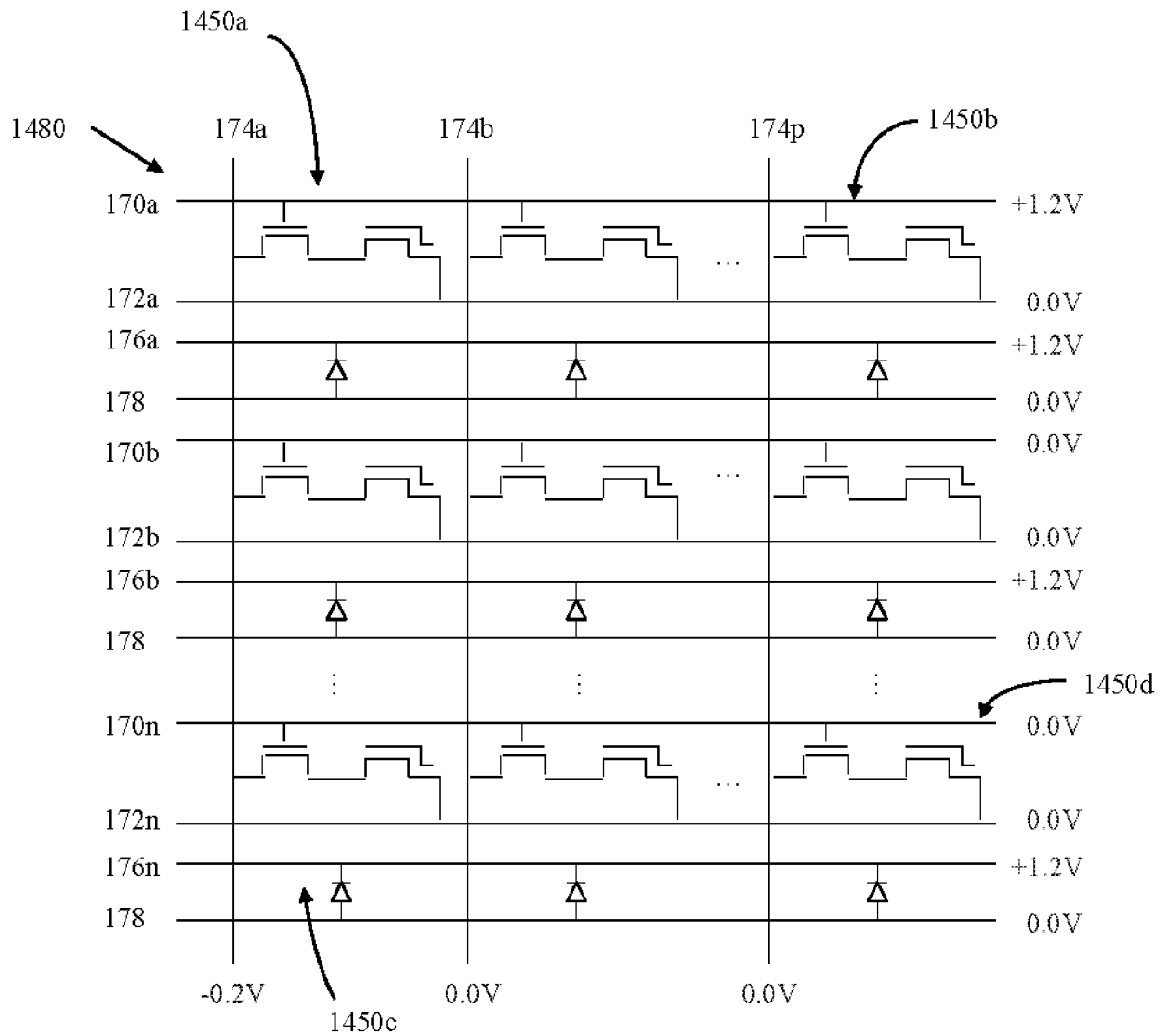


FIG. 207C

Write Logic-1 Operation (Memory Cell 1450a)

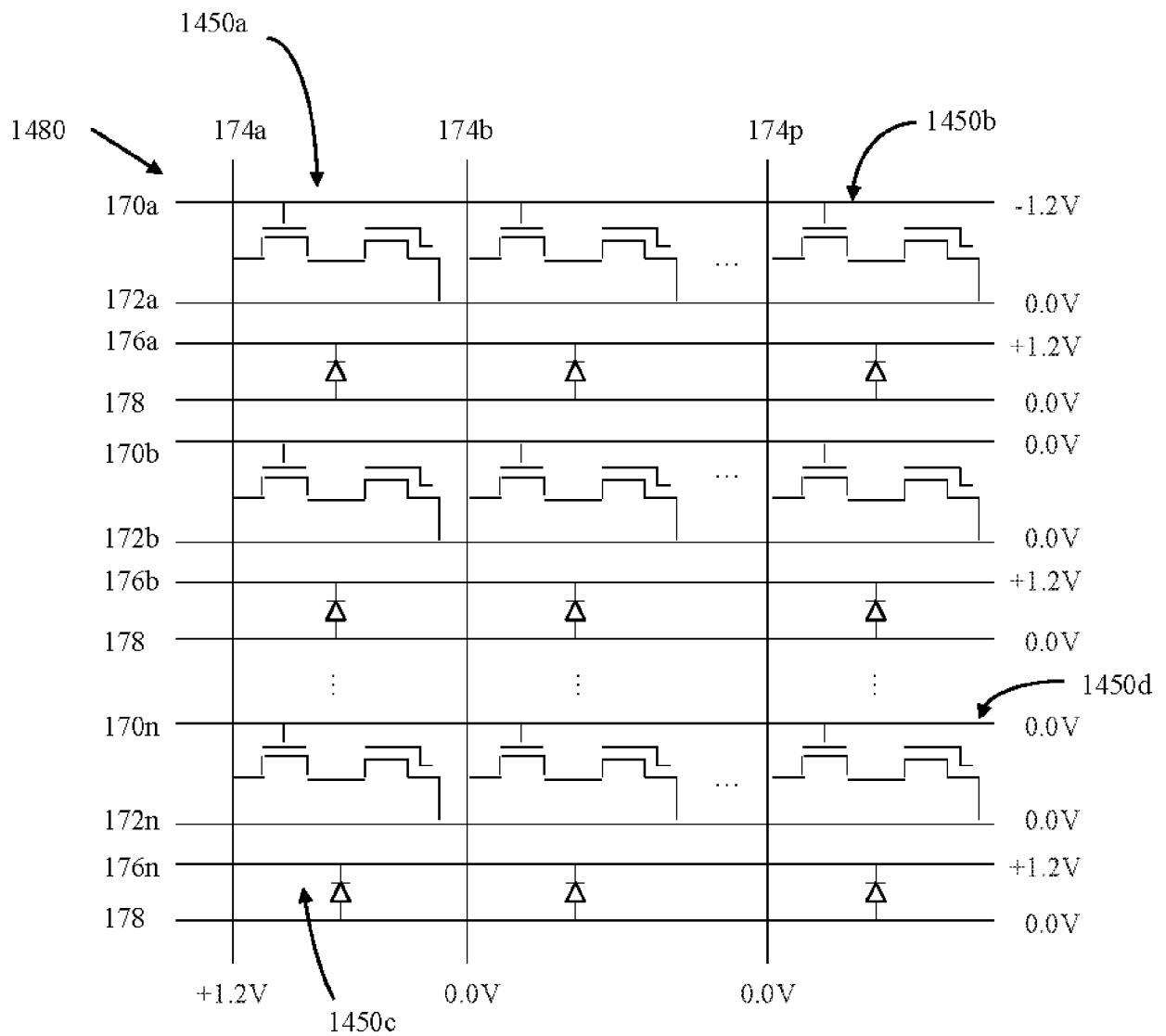


FIG. 208A

Write Logic-1 Operation (Memory Cell 1450a)

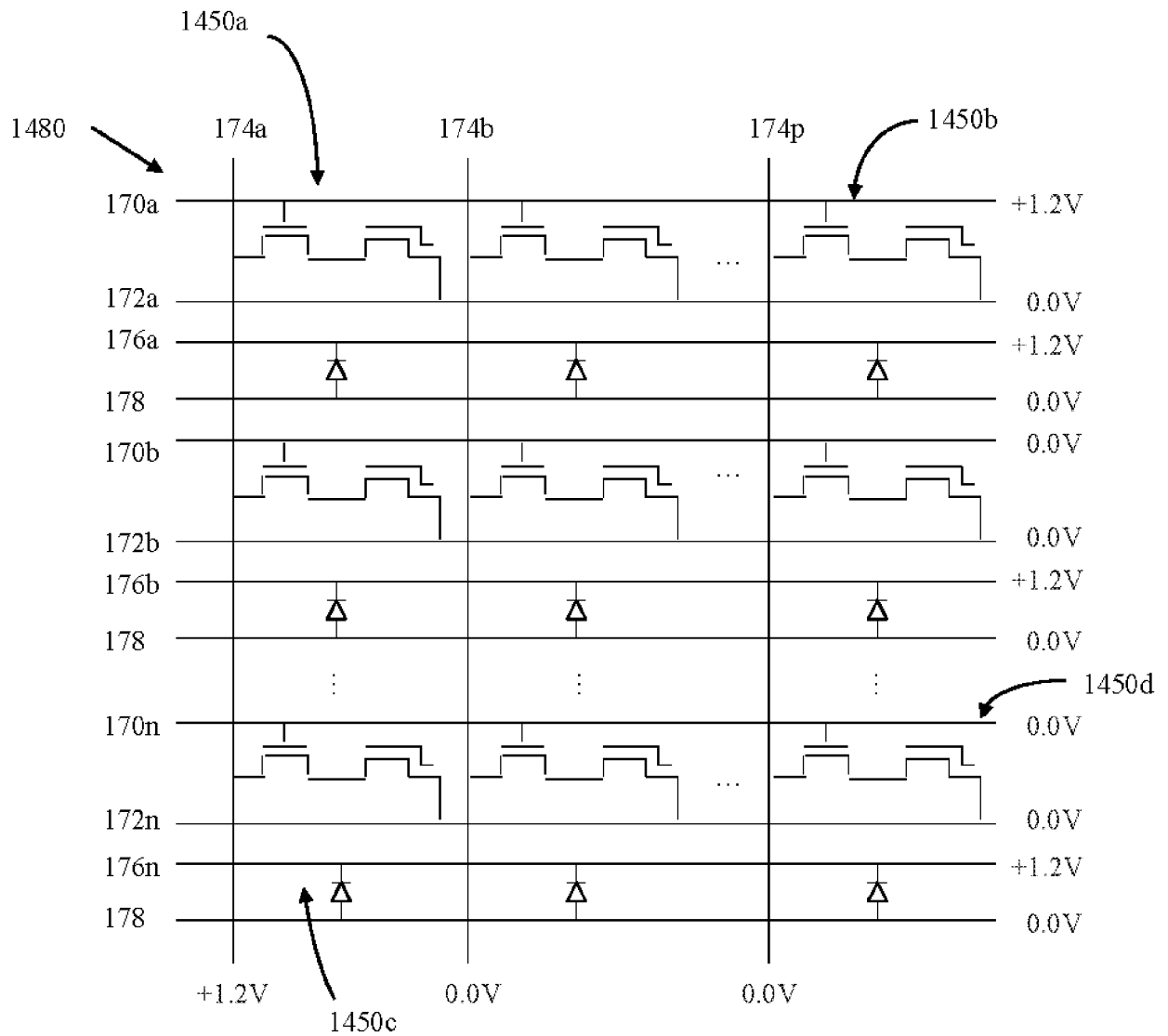


FIG. 208B

Shadowing Operation (All Memory Cells 1450)

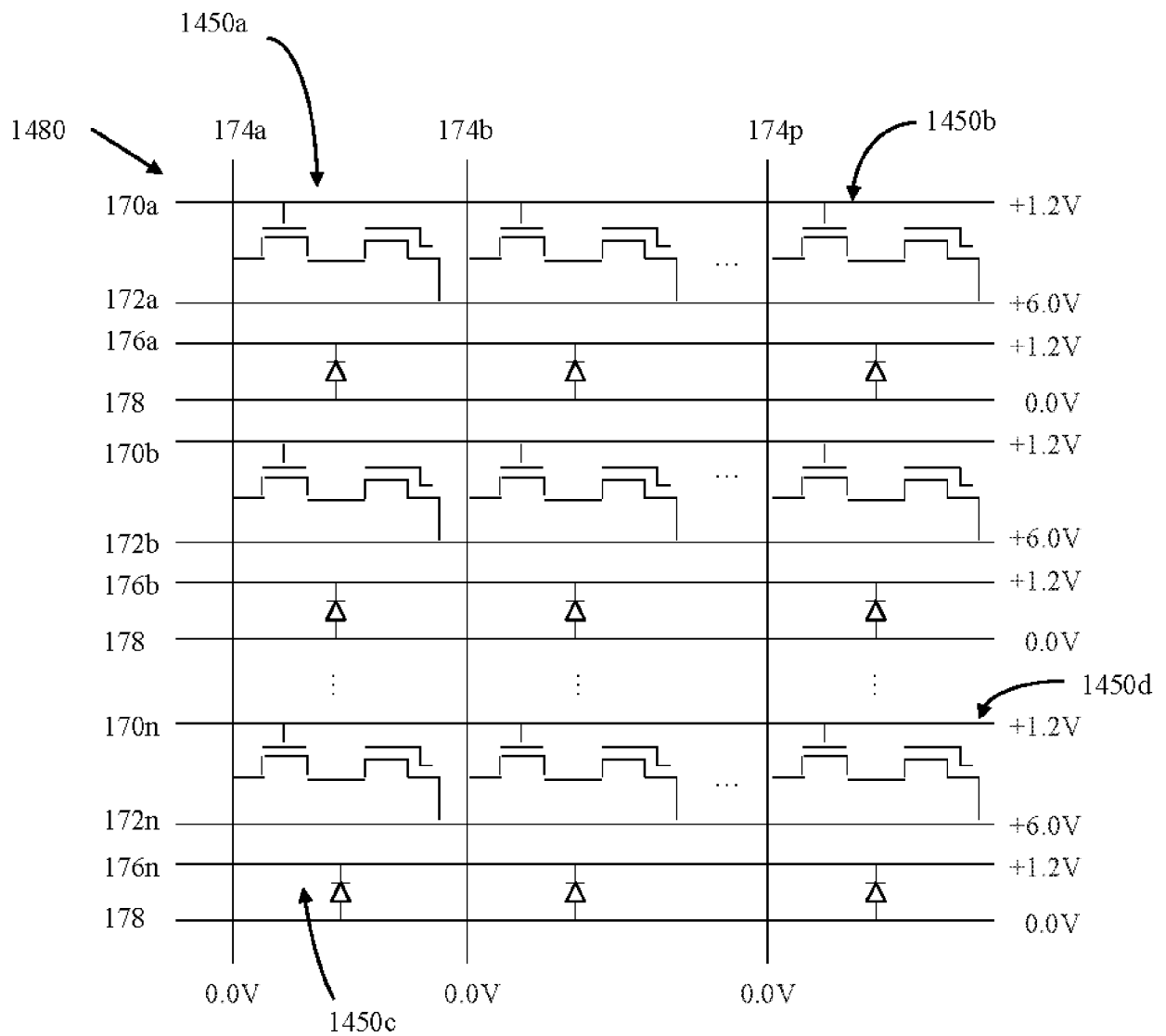


FIG. 209

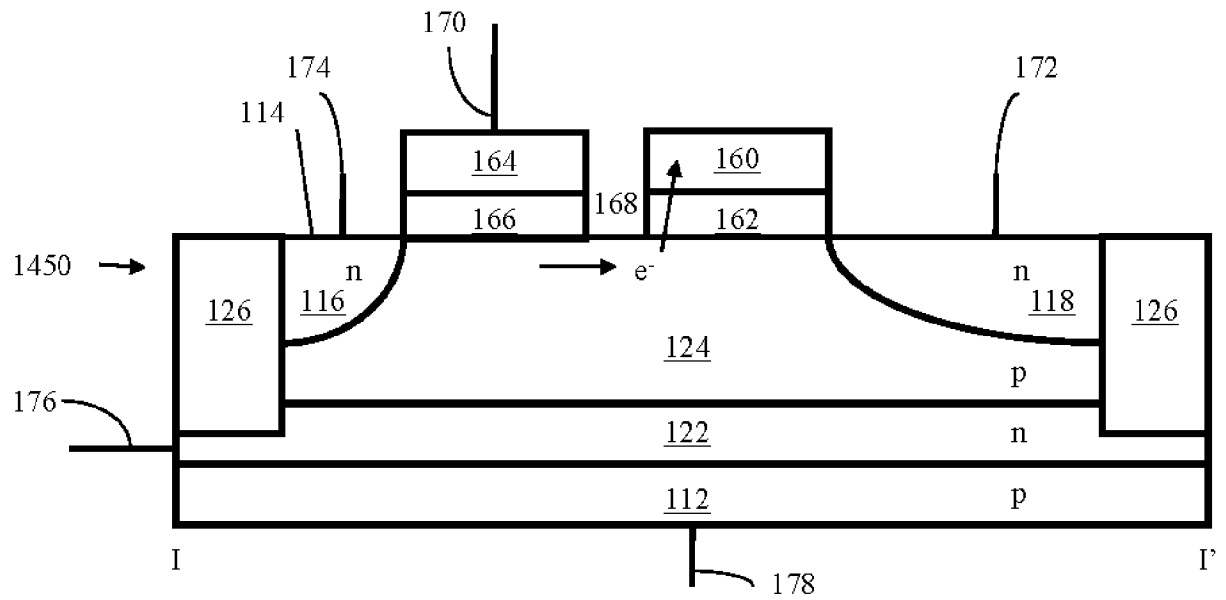


FIG. 210A

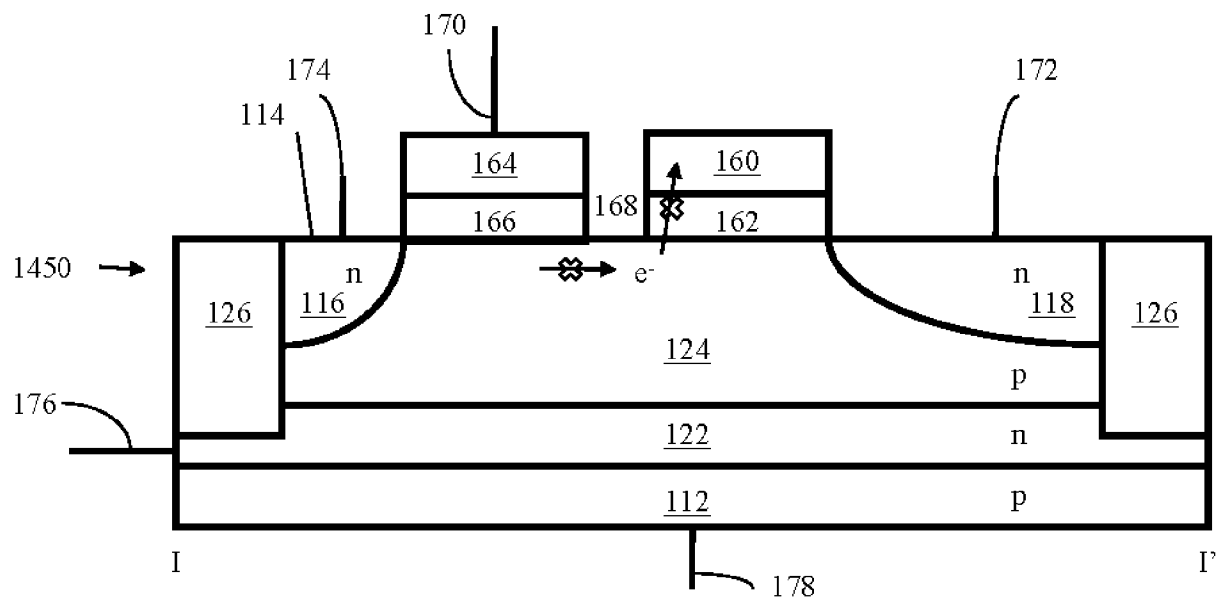


FIG. 210B

Restore Operation (All Memory Cells 1450)

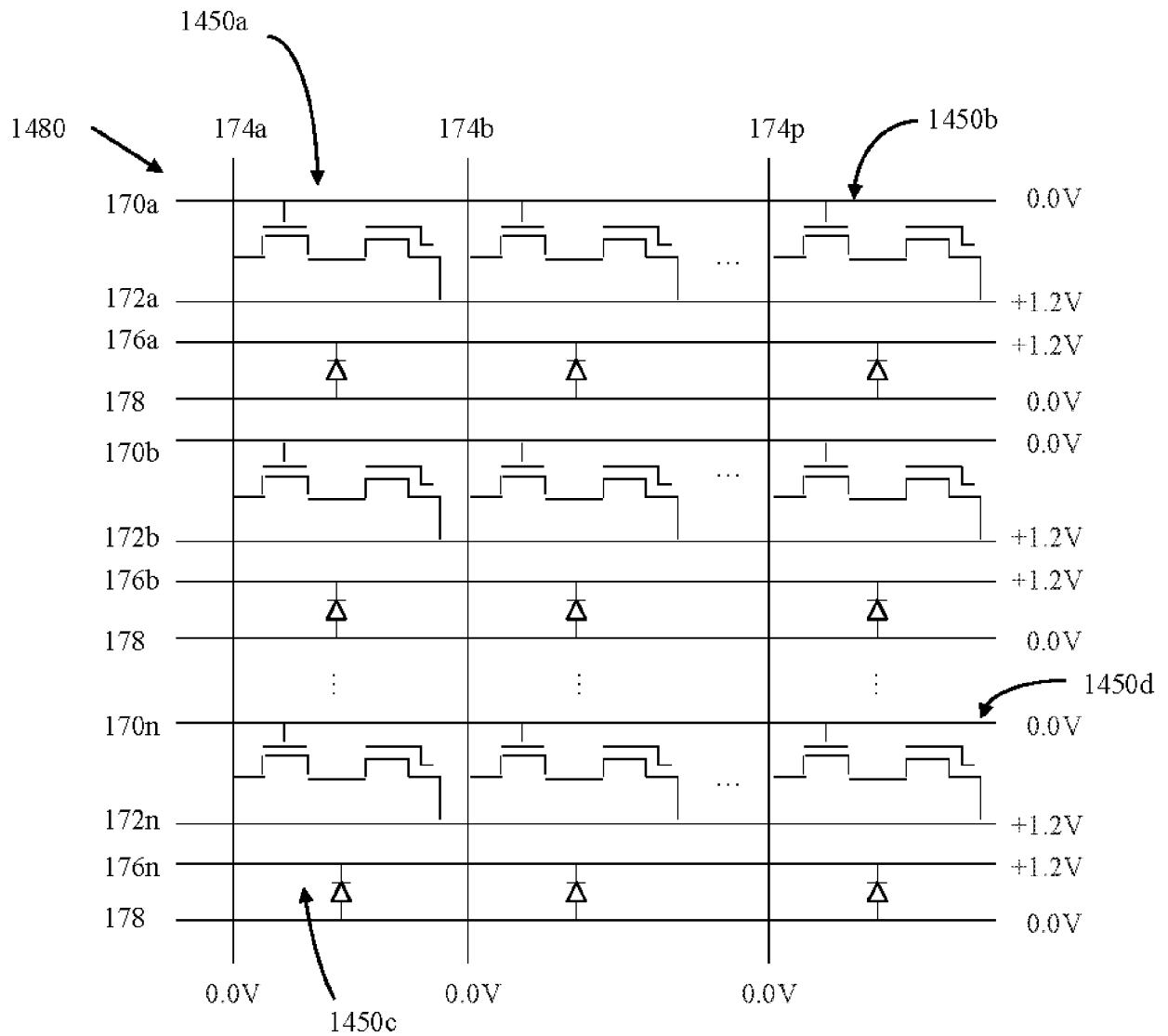


FIG. 211

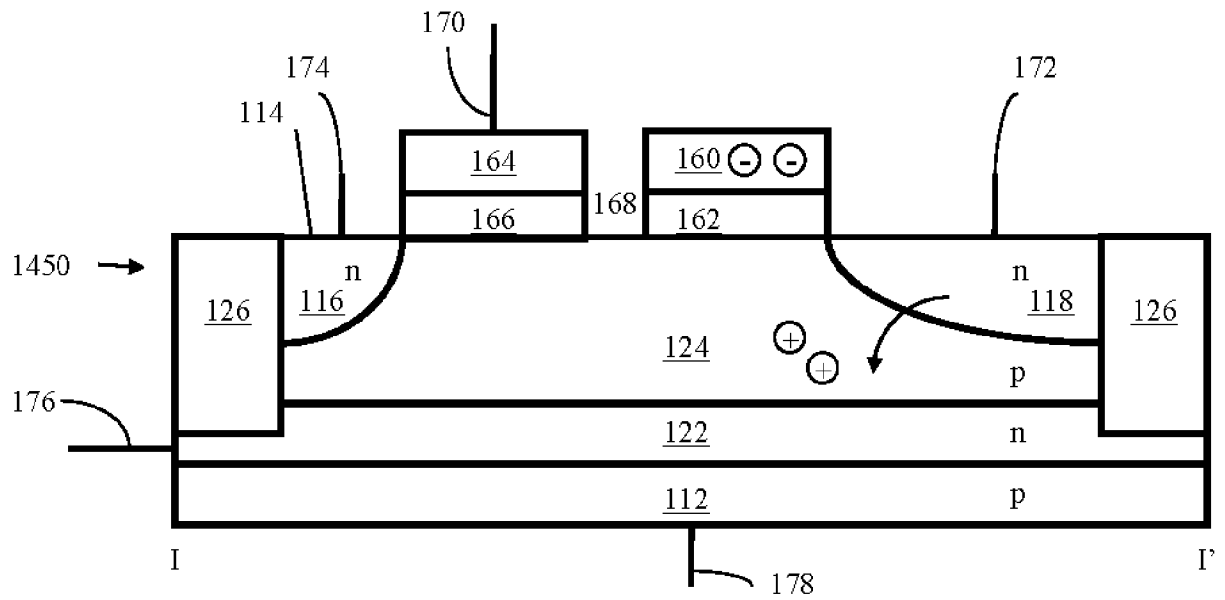


FIG. 212A

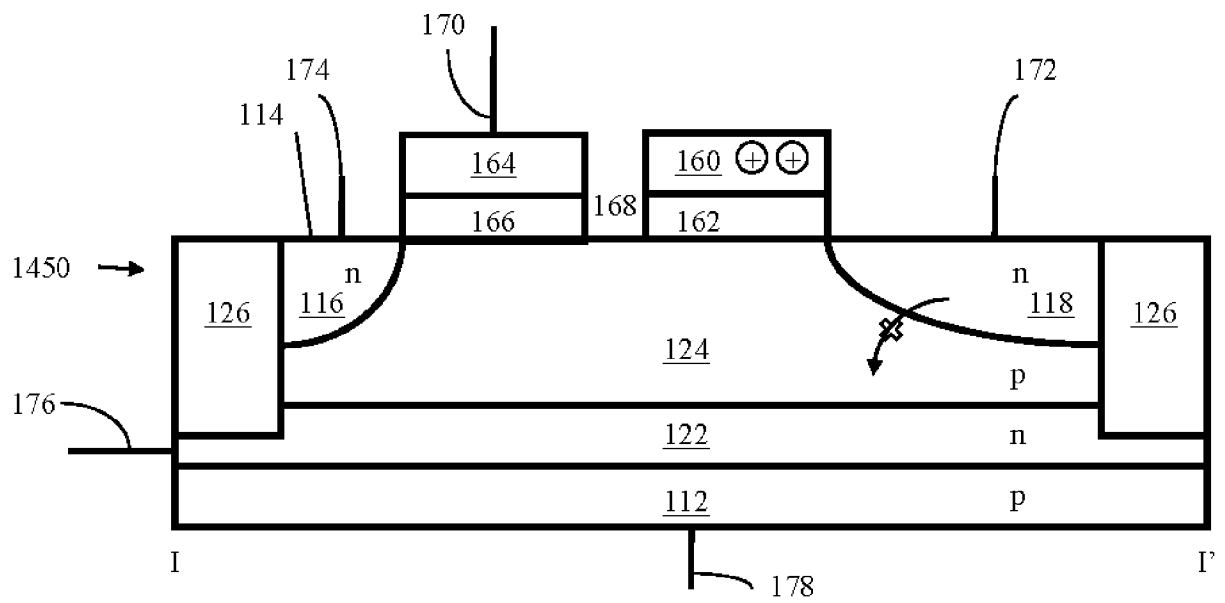


FIG. 212B

Reset Operation (All Memory Cells 1450)

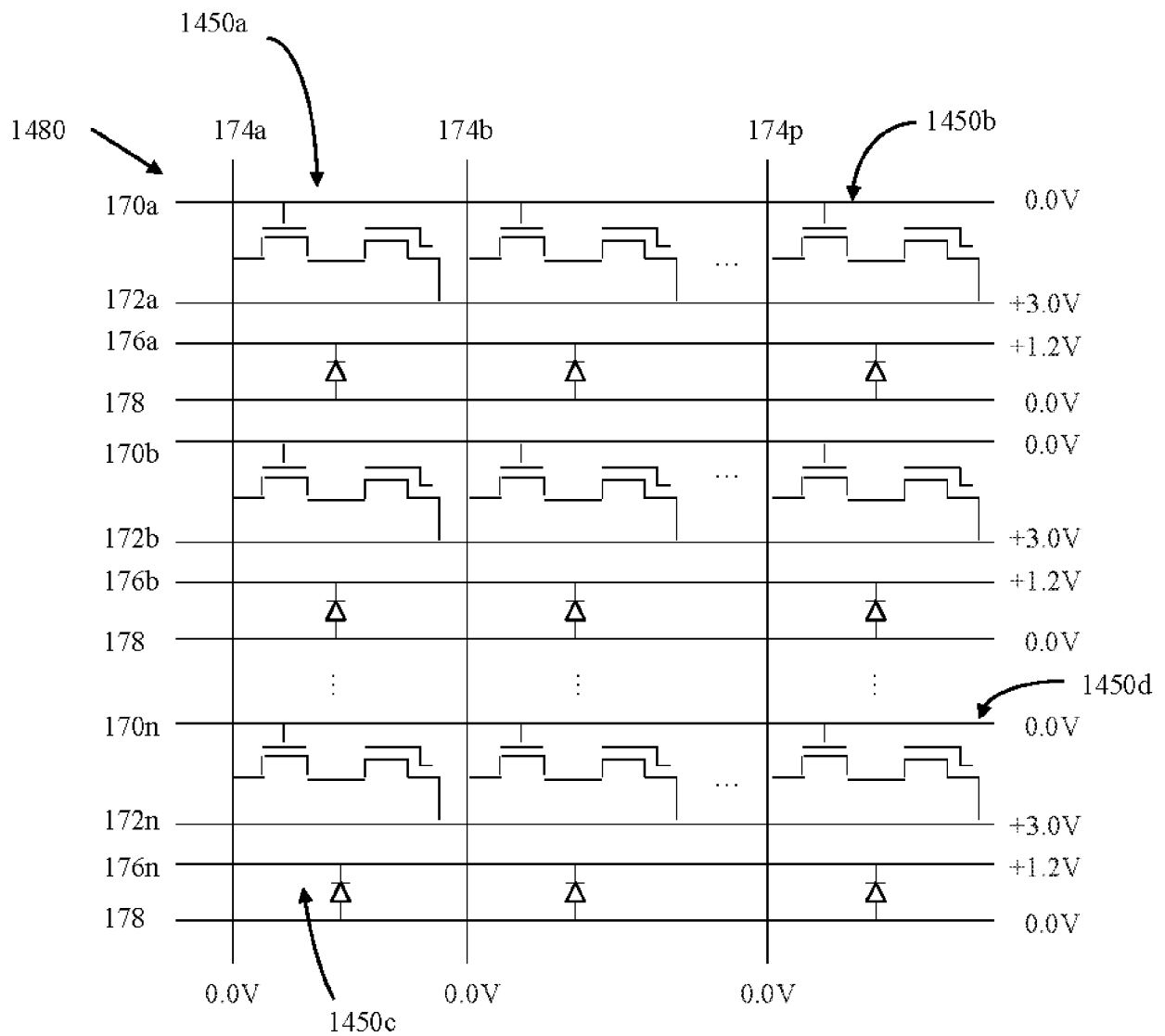


FIG. 213A

Reset Operation (All Memory Cells 1450)

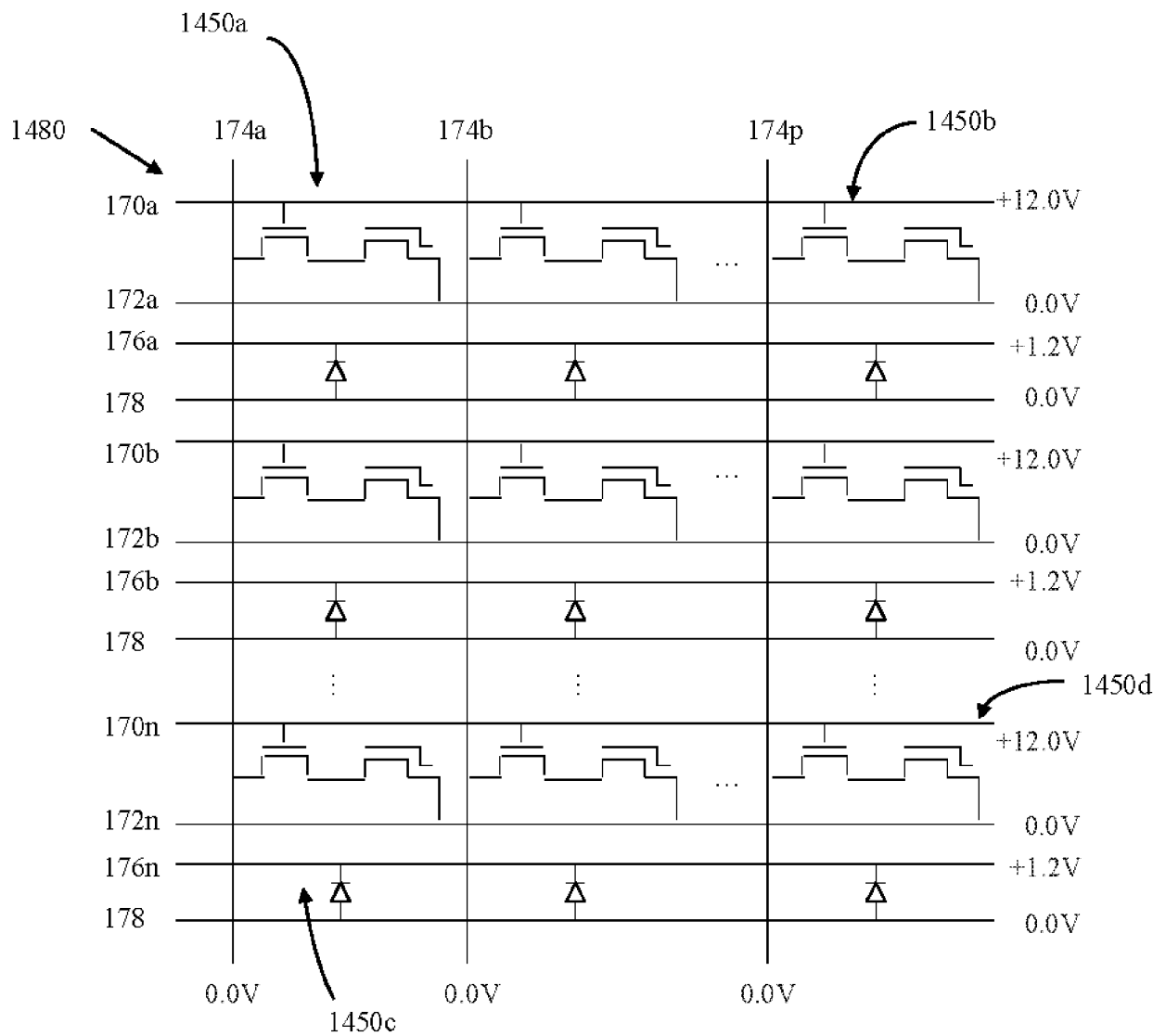


FIG. 213B

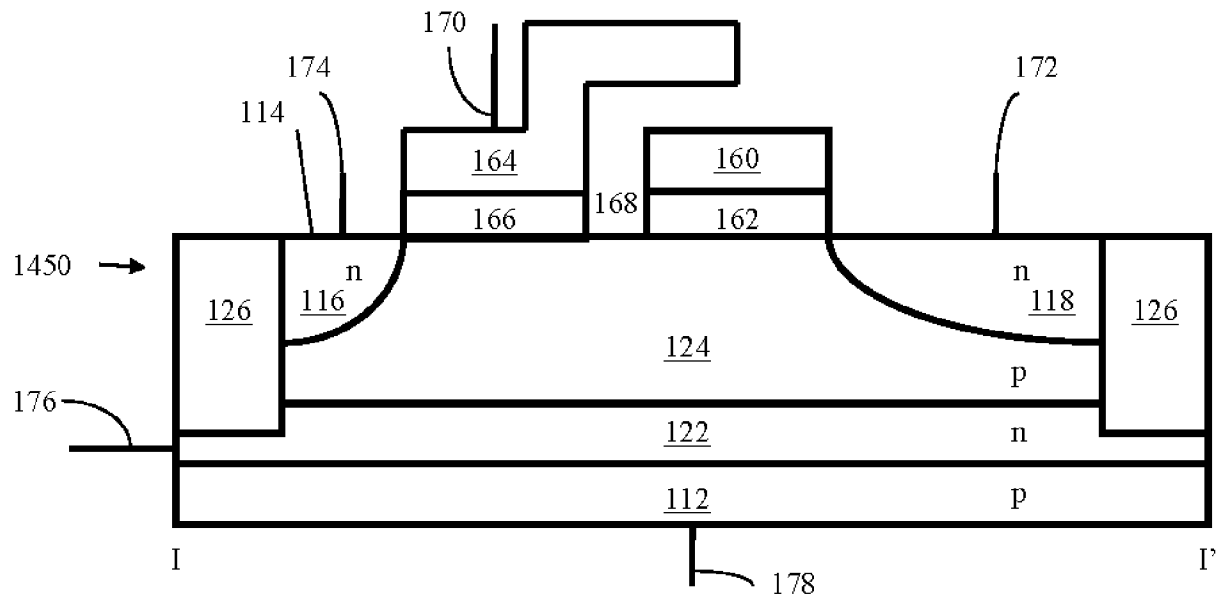


FIG. 214

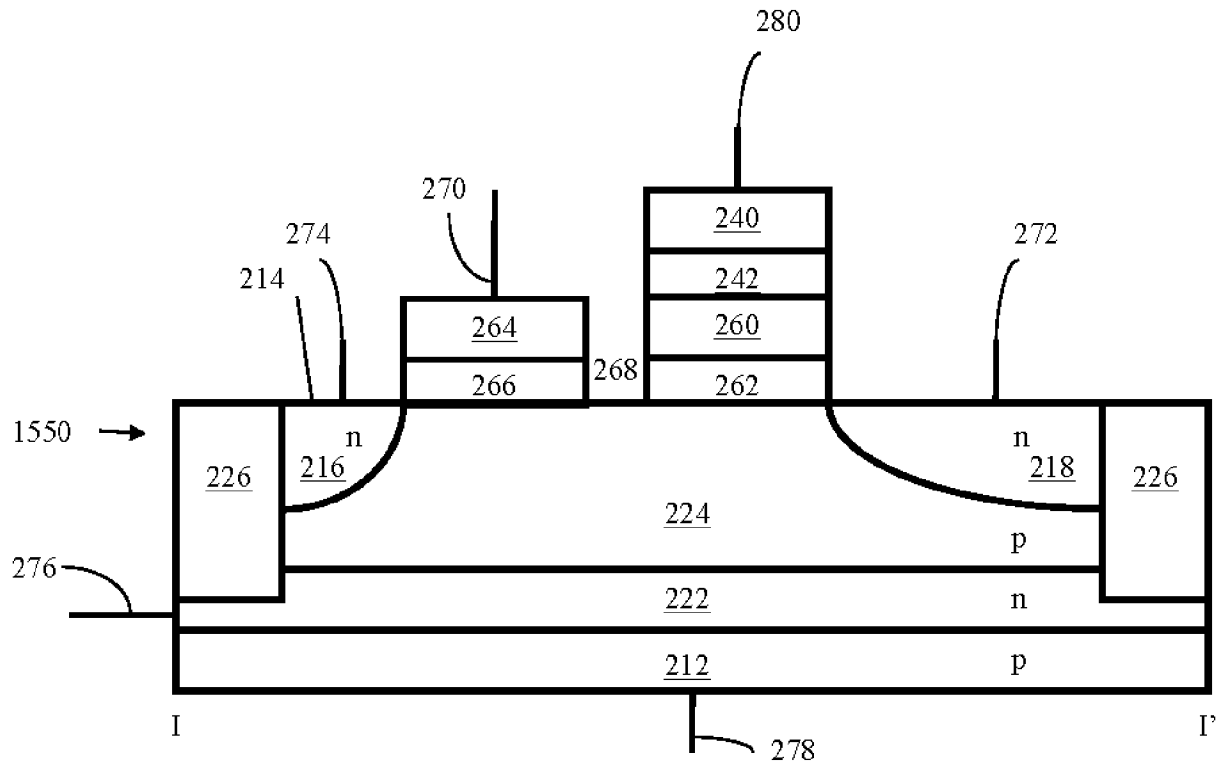


FIG. 215A

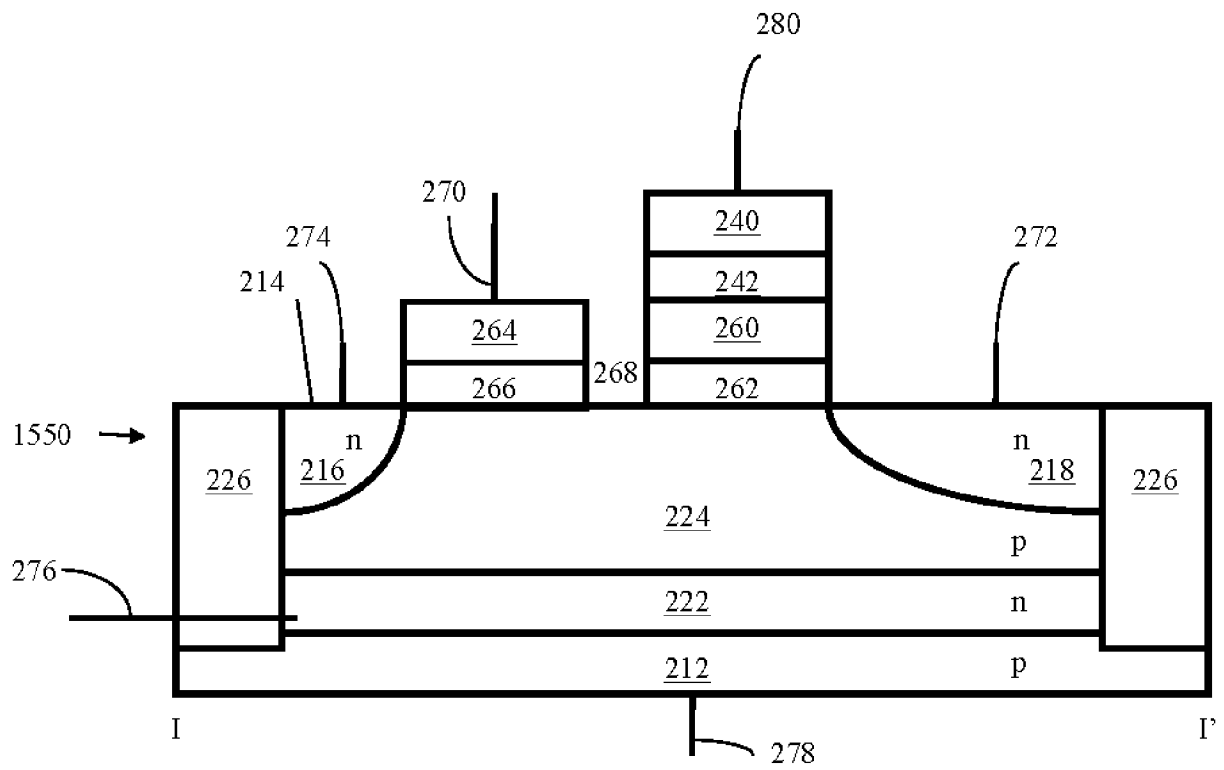


FIG. 215B

Exemplary Memory Array 1580 with
Representative Memory Cells 1550a, 1550b, 1550c
and 1550d

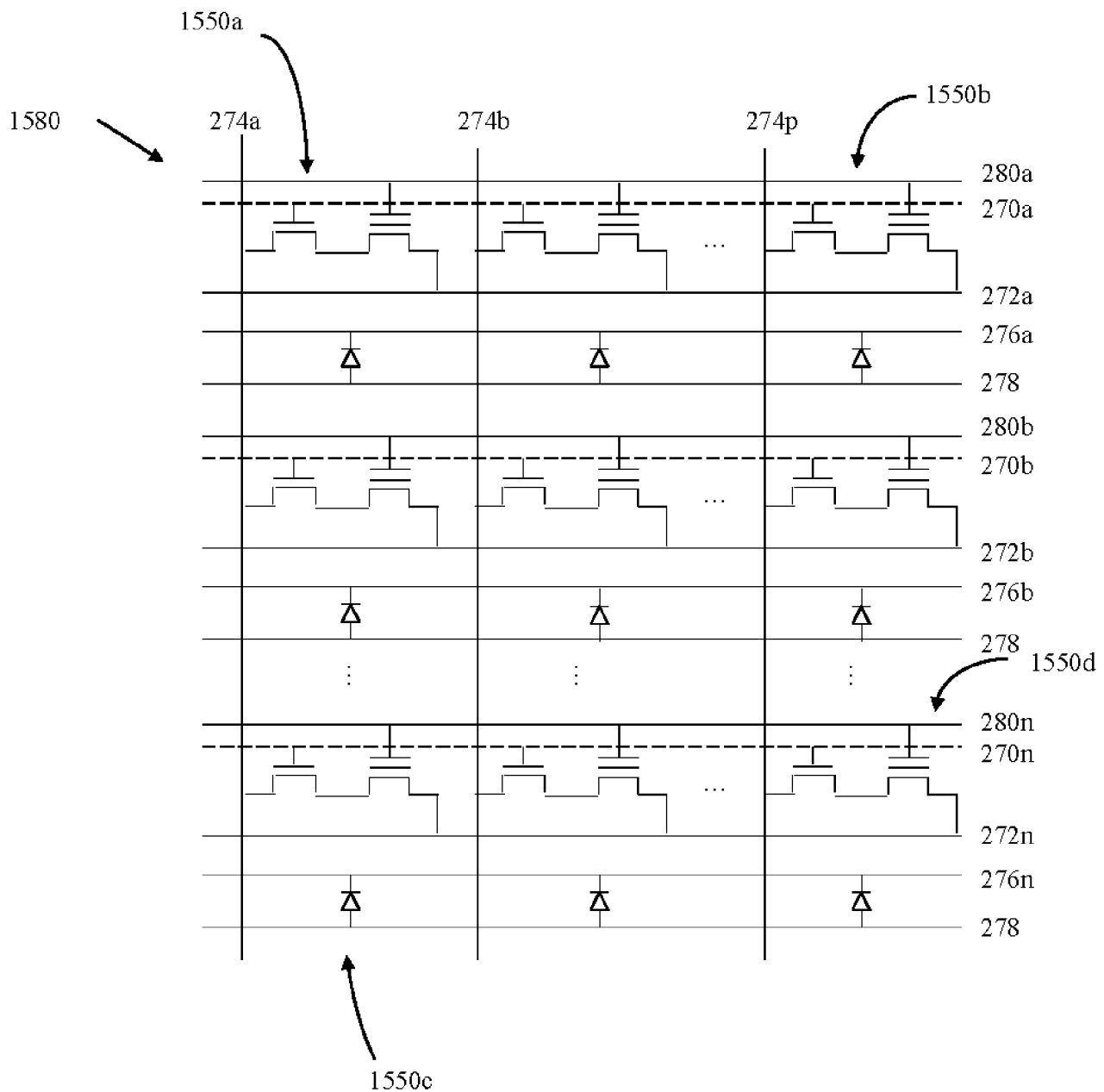


FIG. 217

Array Hold Operation (All Memory Cells 1550)

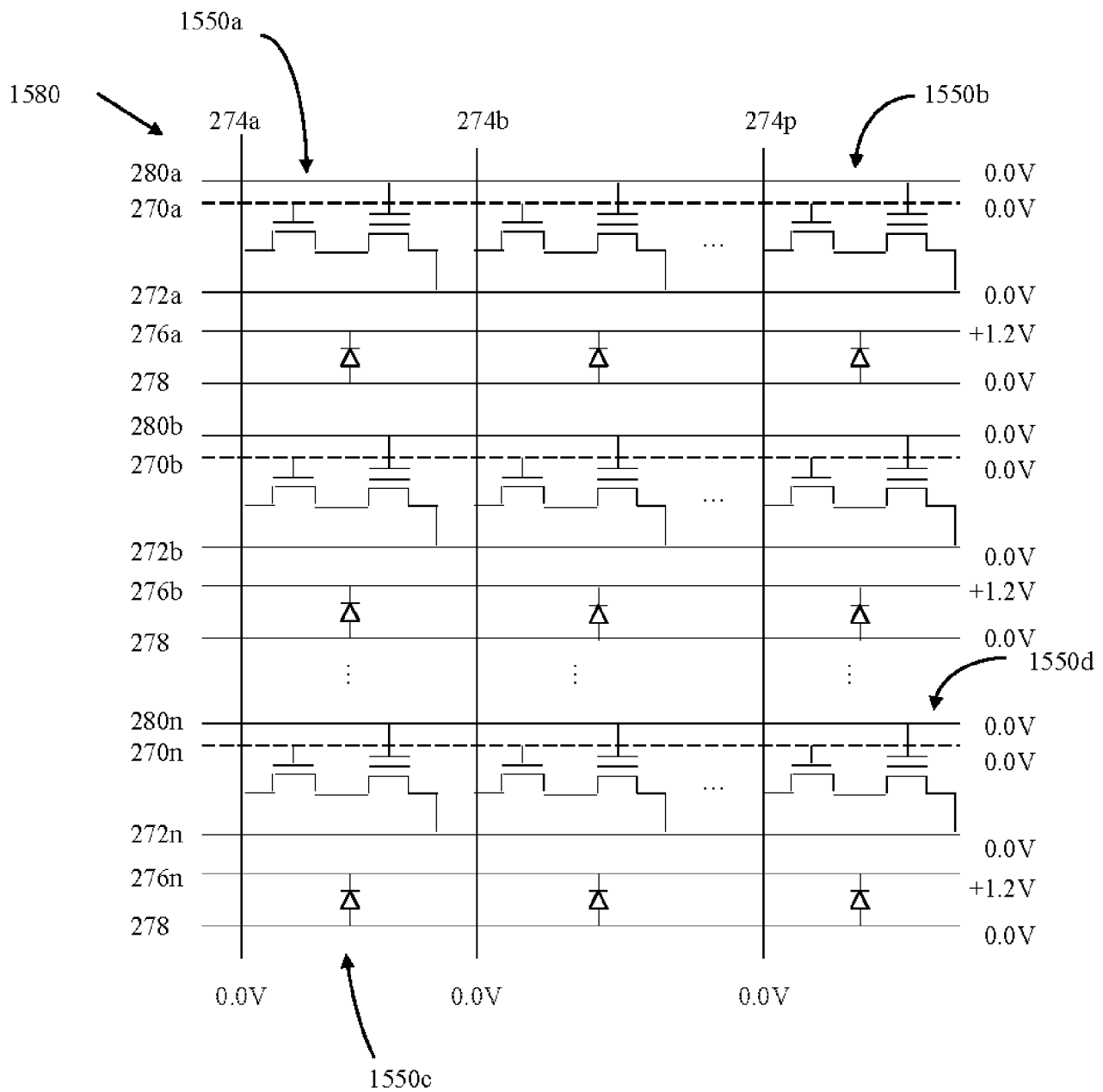


FIG. 218

Read Operation (Memory Cell 1550a)

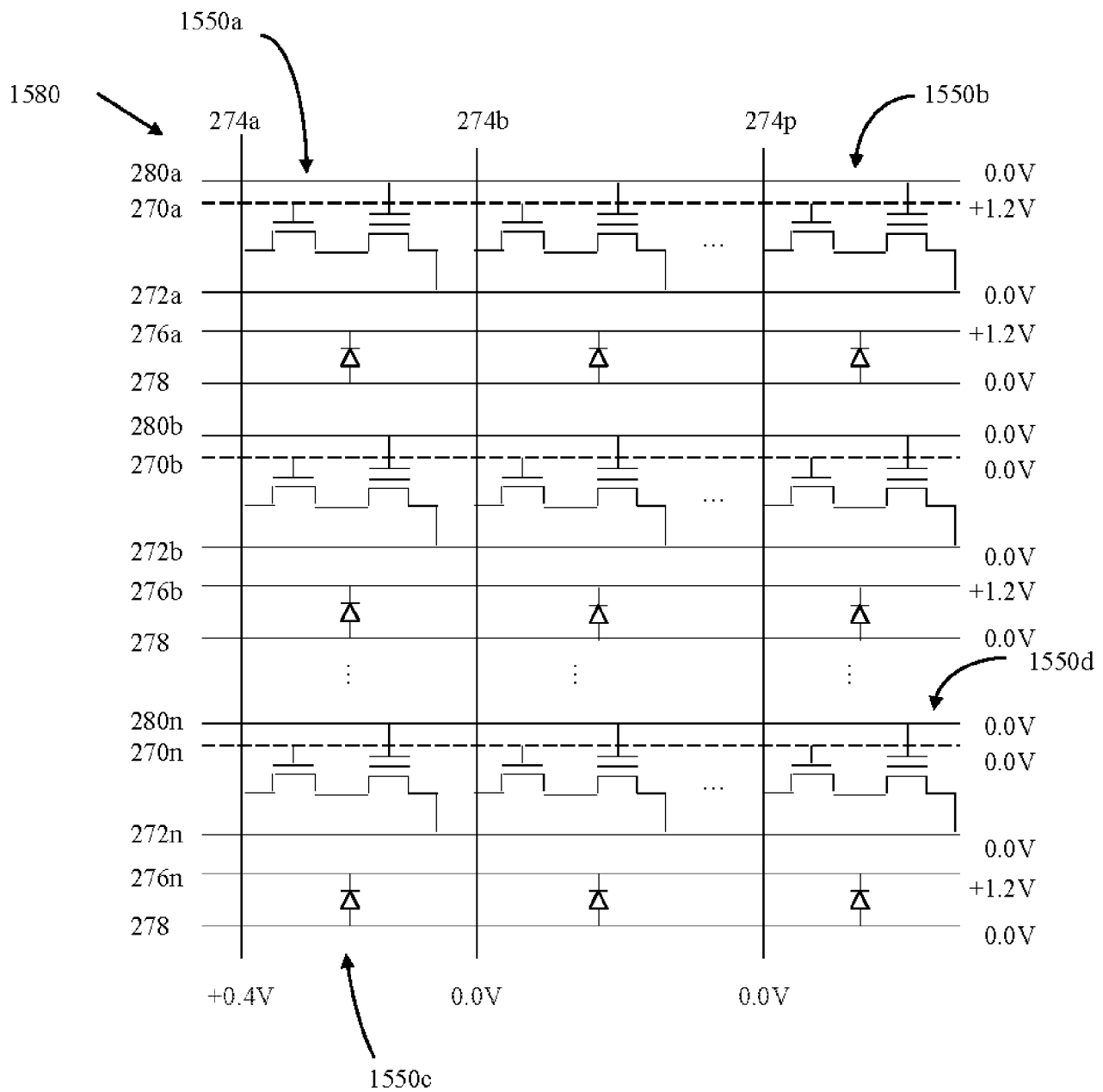


FIG. 219

Write Logic-0 Operation (Memory Cells 1550a, 1550b)

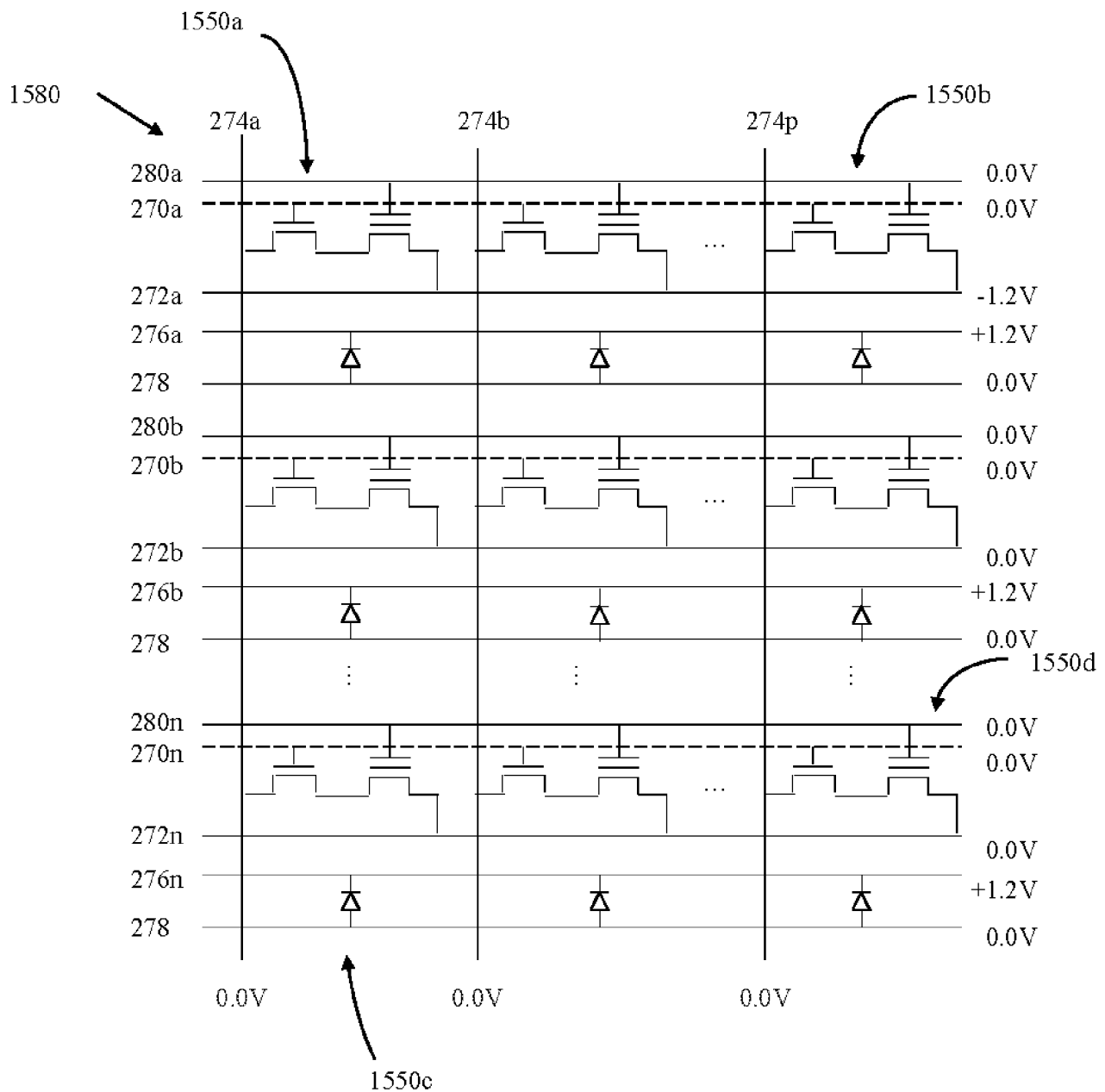


FIG. 220A

Write Logic-0 Operation (Memory Cells 1550a, 1550c)

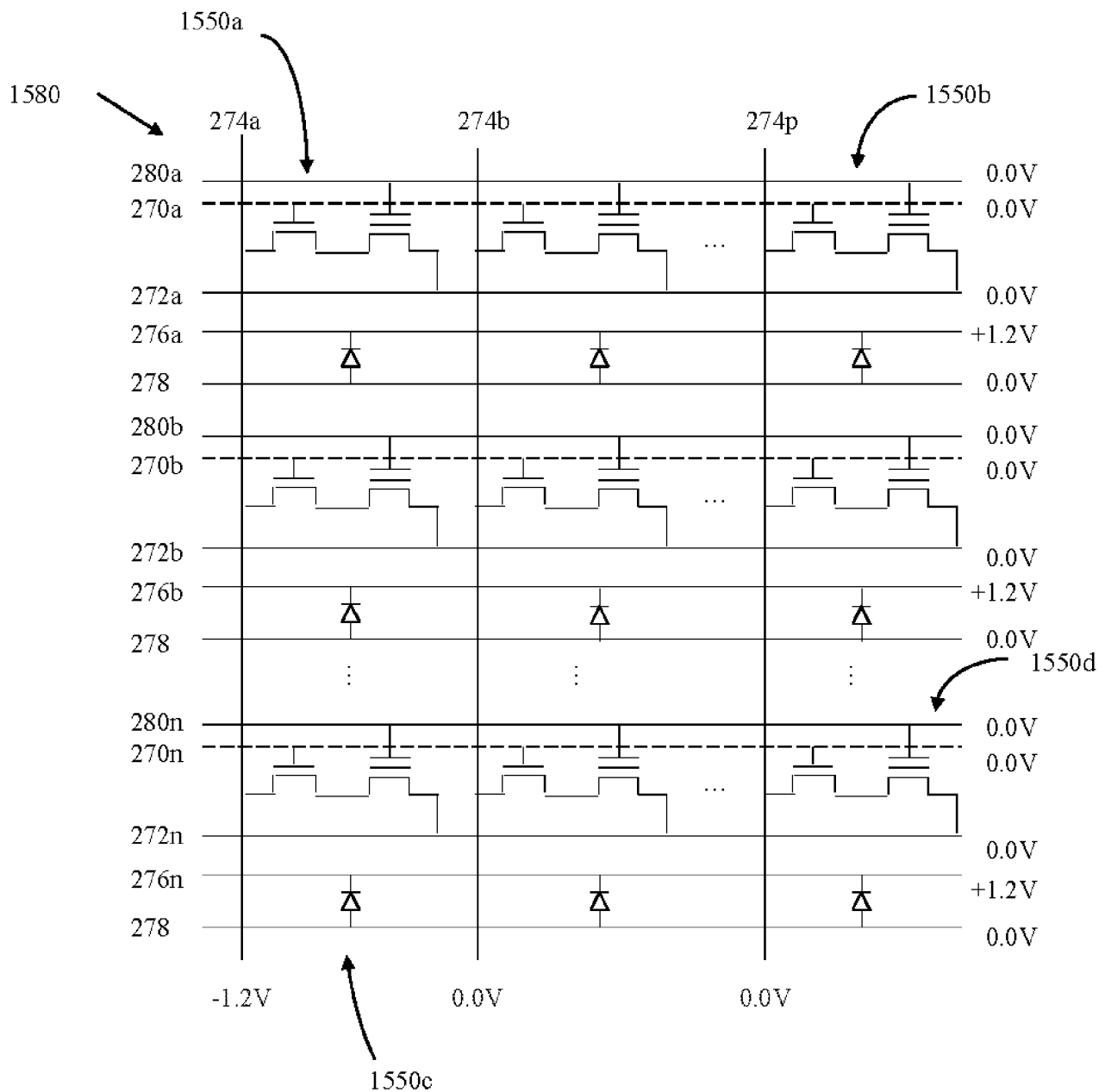


FIG. 220B

Write Logic-0 Operation (Memory Cell 1550a)

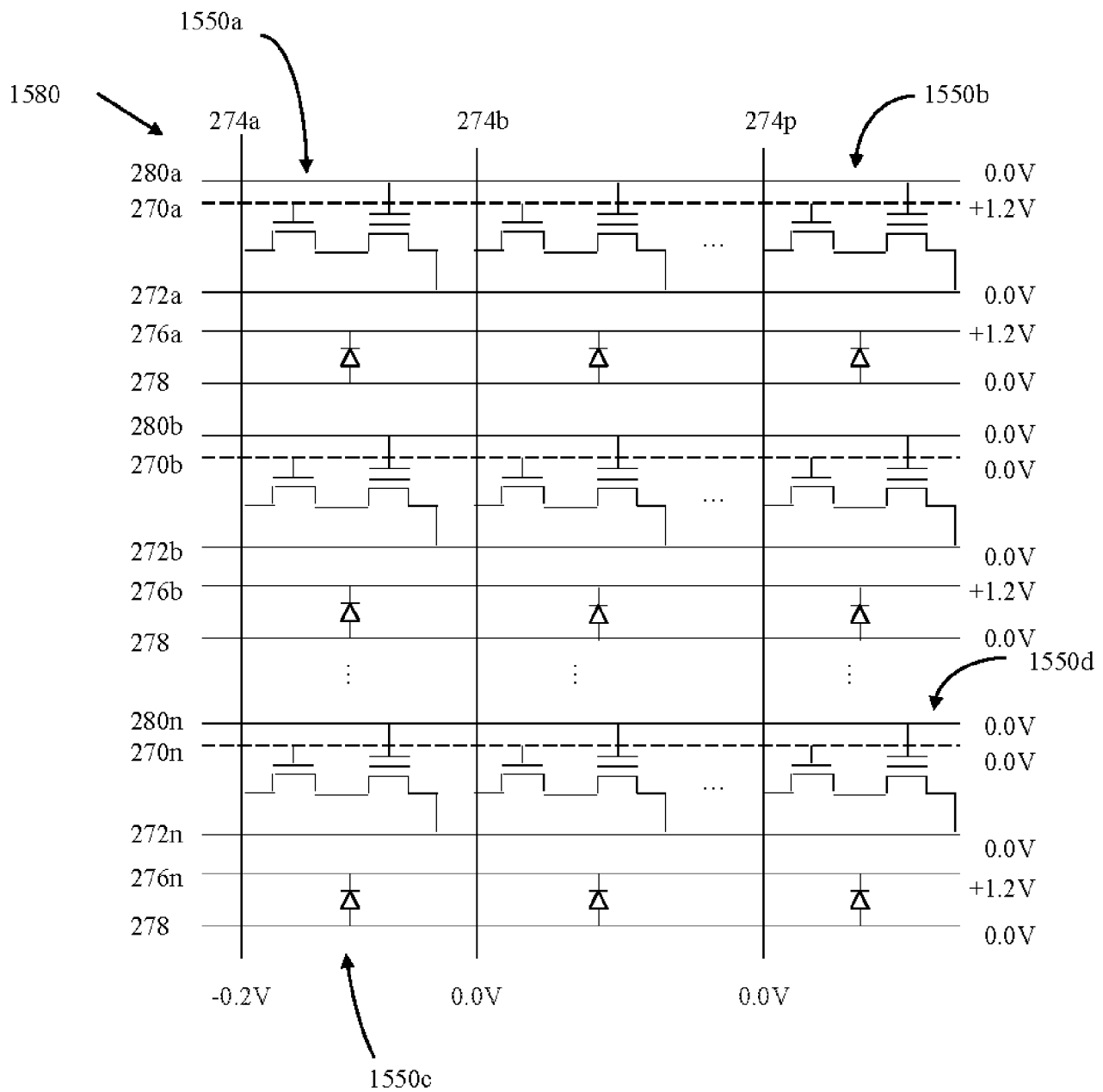


FIG. 221

Write Logic-1 Operation (Memory Cell 1550a)

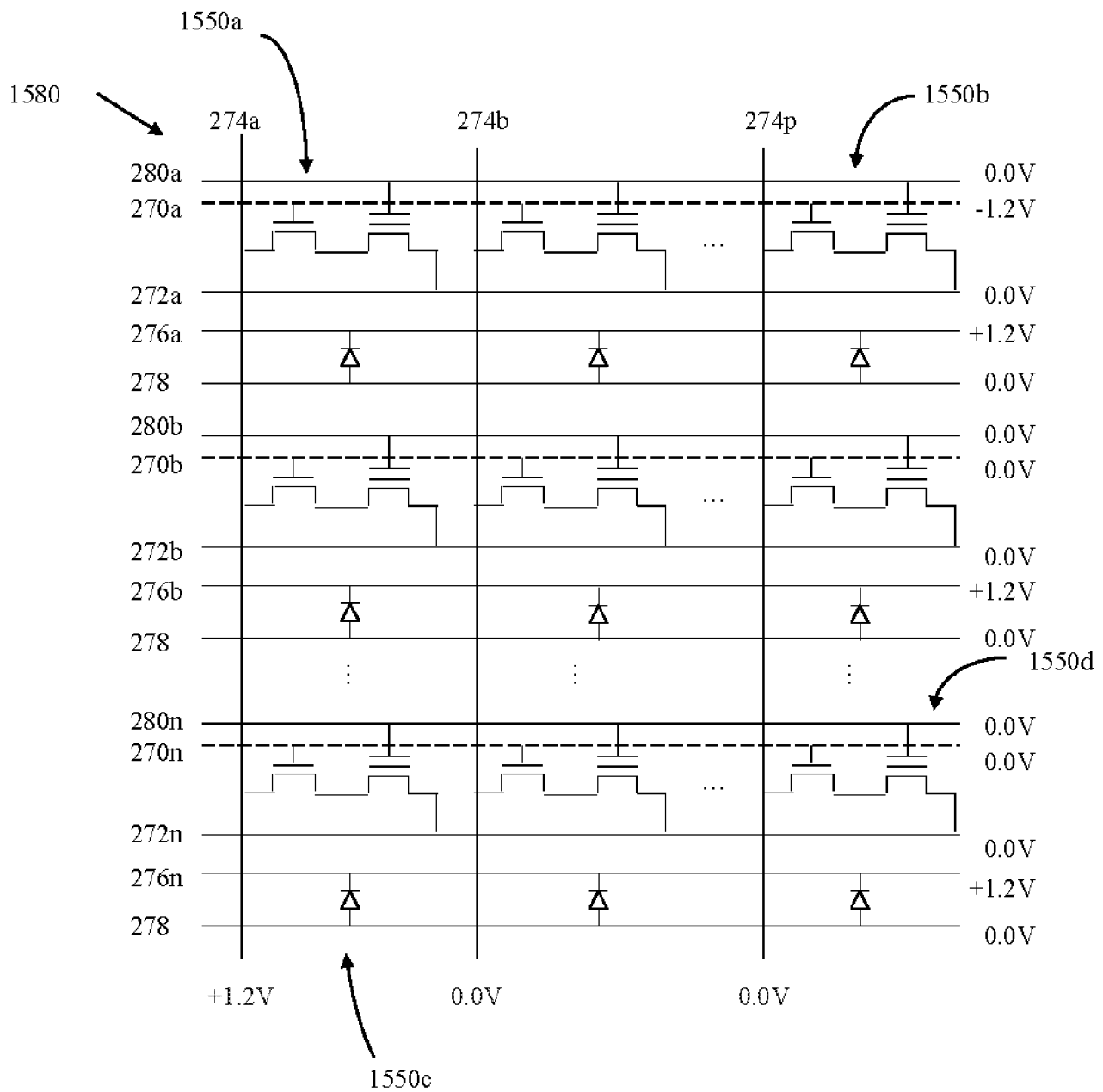


FIG. 222A

Write Logic-1 Operation (Memory Cell 1550a)

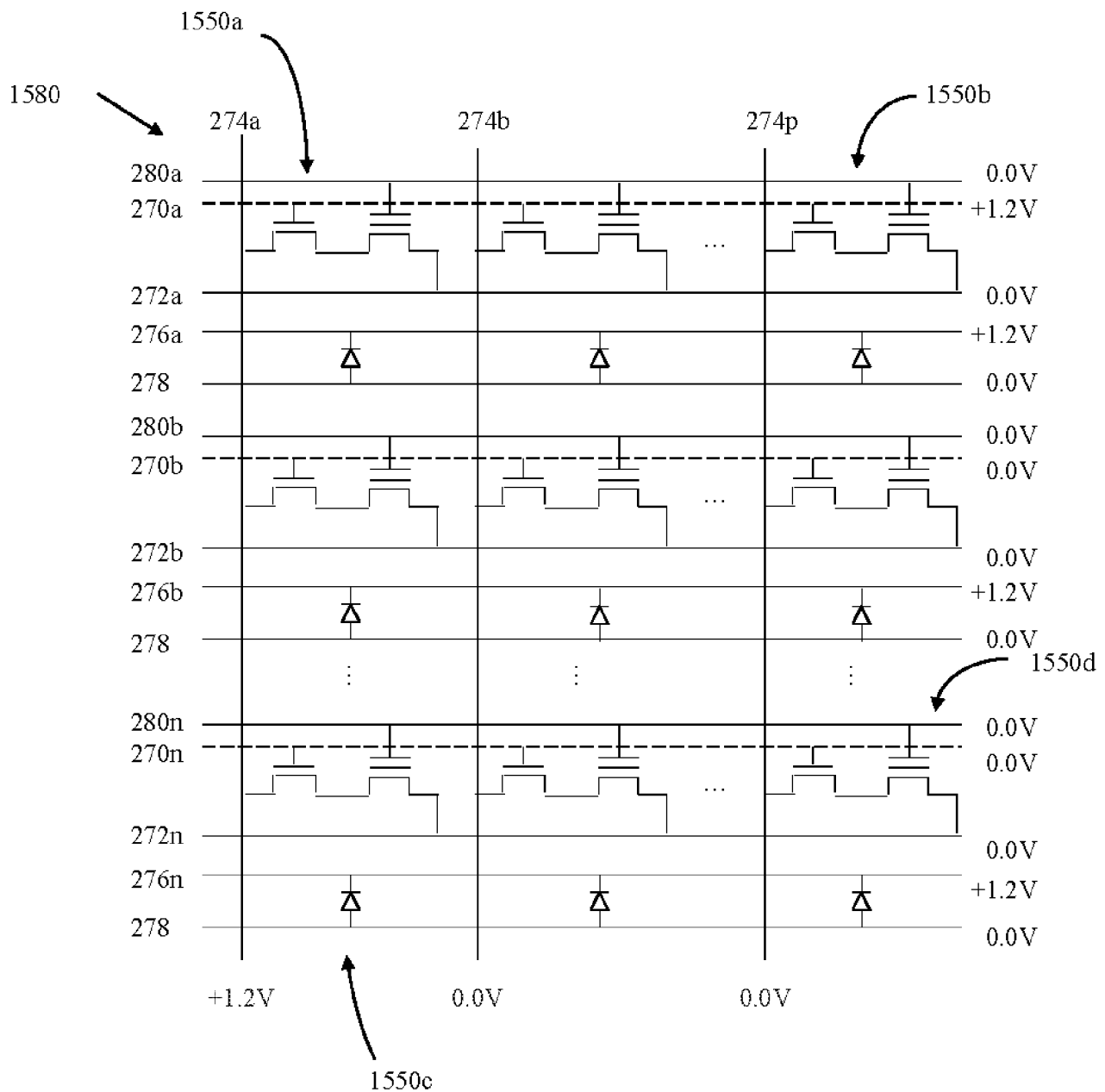


FIG. 222B

Shadowing Operation (All Memory Cells 1550)

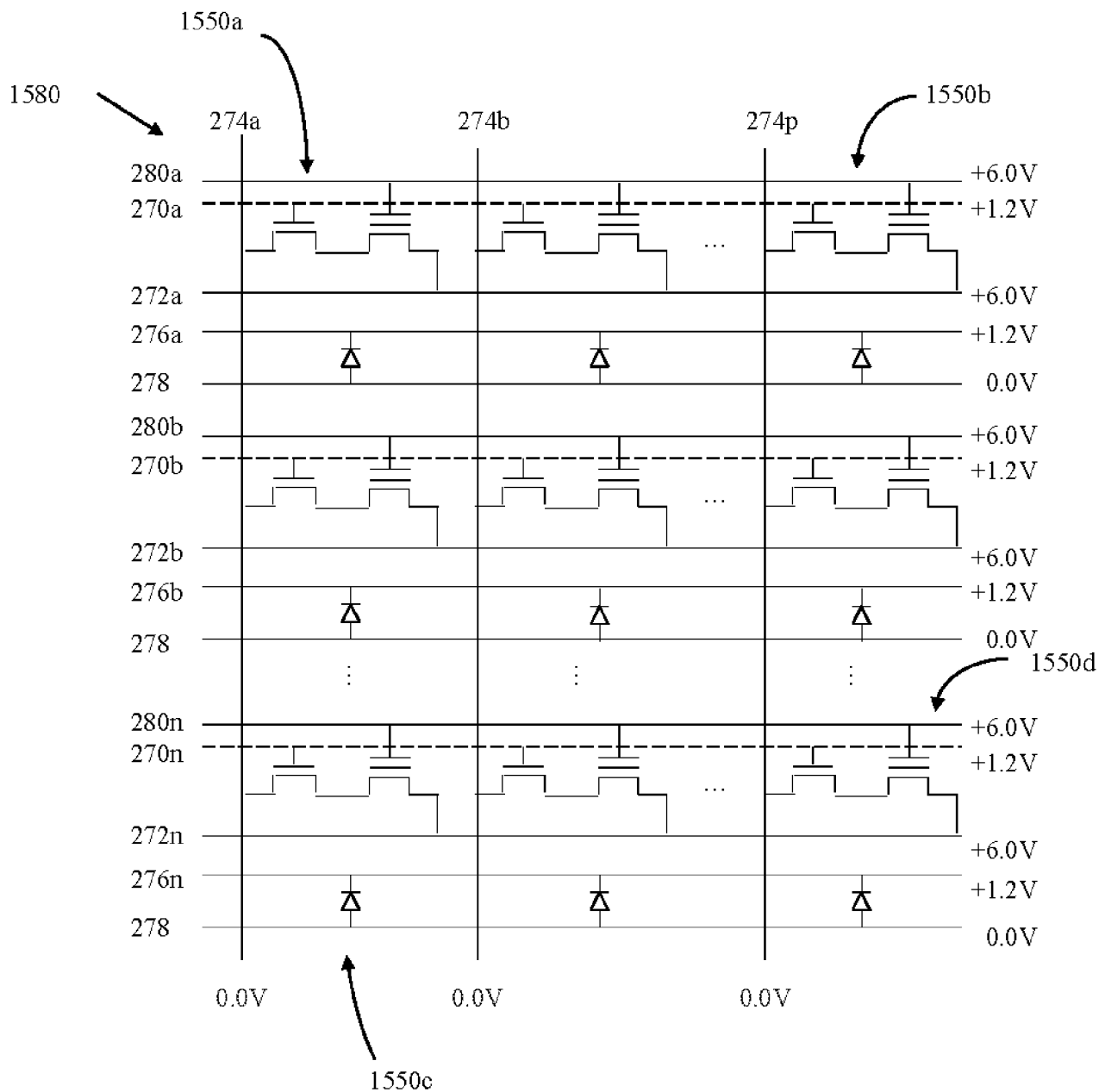


FIG. 223A

Shadowing Operation (All Memory Cells 1550)

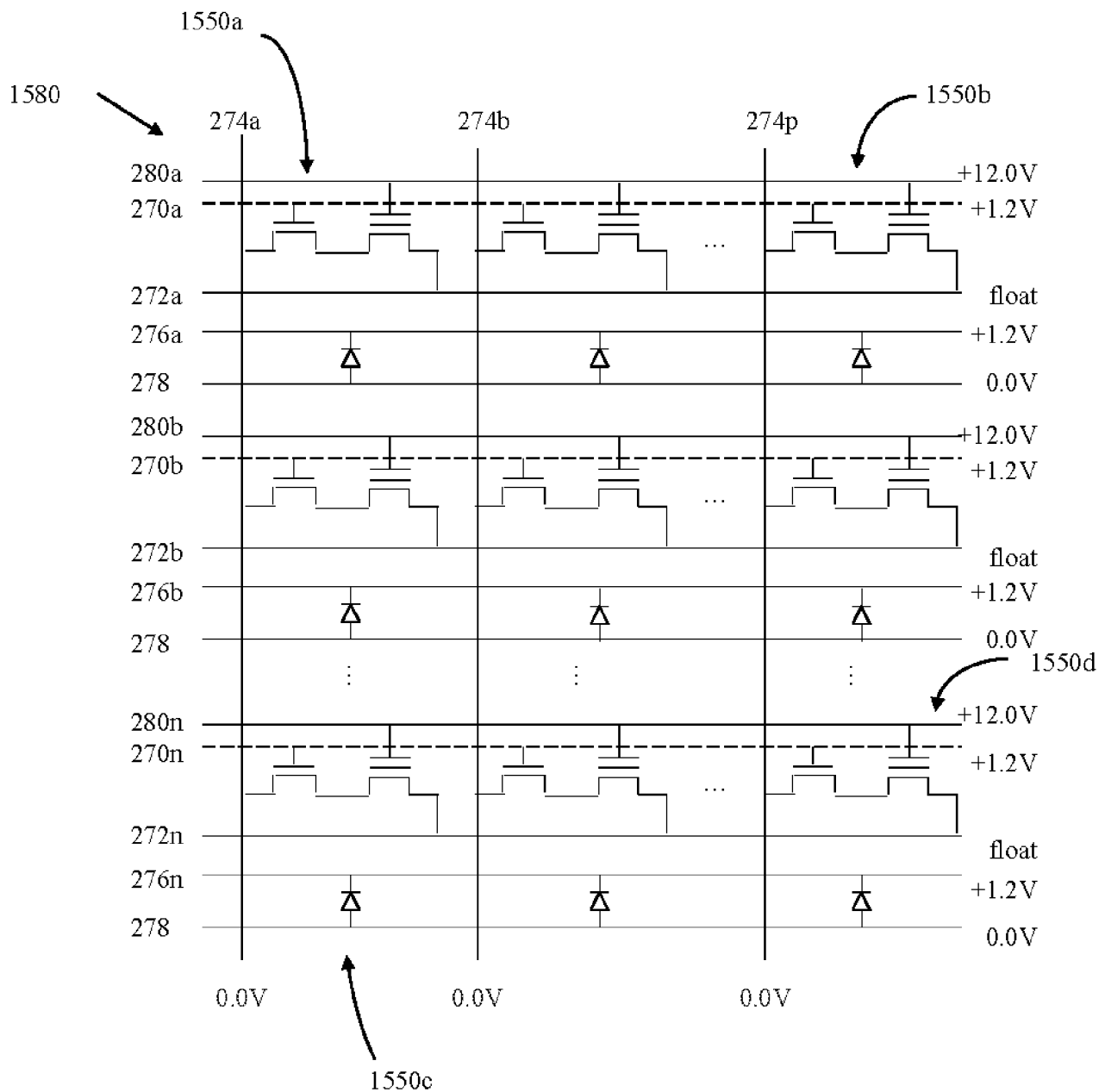


FIG. 223B

Restore Operation (All Memory Cells 1550)

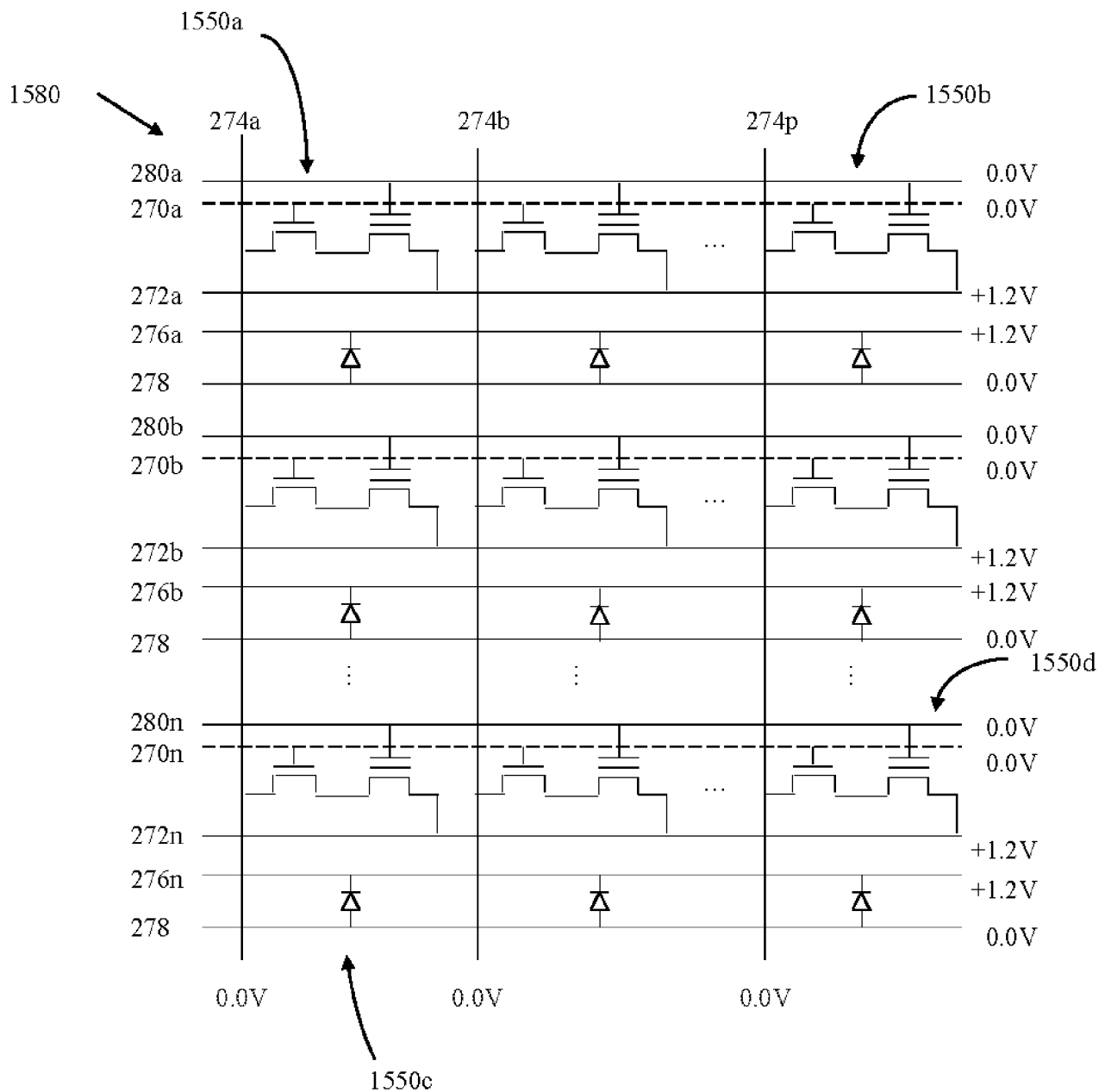


FIG. 224

Reset Operation (All Memory Cells 1550)

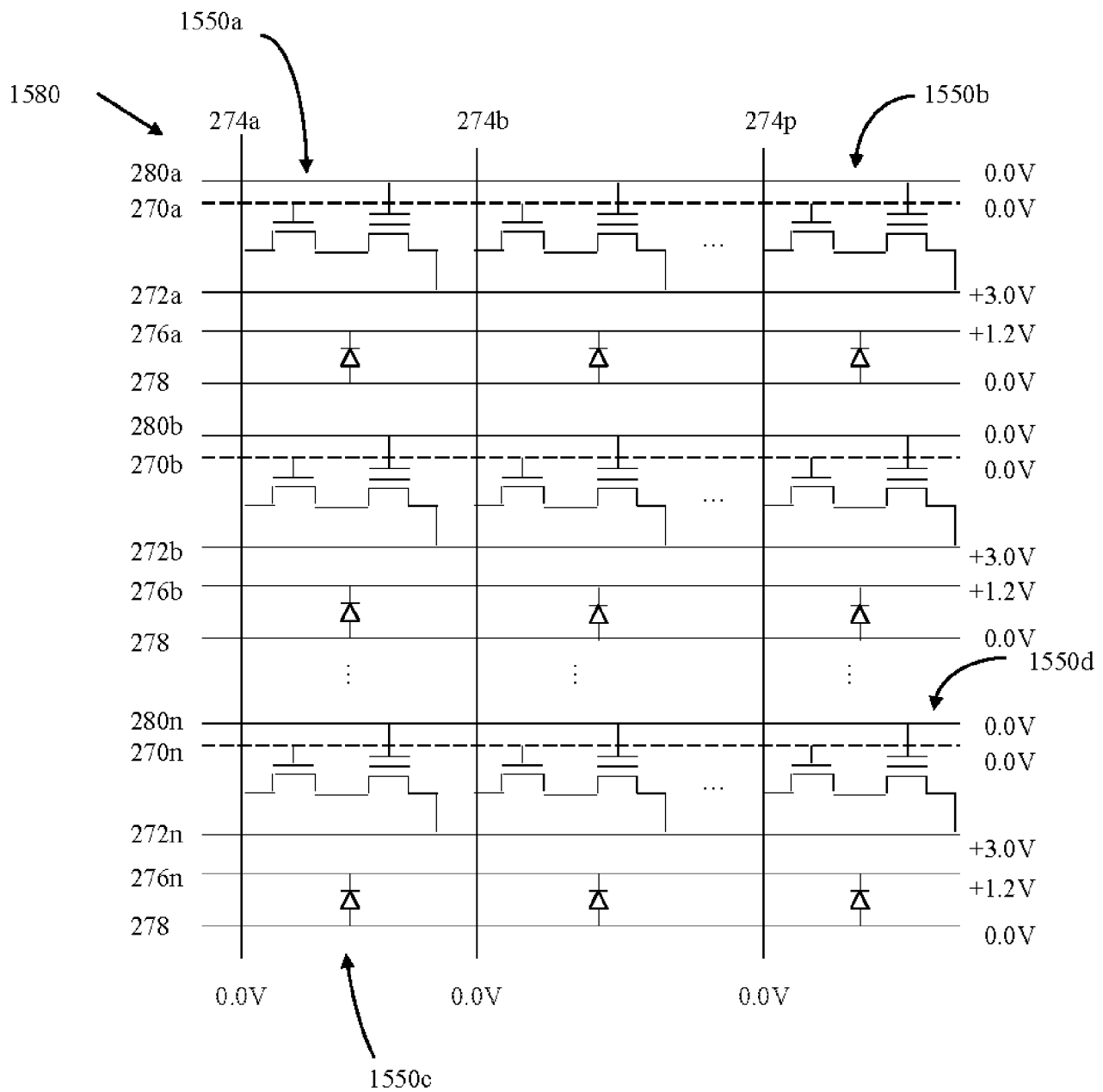


FIG. 225A

Reset Operation (All Memory Cells 1550)

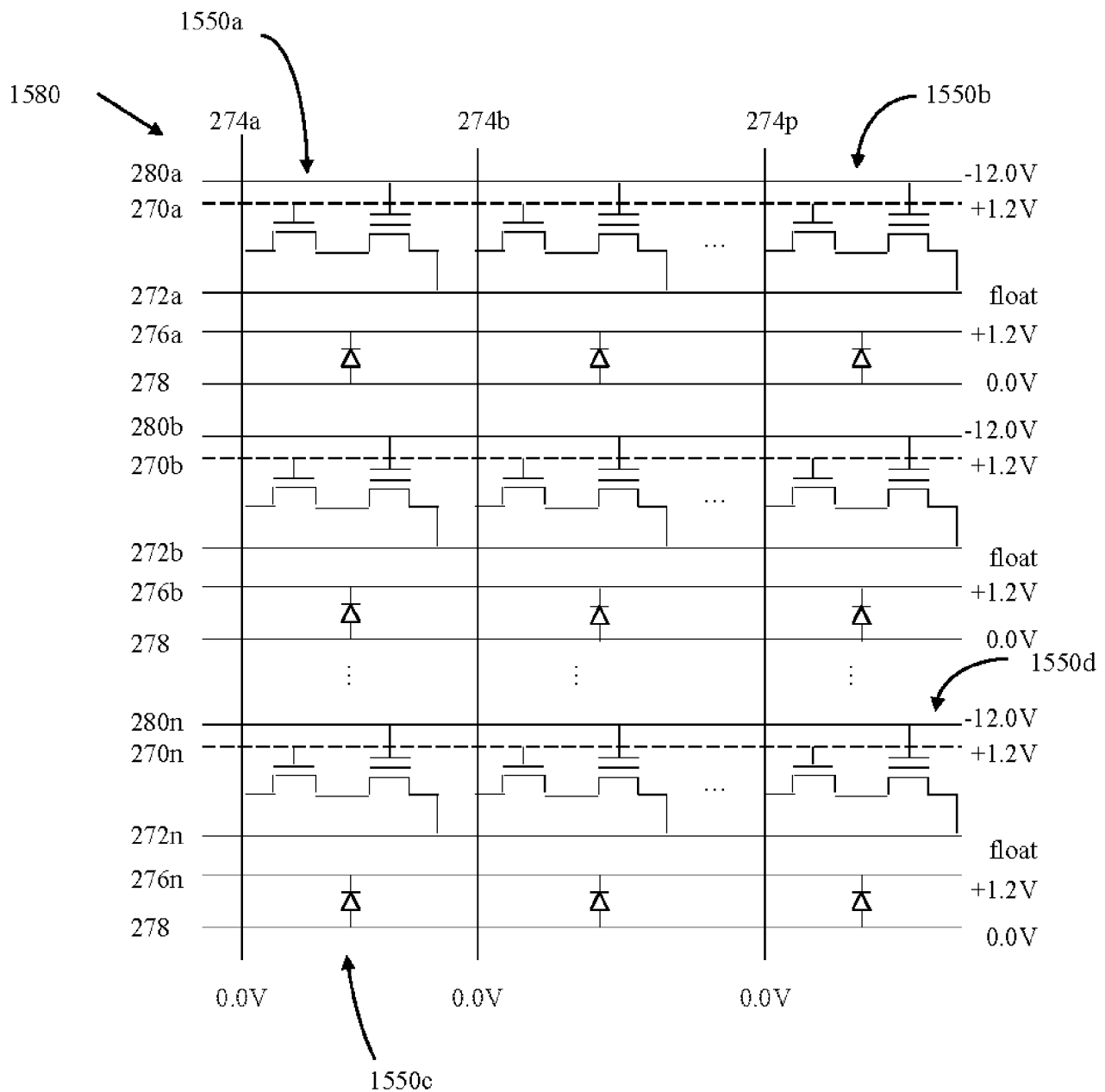


FIG. 225B

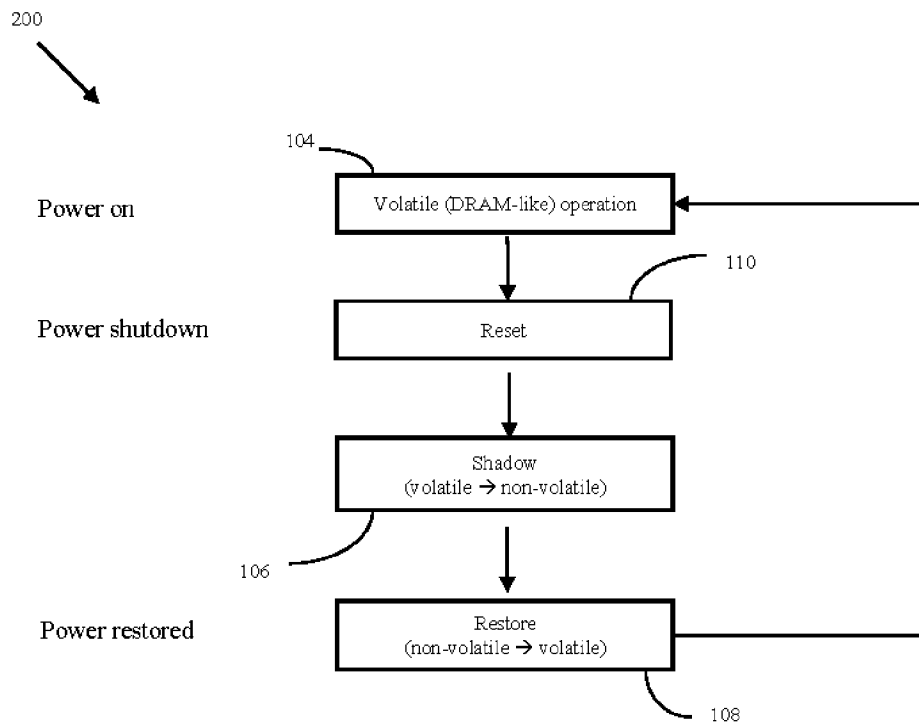


FIG. 226

Read Operation
(Memory Cell 1550a)

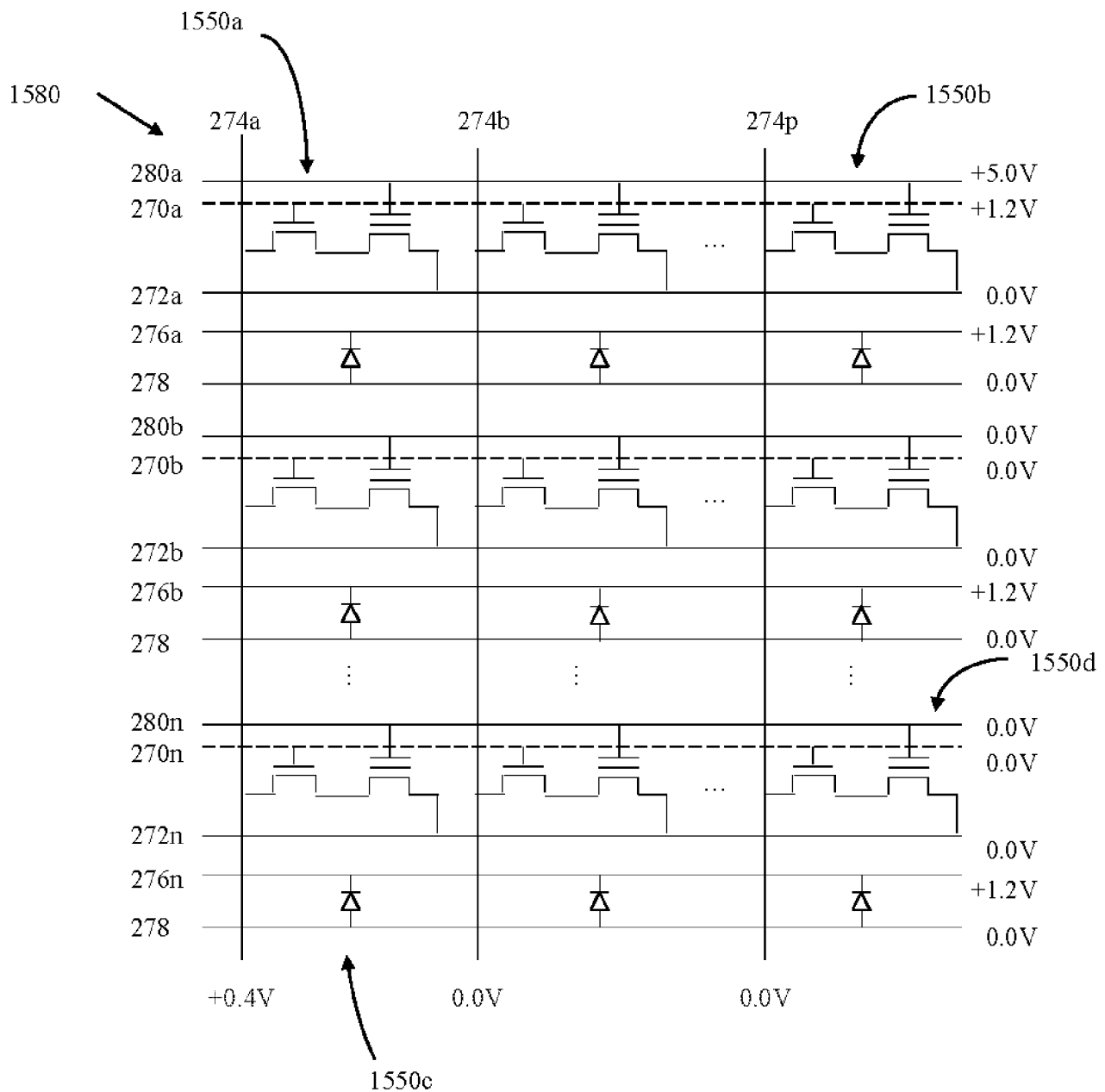


FIG. 227

Write Logic-1 Operation (Memory Cell 1550a)

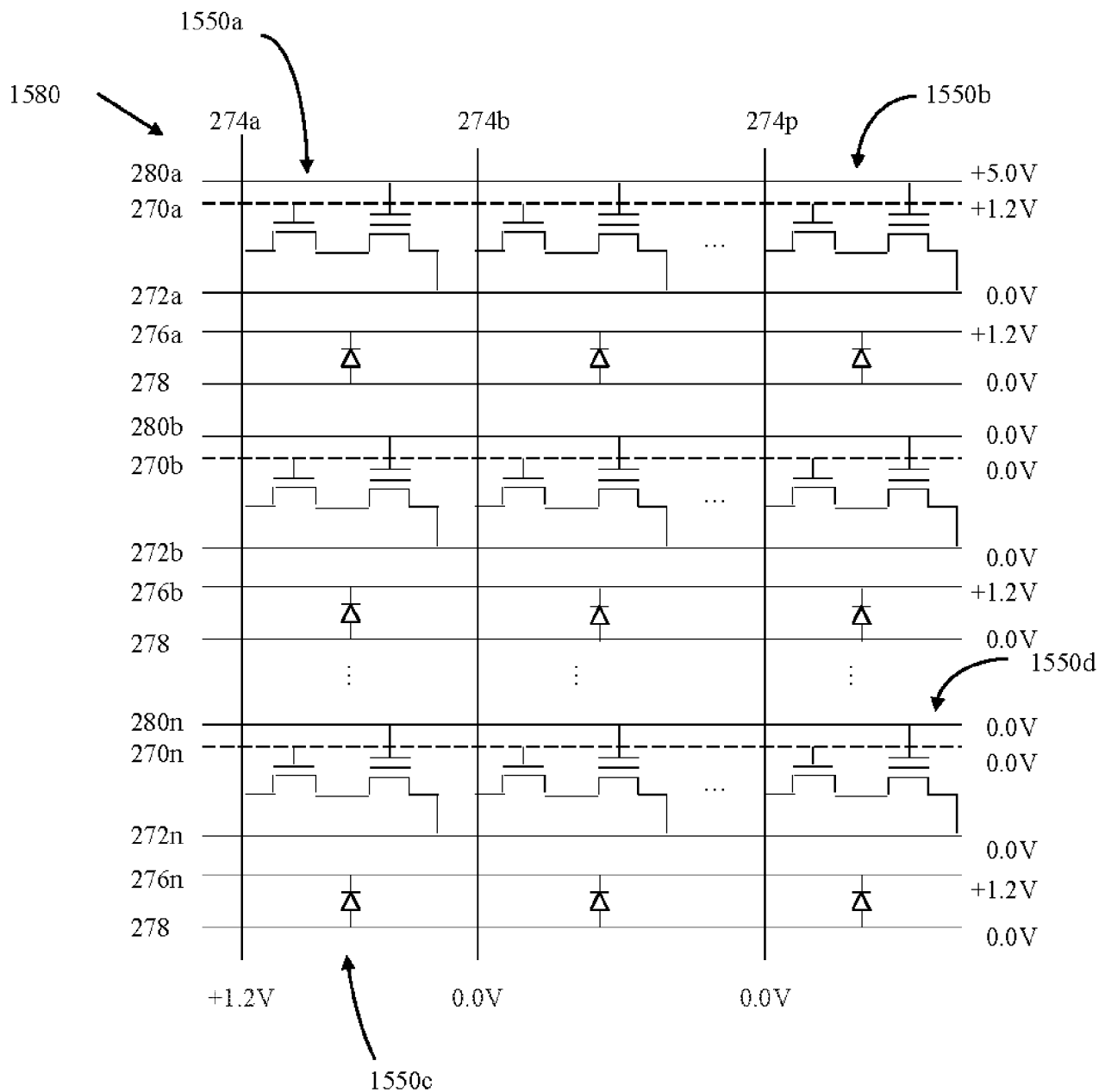


FIG. 228

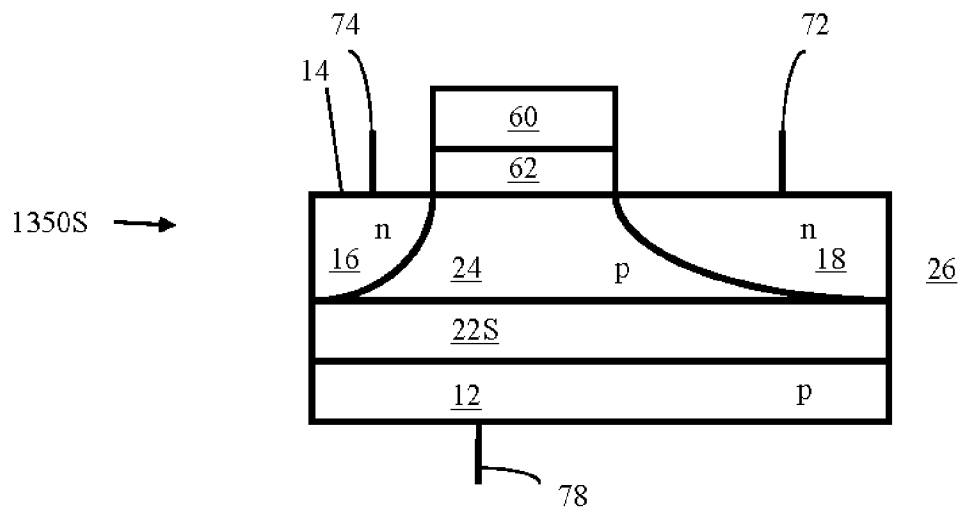


FIG. 229A

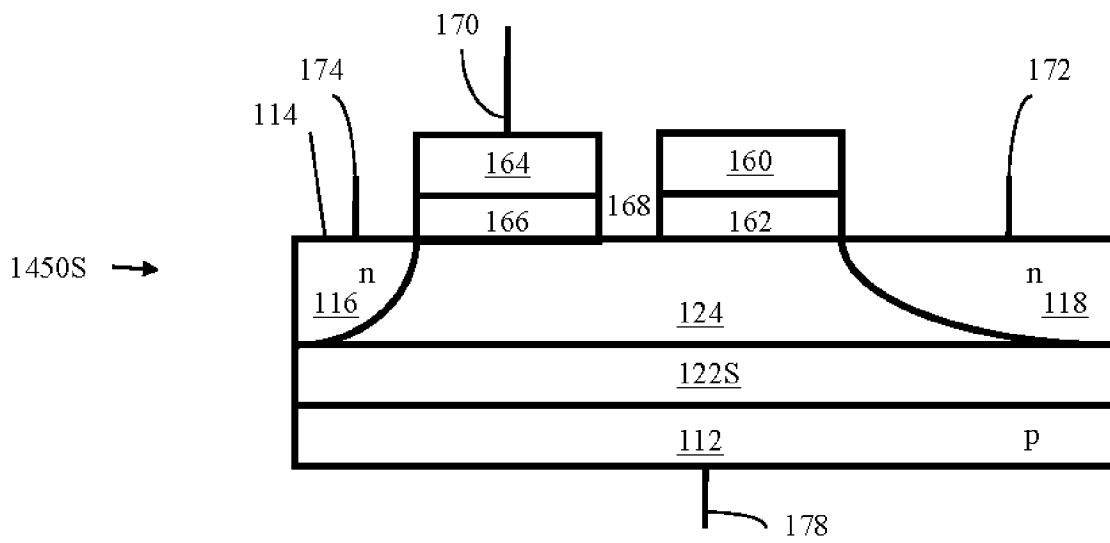


FIG. 229B

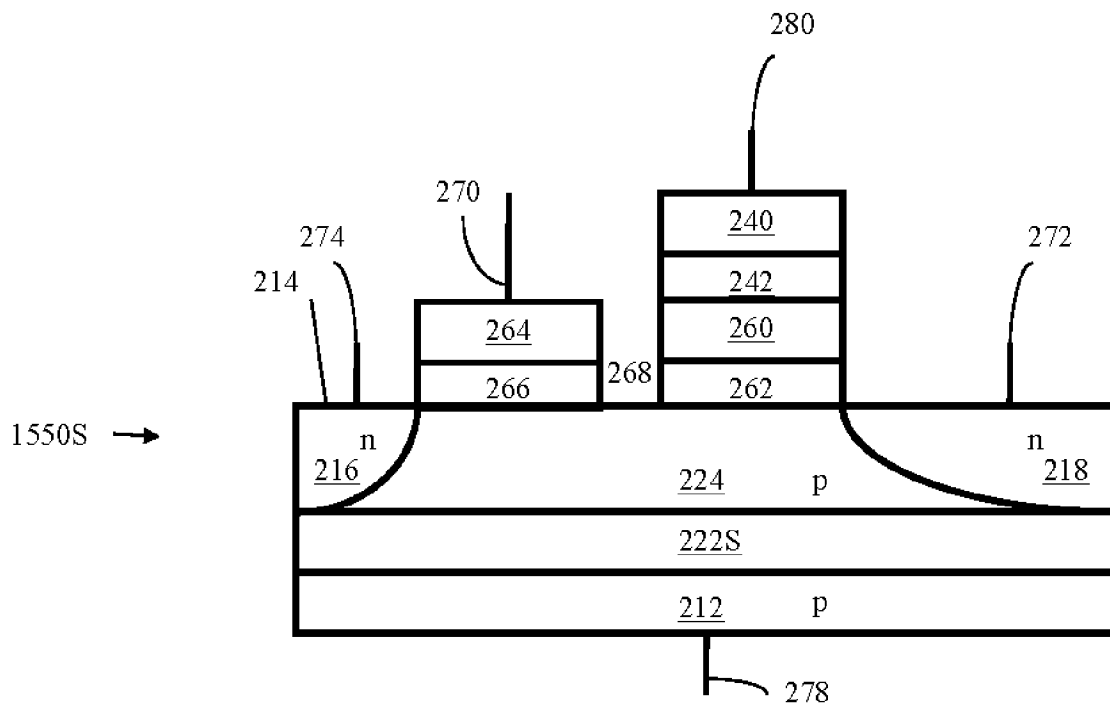


FIG. 229C

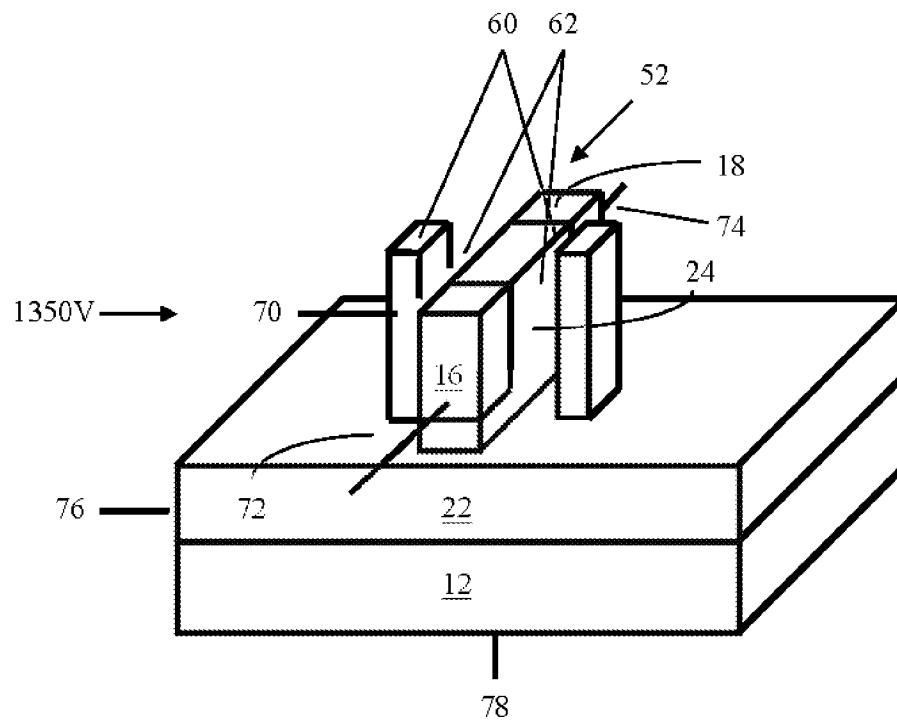


FIG. 230A

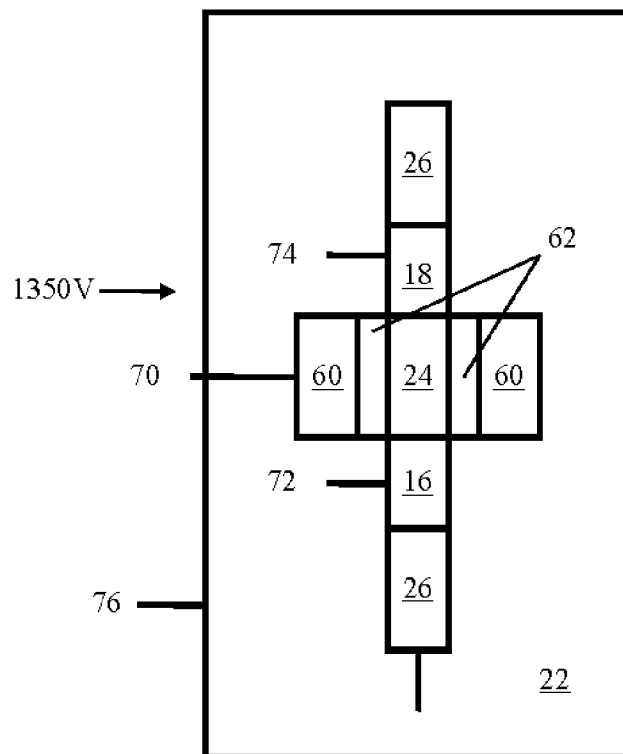


FIG. 230B

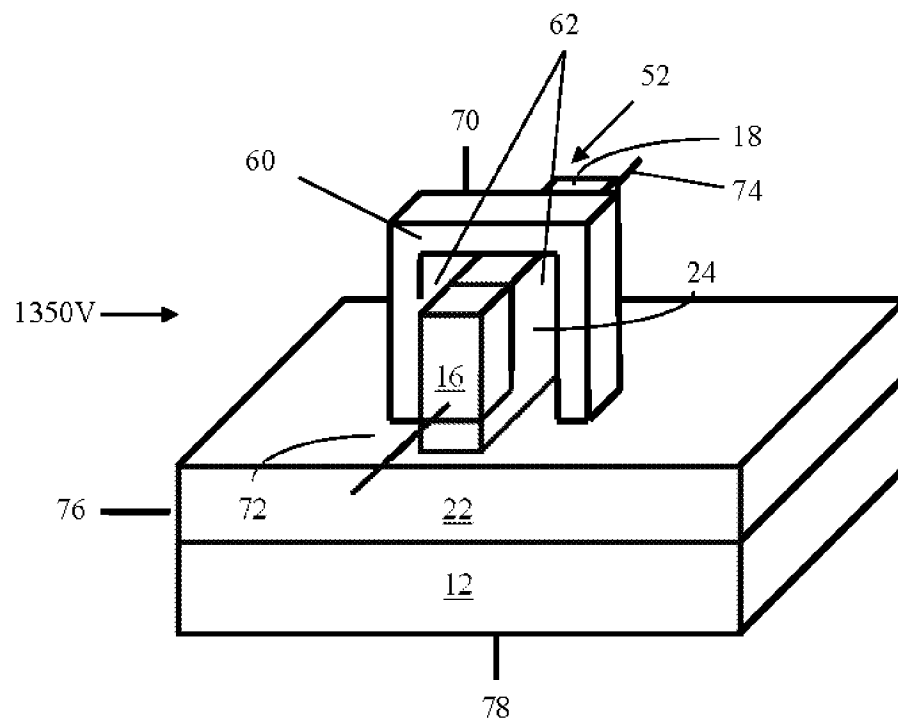


FIG. 230C

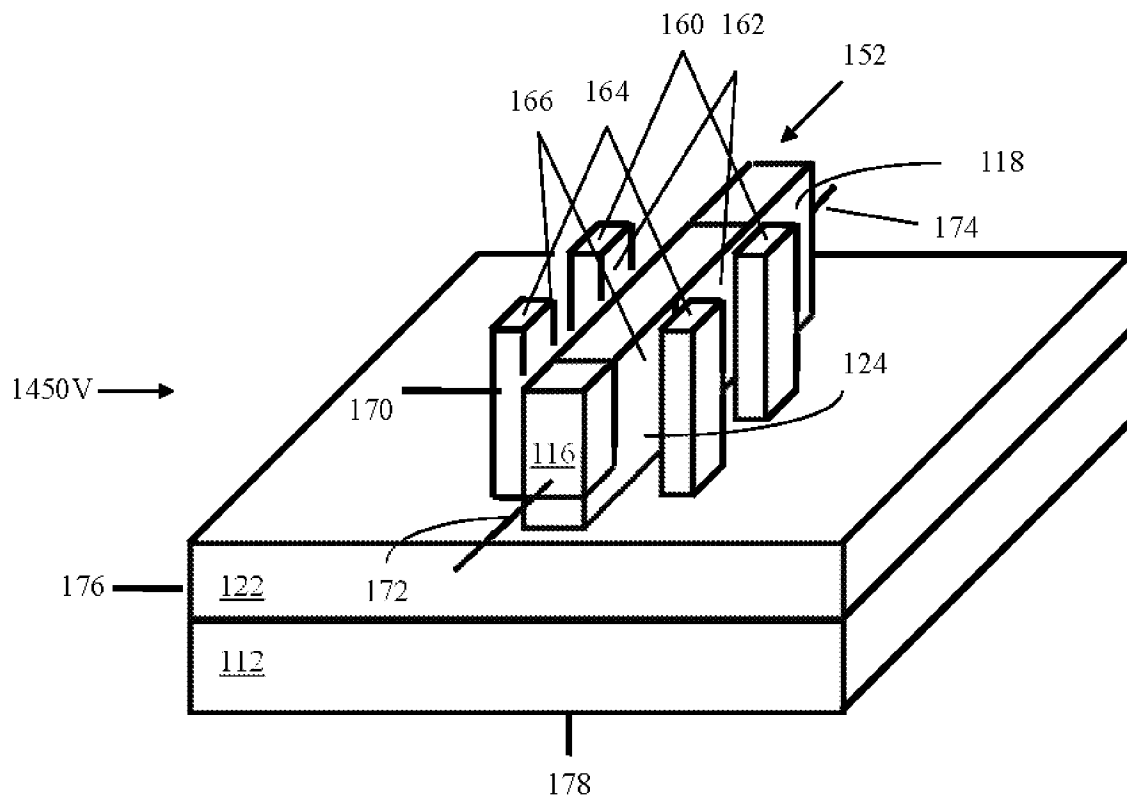


FIG. 230D

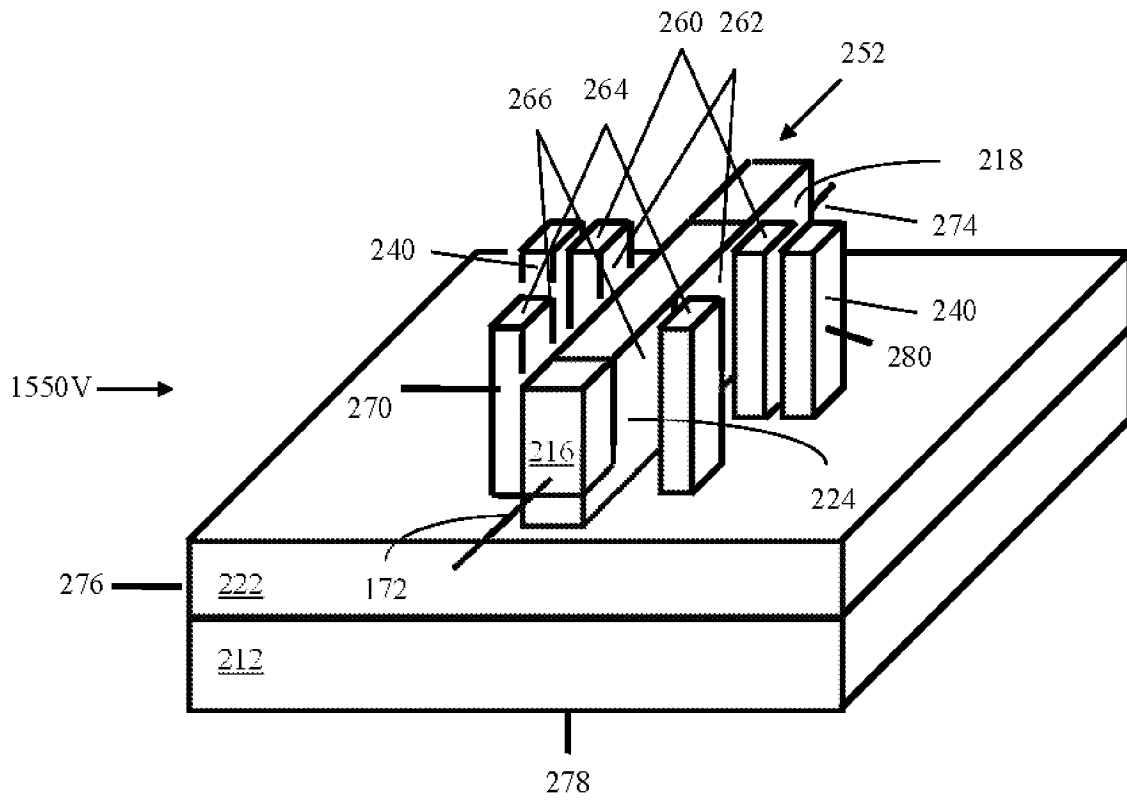


FIG. 230E