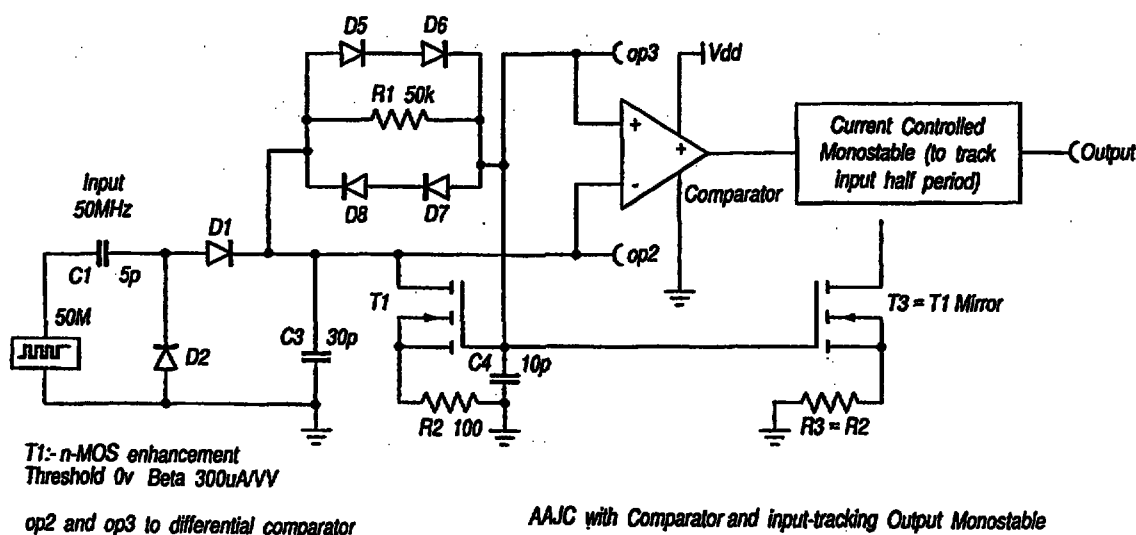


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(54) Title: ANTI-JITTER CIRCUITS**(57) Abstract**

An anti-jitter circuit has an integrator storage capacitor (C3). A charge pump (C1, D1, D2) derives from an input pulse train at least one charge packet during each cycle of the input pulse train and supplies the charge packets to the storage capacitor (C3). A controlled current sink (T1) operating in conjunction with a high impedance low pass filter (R1, C4) continuously discharges the storage capacitor (C3) to create a sawtooth voltage waveform (Op2) having a mean d.c. voltage level (Op3). A differential comparator compares the sawtooth voltage waveform (Op2) with the mean d.c. voltage level (Op3) and the comparator output is used to trigger a monostable circuit to generate an output pulse train having reduced time jitter.