

**Process and circuit for regeneration of the binary bit
stream from a ternary signal**

The invention is based on a process according to the precharacterizing clause of Claim 1. Such a process is used, for example, in "Viterbi detection" and is described in more detail in "IEEE Transactions on Communications", Vol. Com-34, Nr. 5, May 1986, pages 454 - 461. In the case of this known bit regeneration, a reduction in the error rate which corresponds to an improvement in the signal-to-noise-ratio of the order of magnitude of 1 - 3 db [sic] is achieved in comparison with circuits with a straightforward threshold detector.

The invention is based on the object of specifying a process for the regeneration of the binary signal which has, like the said known regeneration, increased noise immunity in comparison with a threshold detector, but can be realized by means of simpler circuits.

This object is achieved by the invention specified in Claim 1. Advantageous developments and circuits for carrying out the process are specified in the subclaims.

The process according to the invention thus makes possible circuits which have the advantages of the known Viterbi detection with regard to error rate or signal-to-noise-ratio, but manage with less complex circuitry.

The known Viterbi detection and the invention are explained below with reference to the drawing, in which:

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| Fig. 1 | shows a block diagram of the overall arrangement, |
| 30 Fig. 2 | shows curves for explaining the signals occurring during tape scanning and bit regeneration, |
| Fig. 3 | shows a block diagram of the circuit according to the invention, |
| 35 Fig. 4 | shows an excerpt from Fig. 3, |
| Fig. 5 | shows curve shapes for explaining the operating principle of the circuits |

according to Figs. 3, 4 and
Tab. 1 shows a code table of the A/D converter
used in Fig. 3,
Figs. 6,7,8 show explanations of how the so-called PR4
5 signal is produced,
Fig. 9 shows an example of a circuit for the
development of the invention for a PR4
signal
Fig. 10 shows an excerpt from the circuit
10 according to Fig. 9

Fig. 1 shows the block diagram of a circuit for
the recovery of the bit stream recorded on a magnetic
medium and Fig. 2 shows the associated signal waveforms.
The magnetic track M contains the bit pattern in binary
15 form, i.e. in the form of oppositely magnetized regions,
as is indicated by the symbols N (north pole) and S
(south pole). In the playback head, the reproduction
voltage is induced by the changes in flux between the
regions N and S or S and N. This voltage approximately
20 represents the differentiated bit pattern. The pulses
generated by the transitions in magnetization are
narrowed in the equalization circuit P or freed of
influences of neighbouring bits. The obtaining of the
original bit stream from the equalized signal E in the
25 circuit part G can be performed in various ways, for
example by integration, zero-crossing detection and
sampling with the bit clock regenerated by a PLL circuit.
The advantage of this process is that the integration
from the ternary signal E has the effect of generating a
30 signal whose evaluation with the zero-crossing detector
is largely level-independent. Whenever the binary signal
contains very low-frequency spectral components and great
run-length values, it is more favourable to evaluate the
ternary signal E directly with a level decision element.
35 A Schmitt trigger which alternately senses the positive
and negative pulses may be used, for example, as the
level decision element. In order to maintain the optimum
trigger points, however, an automatic gain control is
required for the ternary signal E. The binary output

signal of the Schmitt trigger is sampled to determine the ultimate position of the level transitions with the regenerated bit clock. An improvement in the noise immunity can be achieved in the case of the signal evaluation with the known Viterbi detection of the ternary signal E, mentioned at the beginning. In the case of this known circuit, the signal is preferably processed in two circuit branches. For this purpose, the signal is sampled alternately by two A/D converters. Apart from the A/D converter, each branch includes various registers, comparators, adders and a RAM with addressing device.

There follows a description of a circuit for regeneration of the bit stream from the ternary signal which likewise has increased noise immunity in comparison with a straightforward level decision element, but manages with significantly less complex circuitry. Apart from an A/D converter, just a few registers and two comparators are required.

Fig. 3 shows the block diagram of such a bit-stream regenerator, Fig. 5 shows a number of associated signal waveforms. The equalized ternary signal E is sampled with the aid of the regenerated bit clock by the A/D converter 1. The sampling instants are set by the phase control of the clock regeneration circuit (PLL) approximately to the pulse peaks of the signal E.

Table 1 shows in extract form the table for the digital output code of the A/D converter used here. The MSB represents in this case the operational sign, while the remaining $n-1$ bits indicate the absolute amount A of the sampled values. It is expedient to use the MSB (most significant bit) for the bias control at the input of the A/D converter. For this purpose, a voltage generated from the mean value of the MSB's and amplified is set back via the low-pass filter 2 to the A/D converter input. The setting is in this case such that the "0s" and "1s" occur approximately with the same frequency as MSB's.

The comparators 3 and 4 respectively investigate

only the absolute amount A of the sampled values. The comparator 3 establishes thereby whether the sampled value A succeeds a predetermined threshold S. The comparator 4 serves for determining the maximum sampled value by the time the threshold is next exceeded with the opposite operational sign. The maximum value determined in each case is stored in the register 5.

Each time the threshold is exceeded, the outputs of the gates 6 and 7, in dependence on the operational sign (MSB), supply a negative pulse to one of the inputs of the R-S flip-flops formed by the gates 8 and 9. The output signal D of the flip-flops 8, 9 corresponds to the signal regenerated by a straightforward threshold detector. The level transitions of the signal D occur whenever the first exceeding of the threshold takes place with a changed operational sign. With a noise-free signal E, successive instances of exceeding the threshold have a changing operational sign, i.e. each sampled value A which exceeds the threshold S belongs to a level transition of the original bit stream. If there are successive instances of exceeding the threshold with the same operational sign, the sampled value will correspond with a high probability to the greatest amplitude of the actual level transition. The remaining instances of exceeding the threshold are attributable to disturbances. The circuit according to Fig. 3 thus serves for determining the probably correct level transitions when signal disturbances occur. The correction register 10 permits a subsequent correction of the bit stream D.

The bit stream D is read into the correction register 10 via the D flip-flop 15. An arrangement for the correction register 10 is represented in Fig. 4. The length of the two shift registers 11 and 14 corresponds to the maximum run length of the signal, since any required level transition shifts do not exceed the spacing of the actual level transitions. The bit transport in the shift register 11, which contains the last m bits in each case of the sampled bit stream, takes place by means of EXOR gates 12, which if need be permit

the inversion of part of the bit stream. The register 14 is reset clock-synchronously at each initially determined level transition and, between the level transitions, is set stage by stage with the bit clock. By means of the AND gates 13, the inversion of the bits in the shift register 11 can be triggered in a manner corresponding to the stages set in the shift register 14.

Each level transition of the signal D generates at the output of the EXOR gates 16 a positive pulse T of the duration of one bit. The OR gate 17 has the effect that the register 5 is loaded with the current sampled value not only when an increase in the sampled value is established, but also at each level transition of the signal D.

The gate 18 has the effect that, on establishing an increase in the sampled value which is not associated with a level transition, the inversion of a series of bits takes place in the correction register 10. The signal C required for this purpose is delayed by one bit with the aid of the D flip-flop 19 to adapt the timing.

The gate 20 has the effect that the register 14 in the correction circuit 10 is reset at each level transition T or at each level transition shift carried out for the purpose of signal correction.

The possibility exists of adapting the threshold S automatically to the signal level and to the signal quality. An increased frequency of the pulses Co means that the threshold S is set too low. A threshold S set too high has the effect that some level transitions are no longer sensed. As a result, a change in the run-length statistics of the signal takes place in favor of the higher run-length values, or there occur instances of a signal limited in run length exceeding the maximum run length. With the aid of a logic circuit 21, this information can be utilized for the automatic optimization of the threshold S. By means of this logic circuit, the reference voltage V Ref of the A/D converter can also be set. Consequently, it may be possible to dispense with automatic gain control for the input signal E.

In the case of the circuit described here, bit errors occur only when a value A caused by a disturbance is greater than the value of the neighbouring level transition or if a disturbance-induced exceeding of a threshold is followed by a further disturbance-induced exceeding of the threshold with an opposite operational sign. Threshold optimization makes this event relatively improbable. Consequently, the circuit brings about an improvement in the noise immunity in comparison with a straightforward threshold detector.

In Fig. 3, the circuit part comprising the A/D converter 1, the two comparators 3 and 4 and the register 5 may also be designed as an analog circuit. The A/D converter and the register 5 are then substituted by sample-and-hold circuits, and the two comparators are substituted by analog comparators with binary output. An additional comparator may in this case serve for determining the operational sign of the sampled values, while, for forming the absolute amount, the ternary signal E is sent via a full-wave rectifier. The remaining circuit can remain unchanged.

Figs. 3 to 5 depict a circuit which brings about an improvement in noise immunity in the bit-stream regeneration. In the publication mentioned above, the improvement in noise immunity is achieved by a Viterbi detector, to be precise on a partial-response class IV signal (PR4).

While the high frequencies are particularly accentuated in the signal E used in Fig. 3, the medium frequency range is accentuated in particular in the case of the PR4 signal, whereby particularly good noise immunity is achieved. The generation of the PR4 signal is diagrammatically explained in Figs. 6 and 7. The signal E in Fig. 3 corresponds to a signal which has arisen from the bit stream Din by the transfer function $1 - D$, D being the signal delay by the duration of one bit. By multiplication with the transfer function $1 + D$, the PR4 signal is then obtained (see Figs. 6 and 7). It is evident that the PR4 signal has less bandwidth than

the signal E.

The PR4 signal may also be generated directly by the circuit indicated on the right in Fig. 6 with the transfer function $1 - D^2$. The PR4 signal is a ternary signal with the level values 1, 0, -1. By forming the absolute amount, a binary signal P can be obtained from this signal. The signal P corresponds to a signal which has been generated by the circuit indicated on the right in Fig. 8 from the signal Din. In this circuit, the input signal Din is combined with the signal delayed from [sic] 2 bit clocks in an EXOR gate. This signal change can be cancelled by a precoding with the aid of the circuit indicated on the left in Fig. 8 (Dout in Fig. 7).

In the circuit according to Fig. 3, the special characteristic that, in the signal E, positive and negative pulses always occur alternately was utilized for the error correction. This is no longer the case with the PR4 signal, as Fig. 7 shows. Deviations from this rule occur if the number of directly successive half-waves of the length of a bit in the binary input signal Din is even. Fig. 7 also shows, however, that the PR4 signal comprises two pulse sequences which conform to the above rule, combined in time-division multiplex. In Fig. 7, negative and positive pulses always occur alternately both in the sequence of all the bits denoted by "1" and in the sequence of all the bits denoted by "2". Consequently, the possibility exists of also processing a PR4 signal with the aid of a correction circuit corresponding to Fig. 3. For this purpose, the PR4 signal is demultiplexed before or after the A/D converter and, as in the case of Viterbi detection, is processed in two parallel branches according to Figs. 3 to 5. Thereafter, the signal is combined again by a multiplexer.

With a circuit according to Figs. 9 and 10, the PR4 signal can also be processed directly in time-division multiplex. The extra circuitry in comparison with the processing circuit for the signal E is then simply as follows: the RS flip-flop 6 to 9 is [sic] duplicated. The delay in the register 5 and at the points 15 and 19

is in each case 2 bit clocks, i.e. there are two D flip-flops sampled with the bit clock connected in series per signal path. The flip-flop 22 generates the switching voltage U, which ensures that the inputs of the RS flip-flops 8, 9 and 8', 9' are activated alternately bit by bit and that the output voltages of the RS flip-flops 8, 9 and 8', 9' are fed to the further processing circuit alternately bit by bit via the changeover switch 23.

In the case of the correction register 10, the complexity is even reduced, since only every second stage of the shift register 11 is coupled via an EXOR gate to the following stage. In the case of the register 14, likewise only every second stage is synchronously reset.

The correction register 10' represented in Fig. 10 has three correction stages. Therefore, signal half-waves up to a run length of 4 double bits, i.e. 8 bits, can be corrected. The signal example of Fig. 7 shows that run-length increases may arise in the partial signals formed from even-numbered or odd-numbered sampled values of the PR4 signal. However, it is not absolutely necessary to increase the length of the correction register correspondingly. Since the majority of the level-transition shifts to be corrected amount to only a few bits, a good corrective effect can be achieved with just a relatively short correction register.

The pulse spacing in the two partial signals 1 and 2 of the PR4 signal (Fig. 7) determines the duration of error propagation owing to an incorrect decision. Error propagation is in any event ended with the next correctly detected level transition.

The circuit according to Figs. 9 and 10 effects a restoration of the bit pattern Din, which is for example the bit pattern on a recording medium. If this bit pattern was generated by a precoding, for example according to Fig. 8, on the left, the original bit pattern must be restored by an additional recoding (according to Fig. 8, on the right). As Fig. 10 shows, this recoding circuit may be combined with the correction register.

The recoding according to Fig. 8, on the right, generates from an erroneous bit only a double bit error, thus causes virtually no error propagation. The circuit according to Figs. 9 and 10 is therefore suitable both for signals with and without precoding. By contrast, the known detection circuits for PR4 signals generates from the signal Din the signal P. In order to obtain the signal Din, the recoding circuit represented on the left in Fig. 8 would have to be connected downstream of the detection circuit. However, this circuit causes unlimited error propagation even if there is just a single bit error. Therefore, it is usual to use this recoding as a precoding before the signal transmission. The known signal-transmission devices with PR4 detection require this precoding. By contrast, the PR4 detection process according to Figs. 9 and 10 is independent of the precoding. This means that this process can also be used for transmission codes which do not use any 2T precoding according to Fig. 8, on the left. Such transmission codes are used, for example, in the case of CD and R-DAT.

Patent Claims

1. Process for regeneration of the binary bit stream from a ternary signal (E), which has been obtained by scanning a binary recording track and comprises pulses which are alternately positively and negatively directed with respect to a centre line, sampled values being obtained from the pulses with the aid of an A/D converter clocked with the regenerated bit clock, characterized in that there is a threshold (S) in each case for the sampled values of the positive pulses and negative pulses, in that each instance of exceeding the threshold with a operational sign which has changed with respect to the preceding instance of exceeding the threshold is initially assessed as a level transition of the binary bit stream, and in that if there are a plurality of instances of successive exceeding with the same operational sign, the sampled value with the greatest exceeding of the threshold determines the ultimate position of the level transition.
2. Circuit for a process according to Claim 1, characterized in that in the output code of the A/D converter (1) the MSB indicates the operational sign and the remaining bits indicate the absolute amount of the sampled values (Tab. 1).
3. Circuit according to Claim 2, characterized in that the bias at the analog input of the A/D converter (1) is controlled with the aid of the MSB such that positive and negative sampled values occur approximately with the same frequency.
4. Circuit for determining the greatest exceeding of a threshold for a process according to Claim 1, characterized in that the absolute amount (A) of the current sampled value is compared in a comparator (4) with the absolute amount (B) stored in the register (5), and in that whenever the threshold is exceeded with a change of operational sign whenever an increase in the absolute amount is established, the register (5) is loaded with the absolute amount of the current sampled value (A).



5. Circuit for a process according to Claim 1, characterized in that, for generating the provisional binary bit stream (D), there is provided a flip-flop (8, 9) whose output is set to the value corresponding to the operational sign in instances of exceeding the threshold.

6. Circuit according to Claim 5, characterized in that the provisional bit stream (D) is read into a correction register (10) which is clocked with the bit clock and whose length corresponds approximately to the maximum run length of the bit stream to be regenerated.

7. Circuit according to Claim 6, characterized in that in the correction register the bit transport takes place in a first register (11) by means of EXOR gates (12), in that there is provided a second shift register (14), which is set stage by stage with the bit clock and is reset each time the threshold is exceeded with changed operational sign, and in that where there are increases in the sampled value without a change in operational sign the bits in the first register are inverted by means of the EXOR gates in a manner corresponding to the stages set in the second register, and the second register is likewise reset.

8. Circuit for a process according to Claim 1, characterized in that the threshold value (S) fed to the comparator for determining the instances of exceeding the threshold (3) is adapted with the aid of a logic circuit (21) to the signal (E) to be processed.

9. Circuit according to Claim 8, characterized in that the logic circuit (21) processes the correction frequency (Co) and/or the run-length values of the uncorrected bit stream (D).

10. Circuit according to Claim 9, characterized in that the logic circuit sets the reference voltage (V Ref) of the A/D converter.

11. Circuit according to one or more of the preceding claims, characterized in that the A/D converter (1) and the register (5) are substituted by sample-and-hold circuits, and in that the comparators (3, 4) for determining the instances of exceeding the threshold and for





determining the maximum exceeding of the threshold have analog inputs and binary outputs.

12. Process for regeneration of the binary bit stream from a ternary signal (PR4), characterized in that a plurality of value sequences which correspond to signals whose pulses are alternately positively and negatively directed with respect to a centre line are formed by demultiplexing the sampled values of the ternary signal, in that each sample sequence is processed in a circuit according to one or more of the preceding claims, and that thereafter the individual signals are combined again in a multiplexer.

13. Process for regenerating the binary bit stream from a ternary signal (PR4), which corresponds to a signal which has arisen by addition of two identical signals (E) which are shifted with respect to each other by one bit duration and correspond to the precharacterizing clause of Claim 1, characterized in that the processing takes place in time-division multiplex in a circuit which corresponds to one or more of the preceding claims.

14. Circuit for a process according to Claim 13, characterized in that, for the processing of the even-numbered and odd-numbered sampled values in time-division multiplex, the RS flip-flop (8, 9) according to Claim 5 is duplicated and the register (5) according to Claim 4 is designed as a two-stage register (5').

15. Correction register according to Claim 6, for a process according to Claim 13, characterized in that in a first shift register (11) the bit transport takes place at every second stage by means of an EXOR gate (12), and in that there is provided a second shift register (14), which is set stage by stage with each bit clock, in that an inversion of the bits in the first register can be carried out by means of the EXOR gates (12) in a manner corresponding to the set stages of the second register (14), and the resetting of the second register takes place synchronously for every second stage (Fig. 10).