A Damascene Interconnect Structure With Cap Layer

TECHNICAL FIELD

[0001] This invention relates generally to metallization of the integrated circuit, and more specifically to damascene process.

BACKGROUND

[0002] Conventional integrated circuit contains a plurality of patterns of metal lines separated by inter-wiring spacings, and a plurality of interconnect lines, such as bus lines, bit lines, word lines and logic interconnect lines. Typically, the metal patterns of vertically spaced metallization layers are electrically interconnected by vias. Metal lines formed in trench-like openings typically extend substantially parallel to the semiconductor substrate. Semiconductor devices of such type according to current technology may comprise eight or more levels of metallization to satisfy device geometry and micro miniaturization requirements.

[0003] A common method for forming metal lines or plugs is known as "damascene". Generally, this process involves forming an opening in the dielectric interlayer, which separates the vertically spaced metallization layers. The opening is typically formed using conventional lithographic and etching techniques. After an opening is formed, the opening is filled with copper or copper alloys to form a via. Excess metal material on the surface of the dielectric interlayer is then typically removed by chemical mechanical planarization (CMP).

[0004] Copper has replaced aluminum because of its lower resistivity and higher reliability, which was expected to be better because of its higher activation energy for diffusion. However, copper still suffers from electro migration (EM) and stress migration (SM) reliability issues as geometries continue to shrink, and current densities increase.

[0005] Figure 1 illustrates a cross sectional view of a conventional interconnection structure 1 formed using damascene process. Metal lines 2 and 4, which are typically formed of copper or copper alloys, are interconnected by via 10. Inter-metal-dielectric (IMD) 8 separates two layers that metal lines 2 and 4 locate. Etch stop layer (ESL) 5 is formed on lower layer copper line 2. Diffusion barrier layers 12 and 14 are formed to prevent copper from diffusing into surrounding materials. The interconnection structure 1 in Figure 1 suffers from electro migration and stress migration problems. Since the copper line 2 is in direct contact with a dielectric ESL 5, the character difference between copper 2 and dielectric ESL 5 causes higher electro migration and stress migration; therefore device reliability is degraded.

[0006] Figure 2 illustrates an improvement made to the conventional interconnection structure 1 by forming a metal cap layer 16 on the copper line 2. Cap layer 16 is typically formed of materials suffering less from electro migration. T his layer greatly improved the reliability of the interconnections structure 15 by removing the interface between copper line 2 and dielectric layer 5. The copper surface migration of structure 15 is reduced. It has been found that under stressed conditions, the mean time to failure (MTTF) of the interconnection structure 3 is ten times longer than that of the interconnection structure 1 due to the reduction of electro migration. With the cap layer 16 formed, the stress induced void formation is also significantly reduced.

[0007] However, the introduction of the cap layer 16 generates another problem. IMD 8 is etched in order to form an opening for via and then ESL 5 is etched. Metal cap layer 16 is typically etched through due to over etching when ESL 5 is etched. In conventional formation of the interconnect structure, the process is only controlled so that the over etching stops at a time after the ESL 5 has been etched out. Typically, over etching may stop in cap layer 16 or

copper 2. If over etching lands in cap layer 16, since metal cap 16 normally has a higher resistance than copper 2, the resistance of the remaining cap layer 16 contributes to the resistance of the interconnection. Higher resistance of the interconnection causes higher RC delay of the integrated circuits; if over etching stops in copper line 2, the contact resistance is much smaller than the contact resistance having a remaining cap layer 16. Therefore, contact resistance and RC delay varies from process to process and is harder to predict.

[0008] In order to reduce contact resistance and RC delay, and reduce process variation, a new method of forming interconnection structures is needed.

SUMMARY OF THE INVENTION

[0009] The preferred embodiment disclosed herein is a method of forming an integrated circuit interconnect structure having a metal cap on a conductive line.

[009a] In one aspect, there is provided an integrated circuit interconnection structure comprising:

a first conductor extending from a surface of a base material into the base material;

a conductive cap layer on the first conductor;

a first dielectric on the conductive cap layer and the base material;

a second dielectric on the first dielectric;

an opening in the first dielectric, second dielectric, and conductive cap layer wherein the opening extends into the first conductor and forms a recess; and wherein the recess has

a depth of greater than about 1nm; and

a second conductor over the second dielectric and filling the opening and the recess.

[0010] In accordance with one embodiment disclosed herein, a first conductive line is formed over a semiconductor substrate. A conductive cap layer can be formed on the first conductive line. An etch stop layer (ESL) can be formed on the conductive cap layer. An inter-metal-dielectric (IMD) can be formed on the ESL. A via opening and a trench can be formed in the ESL, IMD and conductive cap layer. A recess can be formed in the first conductive line. The recess can be formed by over etching when the first dielectric is etched, or by a separate process such as argon sputtering. A second conductive line can be formed filling the trench, via opening and recess.

[0011] With a conductive cap on the first conductive line, the reliability and performance of the interconnection structure may be significantly improved. The preferred embodiment disclosed herein eliminates the possibility that the second conductive line can be coupled to the first conductive line through the cap layer, which causes higher contact resistance and thus higher RC delay.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0013] Figure 1 illustrates a conventional interconnection structure with no metal cap formed;

[0014] Figure 2 illustrates a conventional interconnection structure with a metal cap formed; and

[0015] Figures 3 through 10 are cross-sectional views of intermediate stages in the making of a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0016] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0017] Figures 3 through 10 are cross-sectional views of intermediate stages in the making of a preferred embodiment of the present invention. A via connecting two conductive lines are formed. Figure 3 illustrates formation of a trench 26 in a base material 20. In the preferred embodiment, base material 20 is an IMD preferably comprising a material having a dielectric constant (K value) lower than about 3.3 and contains nitrogen, carbon, hydrogen, oxygen, fluorine and their combinations. In alternative embodiments, base material 20 can be a silicon substrate or other non-conductive material.

[0018] Figure 4 illustrates a diffusion barrier layer 30 and a conductive line 32 formed in trench 26. Barrier layer 30 is preferably formed of a material comprising titanium, titanium nitride, tantalum, tantalum nitride, or other alternatives. The material of the conductive line 32 is preferably a copper or copper alloys comprising at least about 10 atomic percent of copper. Through out the description, conductive line 32 may alternatively referred as copper 32 although it may comprise other conductive materials. In one embodiment, conductive line 32 comprises at least 50 atomic percent of aluminum. In yet other embodiments, conductive line 32 comprises silver or gold. Conductive line 32 preferably has a good conductivity with resistivity lower than about 4ohm-cm and is typically formed by depositing a thin layer of seed copper or copper alloy,

then plating to fill the trench 26. A chemical mechanical planarization (CMP) is performed to level the surface of copper 32.

[0019] Figure 5 illustrates a metal cap 33 formed on conductive line 32 and optionally on barrier layer 30. The metal cap 33 preferably comprises materials such as cobalt, nickel, tungsten, molybdenum, tantalum, boron, and phosphorus. These materials may exist in the form of CoP, CoB, CoWP, CoWB, NiWP, CoSnP, NiWB, CuSi, ZrN, NiMoP and their combinations. Metal cap 33 has a preferred thickness of about 2nm to 20nm. Since metal cap 33 has a better characteristic match with conductive line 32 than a dielectric, electro migration and stress migration are reduced and thus device reliability is improved. In the preferred embodiment, conductor line 32 is a copper or copper alloys so that metal cap 33 can be formed as a copper silicide. Growth of copper silicide 33 can be performed by a chemical vapor reaction (CVR) process that involves introducing a chemical vapor of SiH_4 gas into a chamber at a temperature from about 200°C to about 420°C to react with copper. In other embodiments, metal cap 33 can be formed by electroless plating. In yet other embodiments, metal cap 33 can be deposited using common techniques such as sputtering and CVD and then etched. Metal cap 33 preferably has a thickness of between about 2nm to about 20nm, more preferably about 10nm.

[0020] In the preferred embodiment, after the conductive line 32 and metal cap 33 are formed, a dual damascene process is preferably performed to form a via and a second copper line. In alternative embodiments, the via and second copper line can be formed by single damascene process. Figure 6 shows a via etching stop layer (ESL) 34 formed on cap layer 32 and base material 20. Via ESL 34 is preferably a dielectric material comprising carbon, silicon, nitrogen, and oxygen and having a k value of less than about 5. The thickness of the ESL 34 is preferably smaller than about 80nm. A via IMD layer 36 is formed on the via ESL layer 34 providing

insulation between copper line 32 and a second copper line that will be formed subsequently. The via IMD 36 preferably has a k value less than about 3.4 and comprises carbon-doped silicon oxide, fluorine-doped silicon oxide, organic low-k material and porous low-k material. It is preferably formed by a spin-on, a chemical vapor deposition (CVD) or other known methods. A trench IMD 40 is then formed, as also shown in Figure 6. The trench IMD 40 is preferably formed by similar methods and using similar materials as IMD 36. The materials and methods of forming via ESL 34, via IMD 36, and trench IMD 40 are known in the art.

[0021] Figure 7 illustrates formation of a via opening 44. A photo resist material (not shown) is formed and patterned over the trench IMD 40. An anisotropic etch, preferably using fluorine containing etching gases, cuts through the trench IMD 40, via IMD 36 and stops at the via ESL 34, therefore forming a via opening 44. The via ESL 34 protects the underlying first conductive line 32 from being etched. The length and width W of via opening 44 are preferably smaller than about 500nm.

[0022] Figure 8 illustrates the formation of a trench opening 46. An anisotropic etch cuts through the trench IMD 40 and thus forming the trench opening 46. Trench opening 46 will be used to form a second conductive line when filled.

[0023] In the preferred embodiment, exposed portion of via ESL 34 is etched, preferably by using etchant comprising CF_4, C_4F_8, or O_2. Figure 9 shows the structure after ESL 34 is etched. Because via ESL 34 is quite thin relative to the IMD layers 36 and 40, process control and end-point detection are much more closely controlled, thus limiting the likelihood of over-etching through the underlying first copper line 32. Etching continues into the metal cap 33 after ESL 34 is etched away. In one preferred embodiment, process is controlled so that the metal cap 33 is etched away, and its underlying copper 32 is also over etched to form a recess 48 in conductive

line 32. In other embodiments, after over etching has reached into metal cap 33 or conductive line 32, a sputtering is performed to sputter out the remaining metal cap 33 and into underlying conductive line 32 to form a recess 48. The sputtering typically uses inert species such as argon or helium. Preferably, recess 48 has a depth D of between about 1nm to about 100nm, more preferably about 10nm to about 100nm.

[0024] Figure 10 illustrates formation of a second conductive line 50 and via 52 in openings 44 and 46 and recess 48. The via opening 44 and trench opening 46 are filled with conductive materials. Preferably, conductor line 50 and via 52 are formed of copper or copper alloys. Similar to the first conductive line, the material of the via 52 and second conductive line 50 preferably comprises at least about 10 atomic percent of copper. In alternative embodiments, conductive line 50 may comprises at least 50 atomic percent of aluminum, silver and gold. The resistivity of via 52 and conductive line 50 is preferably lower than about 4ohm-cm. A CMP is performed to level the surface. A barrier layer (not shown) may be formed before the second conductive line 50 is formed. The barrier layer is preferably formed of a material comprising titanium, titanium nitride, tantalum, tantalum nitride, and other layers as well. The thickness of the barrier layer is preferably between about 2nm to about 40nm.

[0025] In another preferred embodiment, after the structure in Figure 8 is formed, a barrier layer (not shown) is formed on the sidewalls of via opening 44, trench opening 46 and exposed portion of via ESL 34. An anisotropic etching or sputtering is then performed to remove materials at the bottom of the via opening 44, including barrier layer, via ESL 34, and metal cap 33. Recess 48 is then formed. The process in this embodiment removes the barrier layer formed between via 52 and conductive line 32. Therefore better contact is formed through a direct contact between copper and copper.

[0026] In the preferred embodiment, the recess 48 formed in the first conductive line 32 ensures that there is substantially no material of cap layer 48 left in exposed portion of via opening 44. The contact resistance is greatly reduced and RC delay reduced. The contact resistance is more predictable and process variation is reduced.

[0027] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. An integrated circuit interconnection structure comprising:

a first conductor extending from a surface of a base material into the base material;

a conductive cap layer on the first conductor;

a first dielectric on the conductive cap layer and the base material;

a second dielectric on the first dielectric;

an opening in the first dielectric, second dielectric, and conductive cap layer wherein the opening extends into the first conductor and forms a recess; and wherein the recess has

a depth of greater than about 1 nm; and

a second conductor over the second dielectric and filling the opening and the recess.

2. The interconnection structure of claim 1 wherein the first and second conductors comprise a material selected from the group consisting essentially of an alloy containing more than about 10 atomic percent of copper, an alloy containing more than about 50 atomic percent of aluminum, silver, gold, and combinations thereof.

3. The interconnection structure of claim 2 wherein the first and second conductors have a resistivity of lower than about 4ohm-cm.

4. The interconnection structure of claim 1 wherein the conductive cap layer comprises a material selected from the group consisting essentially of cobalt, nickel, tungsten, molybdenum, tantalum, boron, phosphorous, and combinations thereof.

5. The interconnection structure of claim 1 wherein the conductive cap layer comprises a material selected from the group consisting essentially of CoP,CoB, CoWP, CoWB, NiWP, CoSnP, NiWB, CuSi, ZrN, NiMoP and combinations thereof.

6. The interconnection structure of claim 1 wherein the conductive cap layer has a thickness of between about 2nm and about 20nm.

7. The interconnection structure of claim 1 wherein the second dielectric comprises a material selected from the group consisting essentially of carbon-doped silicon oxide, fluorine-doped silicon oxide, organic low-k material, porous low-k material and combinations thereof.

8. The interconnection structure of claim 1 wherein the recess has a depth of between about 1nm and about 10nm.

9. The interconnection structure of claim 1 wherein the recess has a depth of between about 10nm and about 100nm.

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ABSTRACT OF THE DISCLOSURE

A method of forming an integrated circuit interconnect structure is presented. A first conductive line is formed over a semiconductor substrate. A conductive cap layer is formed on the first conductive line to improve device reliability. An etch stop layer (ESL) is formed on the conductive cap layer. An inter-level dielectric (IMD) is formed on the ESL. A via opening and a trench are formed in the ESL, IMD, and conductive cap layer. A recess is formed in the first conductive line. The recess can be formed by over etching when the first dielectric is etched, or by a separate process such as argon sputtering. A second conductive line is formed filling the trench, opening and recess.

(FIG. 3)