

Oscillator Circuit

Field of the Invention

This invention relates to a an oscillator circuit, especially to an
5 oscillator circuit for use with a Phase Locked Loop (PLL) system.

Background of the Invention

As is well known, oscillator circuits are used in PLL systems to
provide a signal having a controllable frequency, which is then
compared with a reference frequency in the PLL system and passed
10 through divider stages so as to output a defined frequency output
signal having a predetermined relationship to the reference
frequency.

PLL systems often require a very wide range of output
frequencies, for example in television tuning circuits and monitor
15 scanning timebase circuits. However, known oscillator circuits do
not provide a high degree of accurate control of frequency over such
wide frequency ranges. Consequently, oscillator circuits used in
such applications are relatively complicated, in order to try to
provide accurate frequency control over a wide range, and therefore
20 tend to be noisy, that is there is a high level of spurious noise in the
output signal.

In one known form of a balanced oscillator circuit a current
control circuit controls the current at both plates of a capacitor in
order to control its charge and discharge rates. The voltages on the
25 two capacitor plates are compared by a comparator, whose output is
used to control the current control circuit. The oscillating output is
taken, via an output buffer amplifier, from the output of the
comparator. A control signal is input to the current control circuit to
control the frequency of the oscillating output.

30 Brief Summary of the Invention

The present invention therefore seeks to provide an oscillator
circuit which overcomes, or at least reduces, the above-mentioned
problems of the prior art.

Accordingly, the invention provides an oscillator circuit
35 comprising a capacitor having first and second plates, a current
control circuit having a control input, a balanced input having first
and second sides, a first control output coupled to the first plate of

the capacitor and a second control output coupled to the second plate of the capacitor, a comparator having a first input coupled to the first control output of the current control circuit, a second input coupled to the second control output of the current control circuit
5 and a balanced output having a first side coupled to the first side of the balanced input of the current control circuit and a second side coupled to the second side of the balanced input of the current control circuit, a first diode coupled between the first control output of the current control circuit and a voltage supply source, a second
10 diode coupled between the second control output of the current control circuit and the voltage supply source, a first switching device having a control input coupled to receive the first side of the balanced output of the comparator for selectively switching the first diode into a current path with the first control output of the current
15 control circuit for absorbing current from the first control output of the current control circuit in order to provide a voltage level on the first input of the comparator, a second switching device having a control input coupled to receive the second side of the balanced output of the comparator for selectively switching the second diode
20 into a current path with the second control output of the current control circuit for absorbing current from the second control output of the current control circuit in order to provide a voltage level on the second input of the comparator, and an output terminal coupled to one or both sides of the balanced output of the comparator for
25 providing an oscillating output signal.

In a preferred embodiment, the current control circuit comprises a first constant current pull-down circuit coupled to the first side of the balanced input of the current control circuit for providing a load for the first side of the balanced output of the
30 comparator, and a second constant current pull-down circuit coupled to the second side of the balanced input of the current control circuit for providing a load for the second side of the balanced output of the comparator.

Preferably, the current control circuit comprises a first
35 variable current generator having an input coupled to the control input of the current control circuit and an output coupled to the first control output of the current control circuit, and a second variable

current generator having an input coupled to the control input of the current control circuit and an output coupled to the second control output of the current control circuit.

5 The current control circuit preferably comprises a third constant current pull-down circuit coupled to a current bias input of the comparator. Conveniently, any one or more of the first, second or third constant current pull-down circuits can comprise a current generator.

10 Preferably, the capacitor comprises a pair of capacitors of substantially equal value connected in parallel in anti-phase. The capacitors are preferably formed as a monolithic integrated structure, each of the capacitors comprising a substrate of a first conductivity type having an epitaxial region of a second conductivity type diffused into the substrate, a capacitive region of the first
15 conductivity type diffused into the epitaxial region, and a conductive or semiconductive region on top of the capacitive region, wherein the conductive or semiconductive region is coupled to the capacitive region of the other of the capacitors. The epitaxial region of both of the capacitors is preferably electrically connected to the voltage
20 supply source.

In one embodiment, the oscillator circuit further comprises a differentiating circuit having an input for receiving a synchronisation signal and an output for providing a differentiated synchronisation signal and a phase splitting circuit having an input
25 coupled to the output of the differentiating circuit for receiving the differentiated synchronisation signal and first and second outputs coupled respectively to the first and second plates of the capacitor for forcing the voltage levels on the first and second plates of the capacitor to predetermined opposite levels.

30 The circuit is preferably manufactured utilising active elements which are formed of any one or more of Metal Oxide Semiconductor (MOS) transistors, Field Effect Transistors (FET), Bipolar Junction Transistors (BJT), P-channel transistors, N-channel transistors, PNP transistors or NPN transistors.

35 Brief Description of the Drawings

One embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows an example of an oscillator circuit according to the prior art;

FIG. 2 shows an example of an oscillator circuit according to the invention;

FIG. 3 shows a complete oscillator system incorporating the oscillator circuit of FIG. 2;

FIG. 4 shows the waveforms appearing at the different points of the oscillator circuit of FIG. 2; and

FIG. 5 is a schematic cross-sectional view through a semiconductor structure of a pair of capacitors used in the oscillator circuit of FIG. 2.

Detailed Description of the Drawings

Thus, in one known form of a balanced oscillator circuit, as shown in FIG. 1, the circuit uses a capacitor which is charged and discharged by means of a switched current. Since the frequency range should be large, and the capacitor will have a fixed value, the current will need to be varied over a large range because it is important that the oscillator be active over a large range.

The capacitor 87 is connected between the emitters of two transistors 78 and 79. The collectors of the transistors 78 and 79 are connected, respectively, to the bases of a long tailed transistor pair 70 and 71. The collectors of transistors 70 and 71 are connected via load resistors 72 and 73, respectively, to the supply rail V_{CC} and to the bases of transistors 88 and 91 respectively. The emitter of transistor 88 is connected to transistor 94 in a darlington arrangement with the collectors of both transistors 88 and 94 being connected to V_{CC} . The emitter of transistor 94 is connected to the base of transistor 78. Similarly the emitter of transistor 91 is connected to the base of transistor 97 in a darlington arrangement and the collectors of transistors 91 and 97 are connected to the supply rail V_{CC} . The emitter of transistor 91 is connected to the base of transistor 79.

Transistors 95, 89, 74, 92 and 98 form current generators with their emitters connected via resistors 96, 90, 75, 93 and 99,

respectively, to ground reference potential V_{GND} and their bases all connected to a first reference voltage V_{BIAS1} . Similarly transistors 80, 82 and 68 form current generators with their emitters connected via resistors 81, 83 and 69 respectively to ground reference potential V_{GND} and their bases connected to a second reference voltage V_{BIAS2} .

The output of the collector of current generator transistor 68 is connected to a current generator formed by transistors 67, 76 and 77, whose sources are connected to the positive supply rail V_{CC} . The input of the current generator is at the gate and drain connections of transistor 67 and the gates of transistors 76 and 77. The outputs of the current generator, at the drains of transistors 76 and 77, are connected to the bases of transistors 70 and 71, respectively. In operation the current at the collector of transistor 78 is nominally balanced by the current at the drain of transistor 76. Similarly, the current at the collector of transistor 79 is nominally balanced by the current at the drain of transistor 77. However, because the currents at the collectors of transistors 78 and 79 do not precisely balance the currents at the drains of transistors 76 and 77, respectively, resistors 84, 85 and 86 are provided. Resistor 85 is coupled between the drains of transistors 76 and 77, resistor 84 is coupled between the drain of transistor 77 and the emitter of transistor 88 and resistor 86 is coupled between the drain of transistor 76 and the emitter of transistor 91.

In operation, the oscillator's frequency is controlled by varying the voltage of the second reference voltage V_{BIAS2} . However because of the currents in resistors 84, 85 and 86 the control range over which the oscillator operates is limited.

Referring now to the embodiment of the invention shown in FIG. 2, it will be apparent that the oscillator circuit 101 overcomes much of the limitations of the prior art circuit of FIG. 1 by avoiding the problem of having currents which are required to balance.

The oscillator circuit 101 includes a current control circuit 1 having a bias voltage input for receiving a first reference voltage V_{BIAS1} and a control input for receiving a second reference voltage V_{BIAS2} , as will be explained more fully below. The current control circuit 1 includes first and second constant current pull-down

circuits 2 and 3 having first and second inputs and a third constant current pull-down circuit 4 having an input. The current control circuit 1 also includes first and second variable current generators 5 and 6 providing, respectively, first and second outputs of the
5 current control circuit 1.

The first and second outputs of the current control circuit 1 are coupled to either side of the capacitor 21. As shown in FIG. 2, capacitor 21 is also connected between emitters of transistors 19 and 20, whose collectors are respectively coupled to emitters of
10 diode-coupled transistors 17 and 18, respectively. The collectors of transistors 19 and 20 are also connected to the bases of transistors 11 and 12, respectively, which form a long-tailed pair. The emitters of the diode-coupled transistors 17 and 18 are also connected to the bases of transistors 11 and 12, respectively. The collectors and
15 bases of transistors 17 and 18 are all connected to the supply rail V_{CC} .

The collector of transistor 11 is also connected to the base of transistor 27 and, via a load resistor 13, to the supply rail V_{CC} . The emitter of transistor 27 is connected to the base of transistor 19.
20 Similarly the collector of transistor 12 is connected to the base of transistor 34 and, via the load resistor 14, to the supply rail V_{CC} . The emitter of transistor 34 is connected to the base of transistor 20. The transistors 11 and 12 and resistors 13 and 14 thus form a comparator 7 having first and second inputs, at the bases of
25 transistors 11 and 12, respectively, and first and second sides of a balanced output at the collectors of transistors 11 and 12, respectively. Transistors 19 and 27 form a first switching device 8 for switching the diode-connected transistor 17 into and out of connection with the first control output of the current control circuit
30 1 and the first plate of the capacitor 21. Similarly, transistors 20 and 34 form a second switching device 9 for switching the diode-connected transistor 18 into and out of connection with the second control output of the current control circuit 1 and the second plate of the capacitor 21. The outputs V_1 and V_2 of the oscillator circuit 101
35 are taken at the emitters of transistors 27 and 34.

Transistors 28, 35 and 15 have their emitters connected to ground reference potential V_{GND} via resistors 29, 36 and 16,

respectively to form the first, second and third constant current pull-down circuits 2, 3 and 4 to provide currents at the emitters of transistors 27, 34 and at the current bias input of the comparator 7 at the emitters of transistors 11 and 12, respectively. Similarly to the circuit shown in FIG. 1, the first reference voltage V_{BIAS1} controls the base voltage of these current generators.

Transistors 23 and 25 form the first and second variable current generators 5 and 6, respectively, with their emitters connected to ground reference potential V_{GND} via resistors 24 and 26, respectively, and their bases connected to the second reference voltage V_{BIAS2} . The second reference voltage V_{BIAS2} is used to control the charging current in the capacitor 21 and therefore to control the frequency. It can thus be seen that the circuit can improve the range of controllable frequency by avoiding the use of resistors (84, 85 and 86 in FIG. 1) and using instead the properties of diode-coupled transistors 17 and 18 as loads.

Referring now to FIG. 3, there is shown a complete oscillator system incorporating the oscillator circuit 101 of FIG. 2. Transistors 31 and 32 and resistors 30 and 33 are used to form a first voltage reference circuit to provide the first reference voltage V_{BIAS1} . The collector of transistor 32 is connected to the base of transistor 31 and to the supply rail V_{CC} via resistor 30. The emitter of transistor 32 is connected to ground reference potential V_{GND} via resistor 33. The output of the first voltage reference circuit at the junction of the base of transistor 32 and emitter of 31 provide the first reference voltage V_{BIAS1} .

The second reference voltage V_{BIAS2} is provided by a second reference voltage circuit formed by transistors 56 and 57 and resistor 58. The collector of transistor 57 is connected to the base of transistor 56 and to a controlling voltage V_{CONTR} . The emitter of transistor 57 is connected to ground reference potential V_{GND} via resistor 58 and the collector of transistor 56 is connected to the supply rail V_{CC} . The output of the second voltage reference circuit at the junction of the base of transistor 57 and emitter of 31 provide the second reference voltage V_{BIAS2} .

The outputs V_1 and V_2 of the oscillator circuit 101 at the emitters of transistors 27 and 34 are connected to the inputs of an

output buffer circuit 102. The output buffer circuit 102 is formed by transistors 37 and 38 and resistor 39 coupled in series between the supply rail V_{CC} and the ground reference potential V_{GND} and transistors 40 and 41 and resistor 42 also coupled in series between
5 the supply rail V_{CC} and the ground reference potential V_{GND} . The bases of transistors 38 and 41 are coupled to the first reference voltage V_{BIAS1} . The bases of transistors 40 and 37 form the inputs of the output buffer circuit 102 and are coupled to receive the outputs V_1 and V_2 of the oscillator circuit 101, respectively. Outputs
10 V_{OUT1} and V_{OUT2} of the output buffer circuit 102 are taken at the emitters of transistors 40 and 37, respectively.

In order to phase lock the oscillator to the intended synchronization pulse, a synchronisation input buffer is also included. This is in addition to the use of the normal Phase Locked
15 loop arrangement. The synchronisation input buffer includes a synchronisation differentiating circuit 100 and a phase splitting circuit 103. In the synchronisation differentiating circuit 100, a synchronization input signal V_{SYNC} is applied to the base of a transistor 45, whose emitter is at reference potential V_{GND} . A
20 resistor 43, is connected between the base of the transistor 45 and the supply rail V_{CC} in case the synchronization input signal pulse is a.c. coupled. The collector of transistor 45 is connected to the supply rail V_{CC} via resistor 44 and to the base of transistor 49 via a capacitor 46. The base of transistor 49 is further connected to the
25 supply rail V_{CC} via resistor 48. The arrangement of capacitor 46 and resistor 47 forms a differentiating network such that only the negative going signal at the collector of transistor 45 is effective (or positive going edge of the input signal V_{SYNC}). The collector of transistor 49 is connected via resistor 48 to the supply rail V_{CC} .

30 The collector of transistor 49 is further connected to the phase splitting circuit 103 formed of two emitter follower transistors 50 and 55 with their collectors connected to supply rail V_{CC} . The emitter of transistor 50 is connected to the base of transistor 54 via resistor 51. A further resistor 52 is connected between the base and
35 emitter of transistor 54 whose emitter is connected to ground reference potential V_{GND} . The collector of transistor 54 is connected via a diode-connected transistor 53 to one side of a capacitor 22,

which is coupled in parallel with the capacitor 21. The emitter of transistor 55 is connected to the other side of capacitors 22 and 21. The diode connected transistor 53 is connected with it's collector and emitter coupled to the collector of 54 and it's base to one side of capacitor 21.

Thus, when a pulsed input signal V_{SYNC} is provided at the base of transistor 45, a positive pulse is produced at the collector of transistor 49, which is then used via the emitter follower transistor 55 and the diode-connected transistor 53 to initialize the state of the voltage on the capacitors 21 and 22 into a defined state. The capacitor 46 and resistor 47, which are used to define the duration of the differentiated pulse, are chosen such that the initialization pulse is normally shorter than half the period of oscillation of the oscillator system at the fastest rate.

Referring now to FIG. 4, the typical waveforms are shown. The waveform 105 is at the collector of transistor 11, while the waveform 106 is that at the base of transistor 11. The waveform 107 is that at the emitter of transistor 19, which is on one side of the capacitor 21. As the circuit is a balanced symmetrical circuit similar waveforms can be seen at the collector of transistor 12, the base of transistor 12 and at the emitter of transistor 20, the other side of the capacitor 21. These waveforms will, of course be shifted in phase by half a period.

The principle of operation is as follows, assuming that the voltage on the emitter of transistor 19 is positive with respect to the voltage on the emitter of transistor 20. Transistor 20 will be conducting and, since transistor 19 is not in conduction, the voltage at the base of transistor 12 will be negative with respect to the voltage at the base of transistor 11. Transistor 11, therefore, is conducting and will be passing the tail current, at the collector of transistor 15, to the load resistor 13. Now the current at the collector of transistor 23 will charge the capacitor 21 such that the voltage at the emitter of transistor 19 comes in a negative direction, the sloping part of the waveform in waveform 107.

Eventually the voltage at the emitter of transistor 19 will be sufficiently negative to cause transistor 19 to start conducting. Once this happens, the voltage at the base of transistor 11 will also go

negative such that the conduction in the long tailed pair of transistors is switched from transistor 11 to transistor 12. Then, as the voltage at the load resistor 14 goes negative, this will cause transistor 20 to become non conducting, as the voltage change is coupled through the emitter follower 34, and the emitter of transistor 19 will go positive due to the voltage at the load resistor 13 going positive and being coupled through the emitter follower 27. Thus the process begins again but this time with the current generator transistor 25 causing the voltage at the emitter of transistor 20 to become negative on a slope similar to that shown in waveform 107.

As mentioned above, the oscillator circuit can include a pair of capacitors 21 and 22 of substantially equal value connected in parallel in anti-phase. As shown in FIG. 5, the capacitors are formed as a monolithic integrated structure 108, with both of the capacitors being formed in a P-type substrate 109 having an N-type epitaxial region 110 diffused therein. Each of the capacitors includes an N-type capacitive region 111 diffused into the epitaxial region 110 and a conductive metal layer 112 separated from the top of the capacitive region 111 by a layer of oxide 114. The conductive layer 112 of each of the capacitors is electrically connected, via connections 113 to the capacitive region 111 of the other of the capacitors. The epitaxial region 110 of both of the capacitors is electrically connected to the voltage supply source V_{CC} . The conductive layer 112 could, if desired, be replaced by an N-type region formed in the capacitive region 111.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

Claims

1. An oscillator circuit comprising:
a capacitor having first and second plates;
5 a current control circuit having a control input, a balanced input having first and second sides, a first control output coupled to the first plate of the capacitor and a second control output coupled to the second plate of the capacitor;
a comparator having a first input coupled to the first control
10 output of the current control circuit, a second input coupled to the second control output of the current control circuit and a balanced output having a first side coupled to the first side of the balanced input of the current control circuit and a second side coupled to the second side of the balanced input of the current control circuit;
15 a first diode coupled between the first control output of the current control circuit and a voltage supply source;
a second diode coupled between the second control output of the current control circuit and the voltage supply source;
a first switching device having a control input coupled to
20 receive the first side of the balanced output of the comparator for selectively switching the first diode into a current path with the first control output of the current control circuit for absorbing current from the first control output of the current control circuit in order to provide a voltage level on the first input of the comparator;
25 a second switching device having a control input coupled to receive the second side of the balanced output of the comparator for selectively switching the second diode into a current path with the second control output of the current control circuit for absorbing current from the second control output of the current control circuit
30 in order to provide a voltage level on the second input of the comparator; and
an output terminal coupled to one or both sides of the balanced output of the comparator for providing an oscillating
35 output signal.
2. An oscillator circuit according to claim 1, wherein the current control circuit comprises:



a first constant current pull-down circuit coupled to the first side of the balanced input of the current control circuit for providing a load for the first side of the balanced output of the comparator; and

5 a second constant current pull-down circuit coupled to the second side of the balanced input of the current control circuit for providing a load for the second side of the balanced output of the comparator.

10 3. An oscillator circuit according to either claim 1 or claim 2, wherein the current control circuit comprises:

a first variable current generator having an input coupled to the control input of the current control circuit and an output coupled to the first control output of the current control circuit; and

15 a second variable current generator having an input coupled to the control input of the current control circuit and an output coupled to the second control output of the current control circuit.

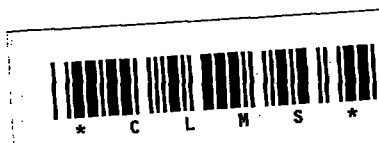
20 4. An oscillator circuit according to any one of claims 1, 2 or 3, wherein the current control circuit comprises a third constant current pull-down circuit coupled to a current bias input of the comparator.

25 5. An oscillator circuit according to claim 2, wherein the first constant current pull-down circuit comprises a current generator.

6. An oscillator circuit according to claim 2, wherein the second constant current pull-down circuit comprises a current generator.

30 7. An oscillator circuit according to claim 4, wherein the third constant current pull-down circuit comprises a current generator.

35 8. An oscillator circuit according to any preceding claim, wherein the capacitor comprises a pair of capacitors of substantially equal value connected in parallel in anti-phase.



9. An oscillator circuit according to claim 8, wherein the capacitors are formed as a monolithic integrated structure, each of the capacitors comprising a substrate of a first conductivity type having an epitaxial region of a second conductivity type diffused into the substrate, a capacitive region of the first conductivity type diffused into the epitaxial region, and a conductive or semiconductive region on top of the capacitive region, wherein the conductive or semiconductive region of each of the capacitors is electrically connected to the capacitive region of the other of the capacitors.
10. An oscillator circuit according to claim 9, wherein the epitaxial region of both of the capacitors is electrically connected to the voltage supply source.
11. An oscillator circuit according to any preceding claim, further comprising:
a differentiating circuit having an input for receiving a synchronisation signal and an output for providing a differentiated synchronisation signal; and
a phase splitting circuit having an input coupled to the output of the differentiating circuit for receiving the differentiated synchronisation signal and first and second outputs coupled respectively to the first and second plates of the capacitor for forcing the voltage levels on the first and second plates of the capacitor to predetermined opposite levels.
12. An oscillator circuit according to any preceding claim, wherein the circuit is manufactured utilising active elements which are formed of any one or more of Metal Oxide Semiconductor (MOS) transistors, Field Effect Transistors (FET), Bipolar Junction Transistors (BJT), P-channel transistors, N-channel transistors, PNP transistors or NPN transistors.
13. An oscillator circuit substantially as hereinbefore described with reference to FIGS. 2, 3 and 4 of the drawings.

