(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 March 2003 (06.03.2003)

PCT

(10) International Publication Number
WO 03/019399 A1

(51) International Patent Classification[7]: G06F 13/40, 13/42

(21) International Application Number: PCT/US02/27430

(22) International Filing Date: 27 August 2002 (27.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/315,144 27 August 2001 (27.08.2001) US
Not furnished 5 August 2002 (05.08.2002) US

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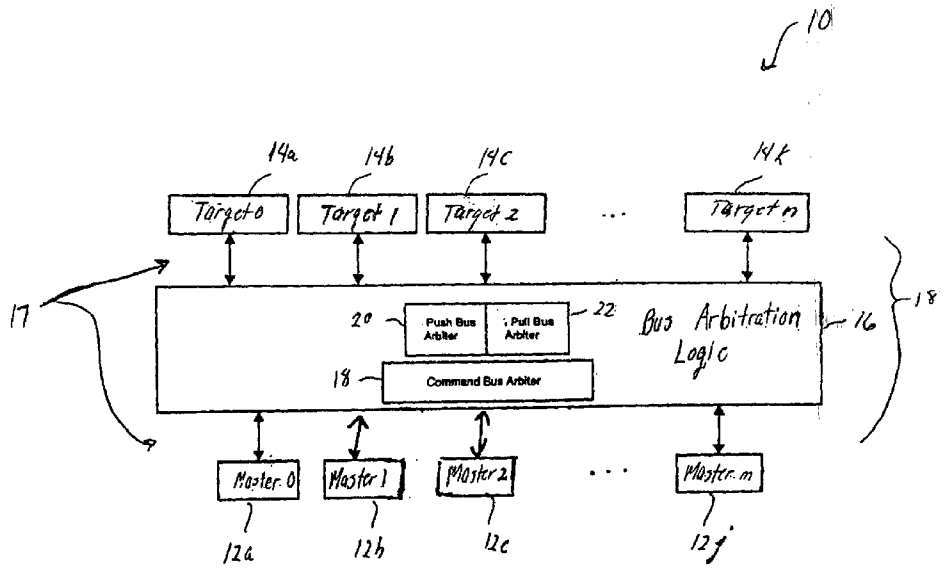
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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: A MULTIPROCESSOR INFRASTRUCTURE FOR PROVIDING FLEXIBLE BANDWIDTH ALLOCATION VIA MULTIPLE INSTANTIATIONS OF SEPARATE DATA BUSES, CONTROL BUSES AND SUPPORT MECHANISMS



(57) Abstract: A bus mechanism to control information exchanges between bus masters and bus targets over a bus structure that includes separate command, push and pull data buses. Commands are generated by bus masters and are interpreted by bus targets on a per-target basis. Each bus target controls the servicing of a command intended for such target by controlling the transfer of push data over the push bus to a bus master specified in the command as a destination, for a push operation type, and by controlling the transfer of pull data over the pull bus to the target from a bus master specified in the command as a destination, for a pull operation type. Arbitration logic associated with each bus is used to control the flow of the information exchanges on that bus.

WO 03/019399 A1

Published:
— *with international search report*

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