

SUSCEPTOR, DEVICE AND METHOD FOR EPITAXIAL GROWTH OF SILICON WAFER, AND EPITAXIAL SILICON WAFER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims a priority to the Chinese patent application No. 202410508018.6 filed in China on April 25, 2024, a disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of semiconductor manufacturing technology, and in particular, to a susceptor, a device and a method for epitaxial growth of a silicon wafer, and an epitaxial silicon wafer.

BACKGROUND

[0003] An epitaxial silicon wafers are fabricated by growing a single-crystal thin film on a polished single-crystal wafer. Compared to a polished wafer, the epitaxial silicon wafer exhibits the characteristics of fewer surface defects, superior crystallinity, and controllable resistivity, making it widely used in the manufacturing of a highly integrated Integrated Circuit (IC) component and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) processes. Typically, epitaxial growth on a wafer is performed using chemical vapor deposition. The wafer is first transferred to a susceptor in a reactor chamber. The chamber is then heated to a predetermined temperature. A clean gas, such as hydrogen, is then introduced to remove a native oxide layer from a wafer surface. Afterward, a silicon source gas is then introduced to grow an epitaxial layer on the front of the wafer continuously and uniformly.

[0004] The preparation of the epitaxial layer of the wafer is primarily divided into two stages. In a first stage, the reactor chamber is self-cleaned, with hydrogen (H_2) and an etching gas (HCl) introduced. In a second stage, epitaxial layer growth occurs, with hydrogen (H_2), a silicon source gas ($SiHCl_3/H_2$), and a dopant gas (B_2H_6/H_2) introduced. In the first stage, hydrogen serves as a primary carrier gas to transport the etching gas (HCl) to react with byproducts deposited in the reactor chamber, thereby cleaning the chamber. In the second stage, hydrogen reacts with the native oxide layer on the wafer surface to produce a clean epitaxial substrate. During a deposition phase, hydrogen serves as the primary carrier gas to transport the deposition gas and dopant gas

to grow an epitaxial layer with controllable resistivity on the wafer surface.

[0005] With the continuous development of semiconductor manufacturing technology, a flatness requirement for the epitaxial silicon wafer is becoming increasingly stringent. Poor flatness in the epitaxial silicon wafer may lead to defocus and even affect a Chemical Mechanical Polishing (CMP) process, thereby adversely impacting product yield. When the local flatness of an epitaxial silicon wafer is inadequate, it may result in over-polishing or insufficient-polishing. And the over-polishing may cause early breakdown of devices, while the insufficient-polishing may cause an error in devices contact.

SUMMARY

[0006] To solve the above technical problems, the present disclosure provides a susceptor, a device and a method for epitaxial growth of a silicon wafer, and an epitaxial silicon wafer, which can improve the flatness of the epitaxial silicon wafer.

[0007] To achieve the above objectives, the technical solutions adopted in the embodiments of the present disclosure are as follows:

- a susceptor for epitaxial growth of a silicon wafer, including:

- a disc-shaped supporting part configured to support the silicon wafer;

- an annular periphery extending radially outward from the disc-shaped supporting part, wherein the annular periphery is provided with a plurality of groove regions that is spaced apart from each other and uniformly distributed along a circumferential direction of the annular periphery, each of the groove regions is annular sector-shaped and provided with a plurality of pits arranged in an array.

[0008] In some embodiments, a central angle corresponding to a sector in which the groove region is located is in a range of 40° to 60°.

[0009] In some embodiments, four groove regions are uniformly distributed along the circumferential direction of the annular periphery.

[0010] In some embodiments, a depth of the pit is in a range of 0.1 mm to 1 mm; and/or

- an area of the pit is in a range of 0.1 mm² to 0.4 mm².

[0011] The present disclosure further provides a device for epitaxial growth of a silicon wafer, including:

- a susceptor as described above;

- a reactor chamber configured to accommodate the susceptor, wherein the susceptor

divides the reactor chamber into an upper reactor chamber and a lower reactor chamber, and the silicon wafer is arranged in the upper reactor chamber;

a gas inlet configured to deliver silicon source gas into the upper reactor chamber to grow an epitaxial layer on the silicon wafer;

an exhaust outlet configured to discharge exhaust gas generated during epitaxial growth from the reactor chamber.

[0012] The present disclosure further provides a method for epitaxial growth of a silicon wafer, which is applied to the device described above and includes:

placing the silicon wafer on the susceptor to allow a <100> crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery;

delivering the silicon source gas into the upper reactor chamber via the gas inlet to grow the epitaxial layer on the silicon wafer;

wherein a flow rate of the silicon source gas flowing through the groove region is greater than a flow rate of the silicon source gas flowing through other area of the annular periphery, to allow a thickness uniformity of the epitaxial layer grown on the silicon wafer;

discharging the exhaust gas generated during epitaxial growth from the reactor chamber via the exhaust outlet.

[0013] In some embodiments, the placing the silicon wafer on the susceptor to allow a <100> crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery includes:

obtaining a crystal orientation corresponding to a V-notch of the silicon wafer;

when the V-notch is in the <110> crystal orientation of the silicon wafer, placing the silicon wafer on the susceptor to allow an angle between a central axis of the V-notch and the central axis of the groove region to be 45°.

[0014] In some embodiments, the placing the silicon wafer on the susceptor to allow a <100> crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery includes:

obtaining a crystal orientation corresponding to a V-notch of the silicon wafer;

when the V-notch is in the <100> crystal orientation of the silicon wafer, placing the silicon wafer on the susceptor to allow an angle between the central axis of the V-notch and the central axis of the groove region to be 0°.

[0015] The present disclosure further provides an epitaxial silicon wafer, which is manufactured by the above-mentioned method for the epitaxial growth of the silicon wafer,

wherein when the thickness of the epitaxial layer of the epitaxial silicon wafer is not greater than 6 μm , a maximum value of an Edge Site Front Quotient Range (ESFQR) of the epitaxial silicon wafer is not greater than 57.1 nm.

[0016] In some embodiments, when the thickness of the epitaxial layer of the epitaxial silicon wafer is in a range of 3 μm to 4 μm , a value of the ESFQR of the epitaxial silicon wafer is in a range of 23 nm to 33.9 nm; and when the thickness of the epitaxial layer of the epitaxial silicon wafer is in a range of 4 μm to 6 μm , a value of the ESFQR of the epitaxial silicon wafer is in a range of 37.4 nm to 57.1 nm.

[0017] The beneficial effects of the present disclosure are as follows.

[0018] In the embodiments of the present disclosure, a groove region is formed on the annular periphery, and a plurality of pits are provided in the groove region. During epitaxial growth, when the silicon source gas is introduced into the reactor chamber, the presence of these pits enables the flow rate of the silicon source gas flowing through the groove region to be greater than the flow rate of the silicon source gas flowing through other area of the annular periphery. Since the growth rates of different crystal orientations of the silicon wafer are different, during epitaxial growth, the silicon wafer can be rotated at different angles according to the crystal orientation corresponding to the V-notch of the silicon wafer, so that the crystal orientation of the silicon wafer matches the position of the groove region, and a crystal orientation with a slower growth rate of the epitaxial layer is aligned with the groove region, thereby increasing the growth rate of the epitaxial layer in the crystal orientation with the slower growth rate. In this way, the growth rates of the epitaxial layers in different crystal orientations of the silicon wafer can be compensated, thereby improving the flatness of the epitaxial silicon wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 shows a schematic diagram showing gas flow in an epitaxial reactor chamber;

[0020] FIGs. 2 and 3 show schematic diagrams of a crystal orientation of a silicon wafer;

[0021] FIG. 4 shows a schematic diagram of the edge flatness of an epitaxial silicon wafer prepared according to the prior art;

[0022] FIG. 5 shows a schematic diagram of a process for preparing an epitaxial silicon wafer according to the prior art;

[0023] FIG. 6 shows a schematic diagram of a susceptor used for epitaxial growth of a silicon wafer according to the prior art;

[0024] FIGs. 7 and 8 show schematic diagrams of a susceptor for epitaxial growth of a silicon wafer according to an embodiment of the present disclosure;

[0025] FIG. 9 shows a schematic diagram of a process for preparing an epitaxial silicon wafer according to an embodiment of the present disclosure;

[0026] FIG. 10 shows a schematic diagram of placing a silicon wafer with a V-notch in a $\langle 100 \rangle$ crystal orientation on a susceptor according to an embodiment of the present disclosure;

[0027] FIGs. 11 and 12 show schematic diagrams of placing a silicon wafer with a V-notch in a $\langle 110 \rangle$ crystal orientation on a susceptor according to an embodiment of the present disclosure;

[0028] FIG. 13 shows a schematic diagram of the edge flatness of an epitaxial silicon wafer prepared according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0029] To make the objectives, technical solutions, and advantages of the embodiments of the present disclosure more apparent, the technical solutions of the embodiments of the present disclosure will be clearly and completely described below in conjunction with the accompanying drawings of the embodiments of the present disclosure. Obviously, the described embodiments are part of the embodiments of the present disclosure, not all of the embodiments. Based on the described embodiments of the present disclosure, all other embodiments obtained by a person of ordinary skill in the art shall fall within the scope of protection of the present disclosure.

[0030] The flatness of an epitaxial silicon wafer is typically characterized by metrics such as an Edge Site Front Quotient Range (ESFQR), a Site Front Quotient Range (SFQR), and a Global Backside Ideal Range (GBIR). The ESFQR is used to evaluate the edge flatness of the epitaxial silicon wafer.

[0031] FIG. 1 shows a schematic diagram showing gas flow in an epitaxial reactor chamber, where arrows indicate the direction of gas flow. After a silicon wafer is transferred to a susceptor 2 in an epitaxial reactor chamber, the susceptor 2, carrying the silicon wafer, rotates at a constant speed. The chamber is then heated to a predetermined temperature. A clean gas (H_2) is then introduced through a preheating ring 1 and an edge of the susceptor 2 to remove a native oxide layer from a wafer surface. Afterward, the primary carrier gas transports the deposition gas and dopant gas through the preheating ring 1 and the edge of the susceptor 2 to grow an epitaxial layer with controllable resistivity on the wafer surface.

[0032] FIGs. 2 and 3 show schematic diagrams of a crystal orientation of a silicon wafer. As shown in FIG. 2, when the three o'clock direction of the silicon wafer corresponds to the $0^\circ/360^\circ$

radial direction and aligns with the $\langle 110 \rangle$ crystal orientation, then the radial directions rotated clockwise by 90° , 180° , and 270° relative to the $0^\circ/360^\circ$ radial direction also correspond to the $\langle 110 \rangle$ crystal orientation of the silicon wafer. In contrast, the radial directions rotated clockwise by 45° , 135° , 225° , and 315° relative to the $0^\circ/360^\circ$ radial direction correspond to the $\langle 100 \rangle$ crystal orientation of the silicon wafer. In other words, for this silicon wafer, the four $\langle 110 \rangle$ crystal orientations correspond to four radial directions distributed at 90° intervals along a circumferential direction of the silicon wafer, and the four $\langle 100 \rangle$ crystal orientations similarly correspond to four radial directions distributed at 90° intervals along a circumferential direction of the silicon wafer. Adjacent $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations are spaced 45° apart along the wafer's circumference. As shown in FIG. 3, a V-notch 4 is formed on the silicon wafer 3 for alignment purposes. The V-notch 4 may correspond to either the $\langle 100 \rangle$ crystal orientation of the silicon wafer or the $\langle 110 \rangle$ crystal orientation of the silicon wafer.

[0033] FIG. 4 shows a schematic diagram of the edge flatness of an epitaxial silicon wafer prepared according to the prior art. FIG. 4 shows the ESFQR results for a 300 mm diameter silicon wafer at a position 1 mm from the radial edge, using a conventional susceptor for epitaxial growth of silicon wafer. In FIG. 4, the horizontal axis represents the angular position along the radial direction of the silicon wafer, and the vertical axis represents the ESFQR value (in nanometers) at the corresponding angular position. As shown in FIG. 4, the radial directions at $0^\circ/360^\circ$, 90° , 180° , and 270° correspond to the $\langle 100 \rangle$ crystal orientation of the silicon wafer, while the radial directions at 45° , 135° , 225° , and 315° correspond to the $\langle 110 \rangle$ crystal orientation of the silicon wafer. It can be observed that the edge flatness is better at the $0^\circ/360^\circ$, 90° , 180° , and 270° radial directions, and poorer at the 45° , 135° , 225° , and 315° radial directions. The epitaxial silicon wafer exhibits significant variation in edge flatness quality between the $\langle 100 \rangle$ and $\langle 110 \rangle$ crystal orientations. This is because the physical properties of the monocrystalline silicon wafer differ with crystal orientation, leading to different growth rates of the epitaxial layers in different crystal orientations of silicon wafers. Specifically, the growth rate of the epitaxial layer in the $\langle 110 \rangle$ crystal orientation is greater than that in the $\langle 100 \rangle$ crystal orientation.

[0034] In order to solve the above problems, the present disclosure provides a susceptor, a device and a method for epitaxial growth of the silicon wafer, and an epitaxial silicon wafer, which can improve the flatness of the epitaxial silicon wafer.

[0035] The present disclosure provides a susceptor for epitaxial growth of a silicon wafer, including:

a disc-shaped supporting part configured to support the silicon wafer;

an annular periphery extending radially outward from the disc-shaped supporting part, wherein the annular periphery is provided with a plurality of groove regions that is spaced apart from each other and uniformly distributed along a circumferential direction of the annular periphery, each of the groove regions is annular sector-shaped and provided with a plurality of pits arranged in an array.

[0036] In this embodiment, a groove region is formed on the annular periphery, and a plurality of pits are provided in the groove region. During epitaxial growth, when the silicon source gas is introduced into the reactor chamber, the presence of these pits enables the flow rate of the silicon source gas flowing through the groove region to be greater than the flow rate of the silicon source gas flowing through other area of the annular periphery. Since the growth rates of different crystal orientations of the silicon wafer are different, during epitaxial growth, the silicon wafer can be rotated at different angles according to the crystal orientation corresponding to the V-notch of the silicon wafer, so that the crystal orientation of the silicon wafer matches the position of the groove region, and the crystal orientation with a slower growth rate of the epitaxial layer is aligned with the groove region, thereby increasing the growth rate of the epitaxial layer in this crystal orientation. In this way, the growth rates of the epitaxial layers in different crystal orientations of the silicon wafer can be compensated, thereby improving the flatness of the epitaxial silicon wafer.

[0037] FIG. 5 shows a schematic diagram of a process for preparing an epitaxial silicon wafer according to the prior art, and FIG. 6 shows a schematic diagram of a susceptor used for epitaxial growth of a silicon wafer according to the prior art. As shown in FIG. 6, a conventional susceptor 2 includes a disc-shaped supporting part 21 configured to support the silicon wafer and an annular peripheral 22 extending radially outward from the disc-shaped supporting part 21. As shown in FIG. 5, during the preparation of an epitaxial silicon wafer, a monocrystalline silicon ingot is first produced and then sectioned into segments. According to product requirements, a V-notch is machined along a specific crystal orientation on the segment. The segment subsequently is subjected to slicing, grinding, polishing, cleaning, and measurement to obtain a substrate silicon wafer. The substrate silicon wafer is then graded and sorted. When the substrate silicon wafer is determined to be acceptable (OK), it is sorted to a corresponding carrier to begin an epitaxial growth process. When the substrate silicon wafer is determined to be unacceptable (NG), it is either reworked or scrapped.

[0038] FIG. 7 and FIG. 8 show schematic diagrams of a susceptor for epitaxial growth of a silicon wafer according to an embodiment of the present disclosure. The susceptor 5 includes a disc-shaped supporting part 51 and an annular peripheral 52 extending radially outward from the disc-

shaped supporting part 51. As shown in FIG. 7, compared to the susceptor shown in FIG. 6, in the embodiments of the present disclosure, it adds a groove region 6 to the annular peripheral 52 of the susceptor 5. The annular peripheral 52 is provided with a plurality of groove regions 6 that is spaced apart from each other and uniformly distributed along a circumferential direction of the annular periphery 52. The groove region 6 is annular sector-shaped, i.e., the groove region 6 is axially symmetrical, with a central axis of the groove region 6 being aligned radially on the susceptor 5. Each of the groove regions 6 is annular sector-shaped and provided with a plurality of pits 61 arranged in an array, which are recessed downward relative to another area of the annular peripheral 52. During epitaxial growth, the arrangement of the pits 61 can increase the amount of gas flowing through the groove region 6 to the surface of the silicon wafer, thereby increasing the growth rate of the epitaxial layer in the regions of the silicon wafer corresponding to the groove region 6.

[0039] In this embodiment, during epitaxial growth, the $\langle 100 \rangle$ crystal orientation of the silicon wafer can be aligned with the groove region 6 of the susceptor, that is, the $\langle 100 \rangle$ crystal orientation of the silicon wafer is oriented along the central axis of the groove region 6. In this way, during epitaxial growth, the growth rate of the epitaxial layer in the region corresponding to the $\langle 100 \rangle$ crystal orientation of the silicon wafer can be increased, thereby reducing the difference in the growth rate of the epitaxial layer between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations of the silicon wafer, and further improving the edge flatness of the epitaxial silicon wafer in the $\langle 110 \rangle$ crystal orientation.

[0040] In the technical solution of this embodiment, it is not strictly required that the $\langle 100 \rangle$ crystal orientation of the silicon wafer is exactly aligned with the central axis of the groove region 6. It is sufficient as long as the angle between the $\langle 100 \rangle$ crystal orientation of the silicon wafer and the direction of the central axis of the groove region 6 is not greater than 20° . In other words, the angle between the $\langle 100 \rangle$ crystal orientation of the silicon wafer and the direction of the central axis of the groove region 6 may be 0° , 5° , 10° , 15° , or 20° . Furthermore, since the growth rate of the epitaxial layer is relatively high in the $\langle 110 \rangle$ crystal orientation of the silicon wafer, in order to reduce the difference in the growth rate of the epitaxial layer between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations of the silicon wafer, the groove region 6 is preferably not provided in the radial direction of the annular peripheral 52 corresponding to the $\langle 110 \rangle$ crystal orientation of the silicon wafer.

[0041] In some embodiments, as shown in FIG. 7, D1, D2, D3, or D4 represent the 45° directions of the susceptor, while the directions of the gas injection port, exhaust outlet, wafer load/unload

port, and auxiliary gas injection port of the epitaxial reactor chamber correspond to the 0° direction of the susceptor. Four groove regions 6 can be uniformly distributed along a circumferential direction of the annular periphery 52, corresponding respectively to the directions of the gas injection port, exhaust outlet, wafer load/unload port, and auxiliary gas injection port of the epitaxial reactor chamber. As shown in FIG. 2 and FIG. 3, a silicon wafer has four $\langle 100 \rangle$ crystal orientations. Thus, when a silicon wafer is placed on the susceptor 5 of this embodiment for epitaxial growth, each $\langle 100 \rangle$ crystal orientation of the silicon wafer can correspond to a groove region 6. This increases the growth rate of the epitaxial layer in each $\langle 100 \rangle$ crystal orientation and effectively improves the edge flatness of the epitaxial silicon wafer in the $\langle 110 \rangle$ crystal orientation.

[0042] In some embodiments, as shown in FIG. 8, a central angle “a” corresponding to a sector in which the groove region 6 is located may be in the range of 40° to 60° , for example, 40° , 45° , 50° , 55° , or 60° . In this way, after the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the central axis of the groove region 6 of the susceptor, the edge flatness in the $\langle 100 \rangle$ crystal orientation and its adjacent areas of the silicon wafer can be effectively improved.

[0043] In this embodiment, the pits 61 can be arranged along the radial direction of the susceptor 5, and the depth of the pits 61 can be in a range of 0.1 mm to 1 mm, such as 0.1 mm, 0.2 mm, 0.3 mm, 0.4 mm, 0.5 mm, 0.6 mm, 0.7 mm, 0.8 mm, 0.9 mm or 1 mm. When the depth of the pits 61 adopts the above-mentioned dimensions, the amount of silicon source gas flowing through the groove region 6 to reach the surface of the silicon wafer during epitaxial growth can be effectively increased.

[0044] The area of the pit 61 can be in a range of 0.1 mm^2 to 0.4 mm^2 , for example, 0.1 mm^2 , 0.2 mm^2 , 0.3 mm^2 or 0.4 mm^2 . When the area of the pit 61 adopts the above-mentioned dimensions, the amount of silicon source gas flowing through the groove region 6 to reach the surface of the silicon wafer during epitaxial growth can be effectively increased.

[0045] In this embodiment, the shape of the orthographic projection of the pit 61 onto a horizontal plane may be a regular shape such as a rectangle, a circle, a parallelogram, or it may be an irregular shape.

[0046] In some embodiments, the distribution density of the pits gradually decreases along the direction from the center of the groove region to the edge of the groove region. In this way, during the epitaxial growth, after the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the central axis of the groove region 6 of the susceptor, the reduction in growth rate of the silicon wafer from the $\langle 100 \rangle$ crystal orientation to the $\langle 110 \rangle$ crystal orientation can be gradually minimized. This results in a more balanced growth rate along the entire circumferential direction

of the silicon wafer, leading to a more thickness uniformity of the epitaxial layer grown on the silicon wafer. Consequently, an epitaxial silicon wafer with improved flatness can be obtained.

[0047] An embodiment of the present disclosure further provides a device for epitaxial growth of a silicon wafer, including:

- a susceptor as described above;

- a reactor chamber configured to accommodate the susceptor, wherein the susceptor divides the reactor chamber into an upper reactor chamber and a lower reactor chamber, and the silicon wafer is arranged in the upper reactor chamber;

- a gas inlet configured to deliver silicon source gas into the upper reactor chamber to grow an epitaxial layer on the silicon wafer;

- an exhaust outlet configured to discharge exhaust gas generated during epitaxial growth from the reactor chamber.

[0048] In addition, similar to the known devices for epitaxial growth of the silicon wafer, the device may also include: a susceptor support frame, an upper quartz bell jar and a lower quartz bell jar that together enclose a reactor chamber, multiple heating bulbs, mounting components, etc. Moreover, there is also a small gap between the radial edge of the susceptor and adjacent components, allowing the susceptor to rotate at a certain speed around its own central axis driven by the susceptor support frame. This will not be elaborated further herein.

[0049] In an embodiment of the present disclosure, it further provides a method for epitaxial growth of a silicon wafer, which is applied to the device described above and includes:

- placing the silicon wafer on the susceptor to allow a <100> crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery;

- delivering the silicon source gas into the upper reactor chamber via the gas inlet to grow the epitaxial layer on the silicon wafer;

- wherein a flow rate of the silicon source gas flowing through the groove region is greater than a flow rate of the silicon source gas flowing through other area of the annular periphery, to allow a thickness uniformity of the epitaxial layer grown on the silicon wafer;

- discharging the exhaust gas generated during epitaxial growth from the reactor chamber via the exhaust outlet.

[0050] In this embodiment, during epitaxial growth, the silicon wafer can be rotated at different angles according to the crystal orientation corresponding to the V-notch of the silicon wafer, so that the crystal orientation of the silicon wafer matches the position of the groove region, and the crystal orientation with a slower growth rate of the epitaxial layer is aligned with the groove region,

thereby increasing the growth rate of the epitaxial layer in this crystal orientation. In this way, the growth rates of the epitaxial layers in different crystal orientations of the silicon wafer can be compensated, thereby improving the flatness of the epitaxial silicon wafer.

[0051] FIG. 9 shows a schematic diagram of a process for preparing an epitaxial silicon wafer according to an embodiment of the present disclosure. During the preparation of an epitaxial silicon wafer, a monocrystalline silicon ingot is first produced and then sectioned into segments. According to product requirements, a V-notch is machined along a specific crystal orientation on the segment. The segment subsequently is subjected to slicing, grinding, polishing, cleaning, and measurement to obtain a substrate silicon wafer. The substrate silicon wafer is then graded and sorted. When the substrate silicon wafer is determined to be acceptable (OK), it is sorted to an appropriate carrier to begin an epitaxial growth process. When the substrate silicon wafer is determined to be unacceptable (NG), it is either reworked or scrapped.

[0052] As shown in FIG. 9, the method for preparing an epitaxial silicon wafer according to the embodiment of the present disclosure further includes the following steps.

[0053] Step 101: setting a sorting rule for a substrate silicon wafer according to the orientation of the V-notch.

[0054] The V-notch of a silicon wafer is used to determine the crystal orientation of the silicon wafer. Depending on different product requirements, some silicon wafers have V-notches aligned along the $\langle 110 \rangle$ crystal orientation, while others have V-notches aligned along the $\langle 100 \rangle$ crystal orientation. In this embodiment, it is necessary to obtain the crystal orientation corresponding to the V-notch of the silicon wafer.

[0055] Step 102: when sorting qualified substrate silicon wafers with different V-notches orientations into corresponding carriers, the wafers are rotated at different angles.

[0056] In the related art, when placing a silicon wafer on a susceptor, the V-notch of the silicon wafer is generally aligned with the 0° direction of the susceptor, i.e., the direction of the gas injection port, exhaust outlet, wafer load/unload port, or auxiliary gas injection port of the epitaxial reactor chamber.

[0057] Step 103: rotating the substrate silicon wafer with the V-notch in the $\langle 110 \rangle$ crystal orientation by 45° .

[0058] When the V-notch is oriented in the $\langle 110 \rangle$ crystal orientation of the silicon wafer, before entering the epitaxial reactor chamber, the substrate silicon wafer with the V-notch oriented in the $\langle 110 \rangle$ crystal orientation is rotated by 45° , so that after the silicon wafer is placed on the susceptor, the angle between the central axis of the V-notch and the central axis of the groove region is 45° .

In this way, the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the groove region 6 of the susceptor, i.e., the $\langle 100 \rangle$ crystal orientation of the silicon wafer is oriented along the direction of the central axis of the groove region 6. During epitaxial growth, this arrangement can increase the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer. Consequently, it reduces the difference in the growth rate of the epitaxial layer between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations of the silicon wafer, thereby improving the edge flatness of the epitaxial silicon wafer at the $\langle 110 \rangle$ crystal orientation.

[0059] Step 104: rotating the substrate silicon wafer with the V-notch in the $\langle 100 \rangle$ crystal orientation by 0° .

[0060] When the V-notch is oriented in the $\langle 100 \rangle$ crystal orientation of the silicon wafer, before entering the epitaxial reactor chamber, the substrate silicon wafer with the V-notch in the $\langle 100 \rangle$ crystal orientation is rotated by 0° (i.e., not rotated), so that after the silicon wafer is placed on the susceptor, the angle between the central axis of the V-notch and the central axis of the groove region is 0° . In this way, the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the groove region 6 of the susceptor, i.e., the $\langle 100 \rangle$ crystal orientation of the silicon wafer is oriented along the direction of the central axis of the groove region 6. During epitaxial growth, this arrangement can increase the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer. Consequently, it reduces the difference in the growth rate of the epitaxial layer between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations of the silicon wafer, thereby improving the edge flatness of the epitaxial silicon wafer at the $\langle 110 \rangle$ crystal orientation.

[0061] FIG. 10 shows a schematic diagram of placing a silicon wafer 3 with a V-notch in a $\langle 100 \rangle$ crystal orientation on a susceptor according to an embodiment of the present disclosure. As shown in FIG. 2, when the V-notch 4 of the silicon wafer is aligned with the $\langle 100 \rangle$ crystal orientation of the silicon wafer, the regions of the silicon wafer that are at intervals of 45° and 135° from the V-groove 4 correspond to the $\langle 110 \rangle$ crystal orientation of the silicon wafer, while the regions at intervals of 90° and 180° correspond to the $\langle 100 \rangle$ crystal orientation of the silicon wafer.

[0062] As shown in FIG. 7, a groove region 6 is present at the edge corresponding to the 0° orientation of the susceptor. Compared to the 45° orientation of the susceptor, the gas flow rate through this groove region 6 increases during epitaxial growth, which accelerates the growth rate of the epitaxial layer. Therefore, to ensure uniform growth rates across different regions of the silicon wafer during epitaxial growth, it is necessary to align the $\langle 100 \rangle$ crystal orientation of the silicon wafer with the 0° orientation of the susceptor (where the groove region resides), and to align the $\langle 110 \rangle$ crystal orientation of the silicon wafer with the 45° orientation of the susceptor.

This increases the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer during epitaxial growth, resulting in thickness uniformity of the epitaxial layer along both the $\langle 100 \rangle$ and $\langle 110 \rangle$ crystal orientations.

[0063] As shown in FIG. 10, since the orientation of the susceptor is fixed when the epitaxial reactor chamber is installed, the 0° direction of the groove region 6 on the edge of the susceptor corresponds to the direction of the gas injection port, exhaust outlet, wafer load/unload port, or auxiliary gas injection port of the epitaxial reactor chamber. The silicon wafer with the V-notch in the $\langle 100 \rangle$ crystal orientation is rotated by 0° , i.e., not rotated. This allows the $\langle 100 \rangle$ crystal orientation of the silicon wafer to align with the 0° orientation of the susceptor (the direction corresponding to the groove region of the susceptor, where the gas flow rate on the silicon wafer surface increases), and the $\langle 110 \rangle$ crystal orientation of the silicon wafer to align with the 45° orientation of the susceptor. This compensates for differences in growth rate of the epitaxial layer caused by different crystal orientations of the silicon wafer, thereby improving the edge flatness of the silicon epitaxial wafer.

[0064] FIGs. 11 and 12 show schematic diagrams of placing a silicon wafer with a V-notch in a $\langle 110 \rangle$ crystal orientation on a susceptor according to an embodiment of the present disclosure. As shown in FIG. 11, when the V-notch 4 of a silicon wafer 3 is aligned along the $\langle 110 \rangle$ crystal orientation, the regions of the silicon wafer that are at intervals of 45° and 135° from the V-groove 4 correspond to the $\langle 100 \rangle$ crystal orientation of the silicon wafer, while the regions at intervals of 90° and 180° correspond to the $\langle 110 \rangle$ crystal orientation of the silicon wafer.

[0065] As shown in FIG. 7, a groove region 6 is present at the edge corresponding to the 0° orientation of the susceptor. Compared to the 45° orientation of the susceptor, the gas flow rate through this groove region 6 increases during epitaxial growth. This increased gas flow rate accelerates the growth rate of the epitaxial layer. Therefore, to ensure uniform growth rates across different regions of the silicon wafer during epitaxial growth, it is necessary to align the $\langle 100 \rangle$ crystal orientation of the silicon wafer with the 0° orientation of the susceptor (where the groove region resides), and to align the $\langle 110 \rangle$ crystal orientation of the silicon wafer with the 45° orientation of the susceptor. This increases the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer during epitaxial growth, resulting in thickness uniformity of the epitaxial layer along both the $\langle 100 \rangle$ and $\langle 110 \rangle$ crystal orientations.

[0066] As shown in FIG. 12, since the orientation of the susceptor is fixed when the epitaxial reactor chamber is installed, the 0° direction of the groove region 6 on the edge of the susceptor corresponds to the direction of the gas injection port, exhaust outlet, wafer load/unload port, or

auxiliary gas injection port of the epitaxial reactor chamber. The silicon wafer with the V-notch in the $\langle 110 \rangle$ crystal orientation is rotated by 45° , which allows the $\langle 100 \rangle$ crystal orientation of the silicon wafer to align with the 0° orientation of the susceptor (the direction corresponding to the groove region of the susceptor, where the gas flow rate on the silicon wafer surface increases), and the $\langle 110 \rangle$ crystal orientation of the silicon wafer to align with the 45° orientation of the susceptor. This compensates for differences in growth rate of the epitaxial layer caused by different crystal orientations of the silicon wafer, thereby improving the edge flatness of the silicon epitaxial wafer.

[0067] The present disclosure further provides an epitaxial silicon wafer, which is manufactured by the above-mentioned method for epitaxial growth of the silicon wafer.

[0068] When the thickness of the epitaxial layer of the epitaxial silicon wafer is not greater than $6\text{ }\mu\text{m}$, a maximum value of an Edge Site Front Quotient Range (ESFQR) of the epitaxial silicon wafer is not greater than 57.1 nm .

[0069] FIG. 13 shows a schematic diagram of the edge flatness of an epitaxial silicon wafer prepared according to an embodiment of the present disclosure. In FIG. 13, the horizontal axis represents the angular position along the radial direction of the silicon wafer, while the vertical axis represents a value of the ESFQR (in nanometers) at the corresponding angular position. It can be seen that the periodic fluctuations in the edge flatness of the epitaxial silicon wafer at 45° intervals have been alleviated, improving the quality of the epitaxial silicon wafer's edge flatness. The value of the ESFQR of the epitaxial silicon wafer can be reduced by 14 nm , effectively improving the quality and yield of the epitaxial silicon wafer.

[0070] In some embodiments, the value of the ESFQR of the epitaxial silicon wafer is inversely proportional to both the depth and the area of the pits. When other parameters of the susceptor remain unchanged, the depth of the pits is increased, the amount of gas participating in a deposition reaction in the groove region during epitaxial growth is increased, the compensation effect for the difference in the growth rate of the epitaxial layer in different crystal orientations of the silicon wafer is better, the value of the ESFQR is smaller, and the improvement effect of the edge flatness quality of the prepared epitaxial silicon wafer is more significant. When other parameters of the susceptor remain unchanged, the area of the pits is increased, the amount of gas participating in a deposition reaction in the groove region during epitaxial growth is increased, the compensation effect for the difference in the growth rate of the epitaxial layer in different crystal orientations of the silicon wafer is better, the value of the ESFQR is smaller, and the improvement effect of the edge flatness quality of the prepared epitaxial silicon wafer is more significant.

[0071] In some embodiments, when the thickness of the epitaxial layer of the epitaxial silicon

wafer is in a range of 3 μm to 4 μm , the value of the ESFQR of the epitaxial silicon wafer is in a range of 23 nm to 33.9 nm; when the thickness of the epitaxial layer of the epitaxial silicon wafer is in a range of 4 μm to 6 μm , the value of the ESFQR of the epitaxial silicon wafer is in a range of 37.4 nm to 57.1 nm.

[0072] In specific embodiment 1, a silicon wafer with a V-notch in the $\langle 100 \rangle$ crystal orientation is selected, and the central angle corresponding to the sector where the groove region of the susceptor is located is in a range of 40° to 50° , for example, it can be 45° ; the depth of the pit is in a range of 0.1 mm to 1 mm, for example, it can be in a range of 0.48 mm to 0.52 mm, or more specifically, 0.5 mm; the area of the pit is in a range of 0.1 mm^2 to 0.4 mm^2 , for example, it can be in a range of 0.18 mm^2 to 0.22 mm^2 , or more specifically, 0.2 mm^2 ; the silicon wafer is placed on the susceptor, and the angle between the central axis of the V-notch and the central axis of the groove region is 0° , so that the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the groove region of the susceptor for epitaxial growth. During epitaxial growth, the flow rate of the carrier gas H_2 is 80,000 sccm, the flow rate of the deposition gas $\text{SiHCl}_3/\text{H}_2$ is 6,000 sccm, and the process temperature is 1100°C , resulting in an epitaxial layer with a thickness in a range of 3.3 μm to 3.5 μm (e.g., 3.5 μm). The resulting epitaxial silicon wafer exhibits a value of the ESFQR of $29.3 \pm 4.6 \text{ nm}$, which is 8.6 nm lower than that obtained with the prior art, thus improving the quality of the epitaxial silicon wafer. This improvement is achieved because the pits in the groove region increase the flow rate of the process gas through the groove region, accelerating the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer, compensating for the difference in growth rates between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations during epitaxial layer growth.

[0073] In specific embodiment 2, a silicon wafer with a V-notch in the $\langle 100 \rangle$ crystal orientation is selected, and the central angle corresponding to the sector where the groove region of the susceptor is located is in a range of 40° to 50° , for example, it can be 45° ; the depth of the pit is in a range of 0.78 mm to 0.82 mm, for example, it can be 0.8 mm; the area of the pit is in a range of 0.38 mm^2 to 0.42 mm^2 , for example, it can be 0.4 mm^2 ; the silicon wafer is placed on the susceptor, and the angle between the central axis of the V-notch and the central axis of the groove region is 0° , so that the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the groove region of the susceptor for epitaxial growth. During epitaxial growth, the flow rate of the carrier gas H_2 is 80,000 sccm, the flow rate of the deposition gas $\text{SiHCl}_3/\text{H}_2$ is 6,000 sccm, and the process temperature is 1100°C , resulting in an epitaxial layer with a thickness in a range of 3.3 μm to 3.5 μm (e.g., 3.5 μm). The resulting epitaxial silicon wafer exhibits a value of the ESFQR of $26.8 \pm$

3.8 nm, which is 11.1 nm lower than that obtained with the prior art, thus improving the quality of the epitaxial silicon wafer. This improvement is achieved because the pits in the groove region increase the flow rate of the process gas through the groove region, accelerating the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer, compensating for the difference in growth rates between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations during epitaxial layer growth. In addition, compared with specific embodiment 1, the depth and area of the pits in the groove region are increased, the amount of gas participating in the deposition reaction in the groove region during epitaxial growth is increased, the compensation effect for the difference in the growth rate of the epitaxial layer in different crystal orientations of the silicon wafer is better, the value of the ESFQR is smaller, and the improvement effect of the edge flatness quality of the prepared epitaxial silicon wafer is more significant.

[0074] In specific embodiment 3, a silicon wafer with a V-notch in the $\langle 100 \rangle$ crystal orientation is selected, and the central angle corresponding to the sector where the groove region of the susceptor is located is in a range of 40° to 50° , for example, it can be 45° ; the depth of the pit is in a range of 0.1 mm to 1 mm, for example, it can be in a range of 0.48 mm to 0.52 mm, or more specifically, 0.5 mm; the area of the pit is in a range of 0.1 mm^2 to 0.4 mm^2 , for example, it can be in a range of 0.18 mm^2 to 0.22 mm^2 , or more specifically, 0.2 mm^2 ; the silicon wafer is placed on the susceptor, and the angle between the central axis of the V-notch and the central axis of the groove region is 0° , so that the $\langle 100 \rangle$ crystal orientation of the silicon wafer is aligned with the groove region of the susceptor for epitaxial growth. During epitaxial growth, the flow rate of the carrier gas H_2 is 80,000 sccm, the flow rate of the deposition gas $\text{SiHCl}_3/\text{H}_2$ is 6,000 sccm, and the process temperature is 1100°C , resulting in an epitaxial layer with a thickness in a range of $4.8 \mu\text{m}$ to $5 \mu\text{m}$ (e.g., $5 \mu\text{m}$). The resulting epitaxial silicon wafer exhibits a value of the ESFQR of $48.4 \pm 8.7 \text{ nm}$, which is reduced compared to that obtained by the prior art, thus improving the quality of the epitaxial silicon wafer. This improvement is achieved because the pits in the groove region increase the flow rate of the process gas through the groove region, accelerating the growth rate of the epitaxial layer in the $\langle 100 \rangle$ crystal orientation of the silicon wafer, compensating for the difference in growth rates between the $\langle 110 \rangle$ and $\langle 100 \rangle$ crystal orientations during epitaxial layer growth.

[0075] In specific embodiment 4, a silicon wafer with a V-notch in the $\langle 100 \rangle$ crystal orientation is selected, and the central angle corresponding to the sector where the groove region of the susceptor is located is in a range of 40° to 50° , for example, it can be 45° ; the depth of the pit is in a range of 0.78 mm to 0.82 mm, for example, it can be 0.8 mm; the area of the pit is in a range of

0.38 mm² to 0.42 mm², for example, it can be 0.4 mm²; the silicon wafer is placed on the susceptor, and the angle between the central axis of the V-notch and the central axis of the groove region is 0°, so that the <100> crystal orientation of the silicon wafer is aligned with the groove region of the susceptor for epitaxial growth. During epitaxial growth, the flow rate of the carrier gas H₂ is 80,000 sccm, the flow rate of the deposition gas SiHCl₃/H₂ is 6,000 sccm, and the process temperature is 1100°C, resulting in an epitaxial layer with a thickness in a range of 4.8 μm to 5 μm (e.g., 5 μm). The resulting epitaxial silicon wafer exhibits a value of the ESFQR of 43.8±6.4 nm, which is reduced compared to that obtained by the prior art, thus improving the quality of the epitaxial silicon wafer. This improvement is achieved because the pits in the groove region increase the flow rate of the process gas through the groove region, accelerating the growth rate of the epitaxial layer in the <100> crystal orientation of the silicon wafer, compensating for the difference in growth rates between the <110> and <100> crystal orientations during epitaxial layer growth. In addition, compared with specific embodiment 3, the depth and area of the pits in the groove region are increased, the amount of gas participating in the deposition reaction in the groove region during epitaxial growth is increased, the compensation effect for the difference in growth rate of the epitaxial layer in different crystal orientations of the silicon wafer is better, the value of the ESFQR is smaller, and the improvement effect of the edge flatness quality of the prepared epitaxial silicon wafer is more significant.

[0076] It should be noted that the various embodiments in this specification are described in a progressive manner. Identical or similar parts between the various embodiments can be understood by referring to each other. Each embodiment focuses on the differences from other embodiments. In particular, with respect to the method embodiments, since they are basically similar to the product embodiments, the description is relatively simple. For relevant parts, reference can be made to the corresponding descriptions in the product embodiments.

[0077] Unless otherwise defined, the technical or scientific terms used in the present disclosure should have the usual meanings understood by those ordinary skill in the art to which the present disclosure belongs. The terms "first", "second" and similar words used in the present disclosure do not indicate any order, quantity or importance, but are merely used to distinguish different components. Terms such as "comprising" or "including" mean that the elements or items preceding the word cover the elements or items listed after the word and their equivalents, without excluding other elements or items. Terms such as "connect" or "connected" are not limited to physical or mechanical connections, but may include electrical connections, whether direct or indirect. Terms such as "upper," "lower," "left," and "right" are used merely to indicate relative positional

relationships. When the absolute position of the described object changes, the relative positional relationship may also change accordingly.

[0078] It is to be understood that when an element such as a layer, film, region, or substrate is referred to as being “ on ” or “ under ” another element, it can be “directly on ” or “ under ” the other element or intervening elements may be present.

[0079] In the description of the above embodiments, specific features, structures, materials or characteristics may be combined in any suitable manner in one or more embodiments or examples.

[0080] The above are merely specific embodiments of the present disclosure, but the protection scope of the present disclosure is not limited thereto. Any changes or substitutions that can be easily conceived by those skilled in the art within the technical scope disclosed in the present disclosure should be included in the protection scope of the present disclosure. Therefore, the protection scope of the present disclosure should be defined by the scope of the claims.

What is claimed is:

1. A susceptor for epitaxial growth of a silicon wafer, comprising:
a disc-shaped supporting part configured to support the silicon wafer;
an annular periphery extending radially outward from the disc-shaped supporting part, wherein the annular periphery is provided with a plurality of groove regions that is spaced apart from each other and uniformly distributed along a circumferential direction of the annular periphery, each of the groove regions is annular sector-shaped and provided with a plurality of pits arranged in an array.
2. The susceptor according to claim 1, wherein a central angle corresponding to a sector in which the groove region is located is in a range of 40° to 60°.
3. The susceptor according to claim 1, wherein four groove regions are uniformly distributed along the circumferential direction of the annular periphery.
4. The susceptor according to claim 1, wherein a depth of the pit is in a range of 0.1 mm to 1 mm; and/or
an area of the pit is in a range of 0.1 mm² to 0.4 mm².
5. A device for epitaxial growth of a silicon wafer, comprising:
the susceptor according to any one of claims 1 to 4;
a reactor chamber configured to accommodate the susceptor, wherein the susceptor divides the reactor chamber into an upper reactor chamber and a lower reactor chamber, and the silicon wafer is arranged in the upper reactor chamber;
a gas inlet configured to deliver silicon source gas into the upper reactor chamber to grow an epitaxial layer on the silicon wafer;
an exhaust outlet configured to discharge exhaust gas generated during epitaxial growth from the reactor chamber.
6. A method for epitaxial growth of a silicon wafer, the method being applied to the device according to claim 5, and comprising:
placing the silicon wafer on the susceptor to allow a <100> crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery;
delivering the silicon source gas into the upper reactor chamber via the gas inlet to grow the epitaxial layer on the silicon wafer;
wherein a flow rate of the silicon source gas flowing through the groove region is greater than a flow rate of the silicon source gas flowing through other area of the annular periphery, to

allow a thickness uniformity of the epitaxial layer grown on the silicon wafer;

discharging the exhaust gas generated during epitaxial growth from the reactor chamber via the exhaust outlet.

7. The method according to claim 6, wherein the placing the silicon wafer on the susceptor to allow a $\langle 100 \rangle$ crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery comprises:

obtaining a crystal orientation corresponding to a V-notch of the silicon wafer;

when the V-notch is in the $\langle 110 \rangle$ crystal orientation of the silicon wafer, placing the silicon wafer on the susceptor to allow an angle between a central axis of the V-notch and the central axis of the groove region to be 45° .

8. The method according to claim 6, wherein the placing the silicon wafer on the susceptor to allow a $\langle 100 \rangle$ crystal orientation of the silicon wafer to be aligned with a central axis of the groove region of the annular periphery comprises:

obtaining a crystal orientation corresponding to a V-notch of the silicon wafer;

when the V-notch is in the $\langle 100 \rangle$ crystal orientation of the silicon wafer, placing the silicon wafer on the susceptor to allow an angle between the central axis of the V-notch and the central axis of the groove region to be 0° .

9. An epitaxial silicon wafer manufactured by the method for the epitaxial growth of the silicon wafer according to any one of claims 6 to 8,

wherein when the thickness of the epitaxial layer of the epitaxial silicon wafer is not greater than $6\text{ }\mu\text{m}$, a maximum value of an Edge Site Front Quotient Range (ESFQR) of the epitaxial silicon wafer is not greater than 57.1 nm .

10. The epitaxial silicon wafer according to claim 9, wherein when the thickness of the epitaxial layer of the epitaxial silicon wafer is in a range of $3\text{ }\mu\text{m}$ to $4\text{ }\mu\text{m}$, a value of the ESFQR of the epitaxial silicon wafer is in a range of 23 nm to 33.9 nm ; and when the thickness of the epitaxial layer of the epitaxial silicon wafer is in a range of $4\text{ }\mu\text{m}$ to $6\text{ }\mu\text{m}$, a value of the ESFQR of the epitaxial silicon wafer is in a range of 37.4 nm to 57.1 nm .