FIG. 1

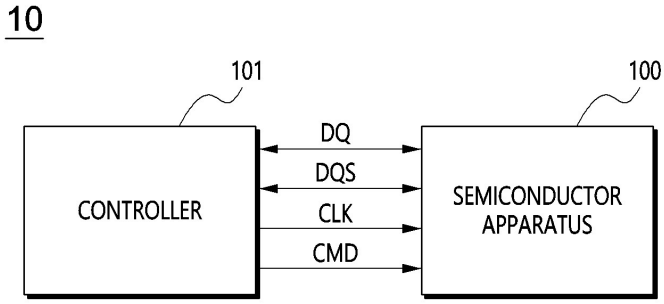

10
101
100
CONTROLLER
DQ
DQS
CLK
CMD
SEMICONDUCTOR APPARATUS

FIG. 2

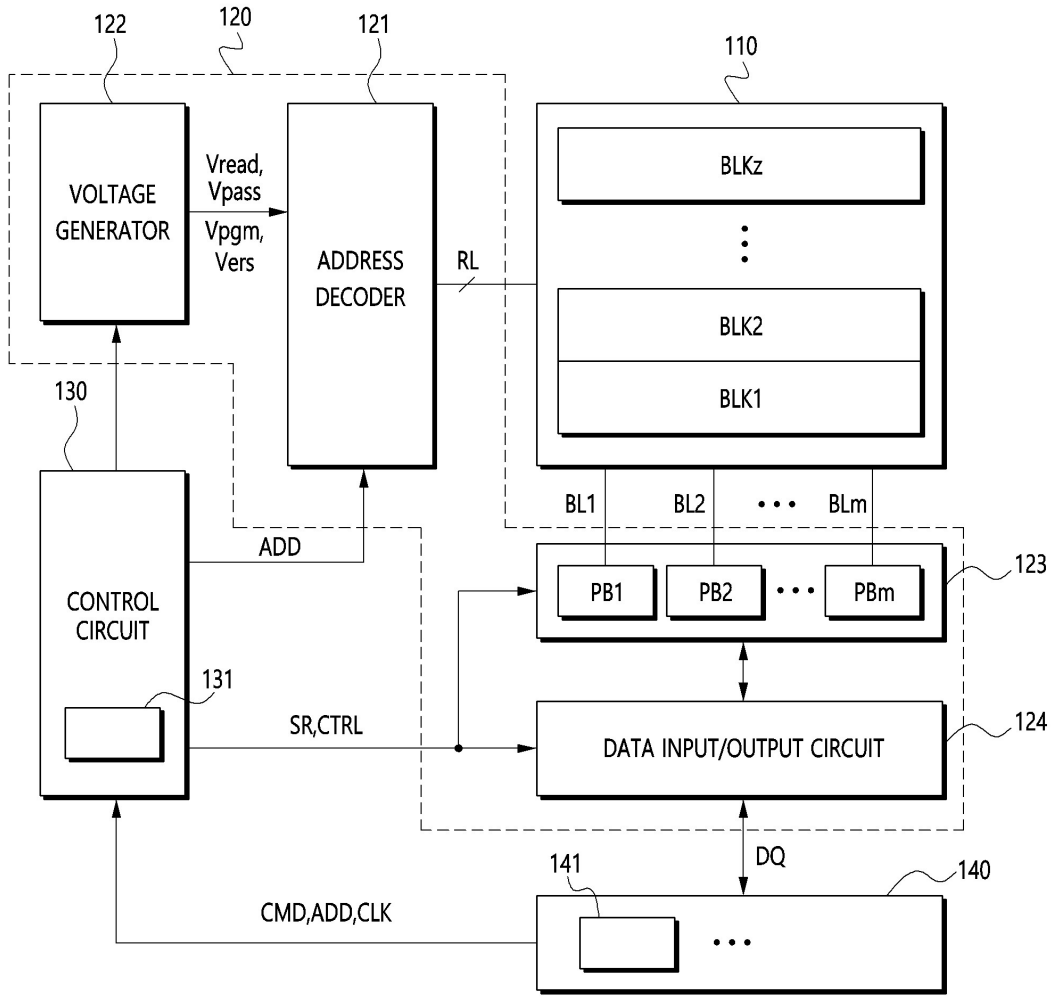

100
122
120
121
110
VOLTAGE GENERATOR
Vread, Vpass
Vpgm, Vers
ADDRESS DECODER
RL
BLKz
BLK2
BLK1
130
BL1
BL2
BLm
ADD
CONTROL CIRCUIT
PB1
PB2
PBm
123
131
SR,CTRL
DATA INPUT/OUTPUT CIRCUIT
124
DQ
141
140
CMD,ADD,CLK

FIG. 3

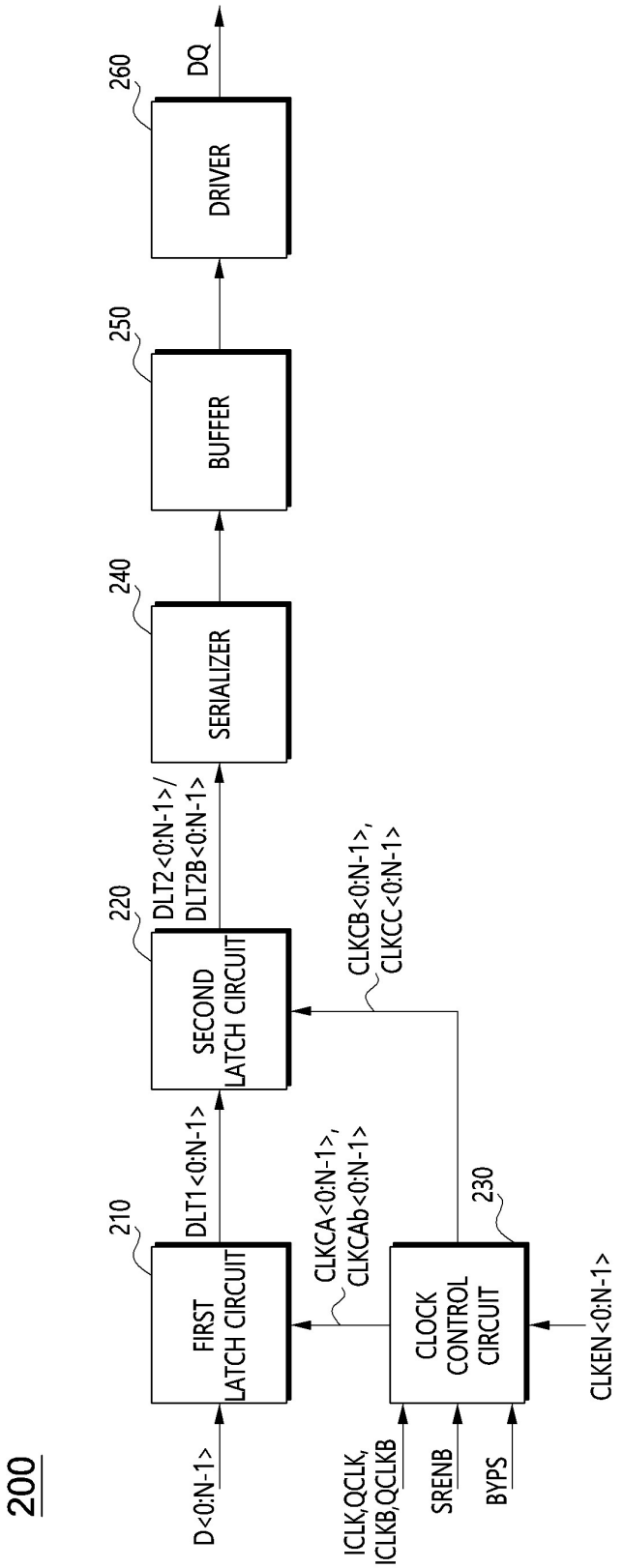

200
D<0:N-1>
ICLK,QCLK,
ICLKB,QCLKB
SRENB
BYPS
CLKEN<0:N-1>
210
FIRST
LATCH CIRCUIT
DLT1<0:N-1>
CLKCA<0:N-1>,
CLKCAb<0:N-1>
230
CLOCK
CONTROL
CIRCUIT
220
SECOND
LATCH CIRCUIT
DLT2<0:N-1>/
DLT2B<0:N-1>
CLKCB<0:N-1>,
CLKCC<0:N-1>
240
SERIALIZER
250
BUFFER
260
DRIVER
DQ

FIG. 4

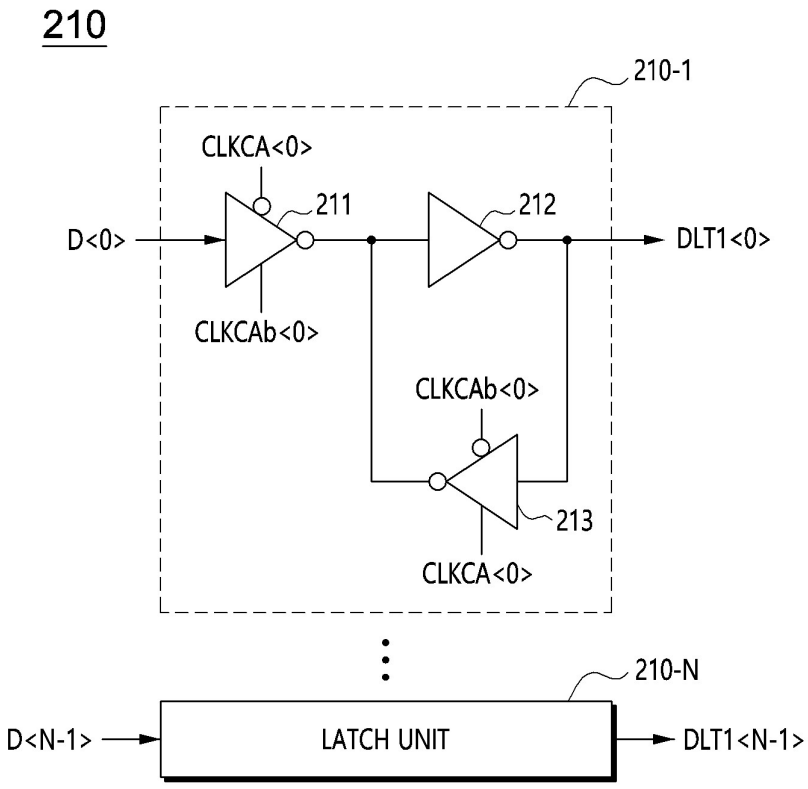

210
210-1
CLKCA<0>
211
212
D<0>
DLT1<0>
CLKCAb<0>
CLKCAb<0>
213
CLKCA<0>
210-N
D<N-1>
LATCH UNIT
DLT1<N-1>

FIG. 5

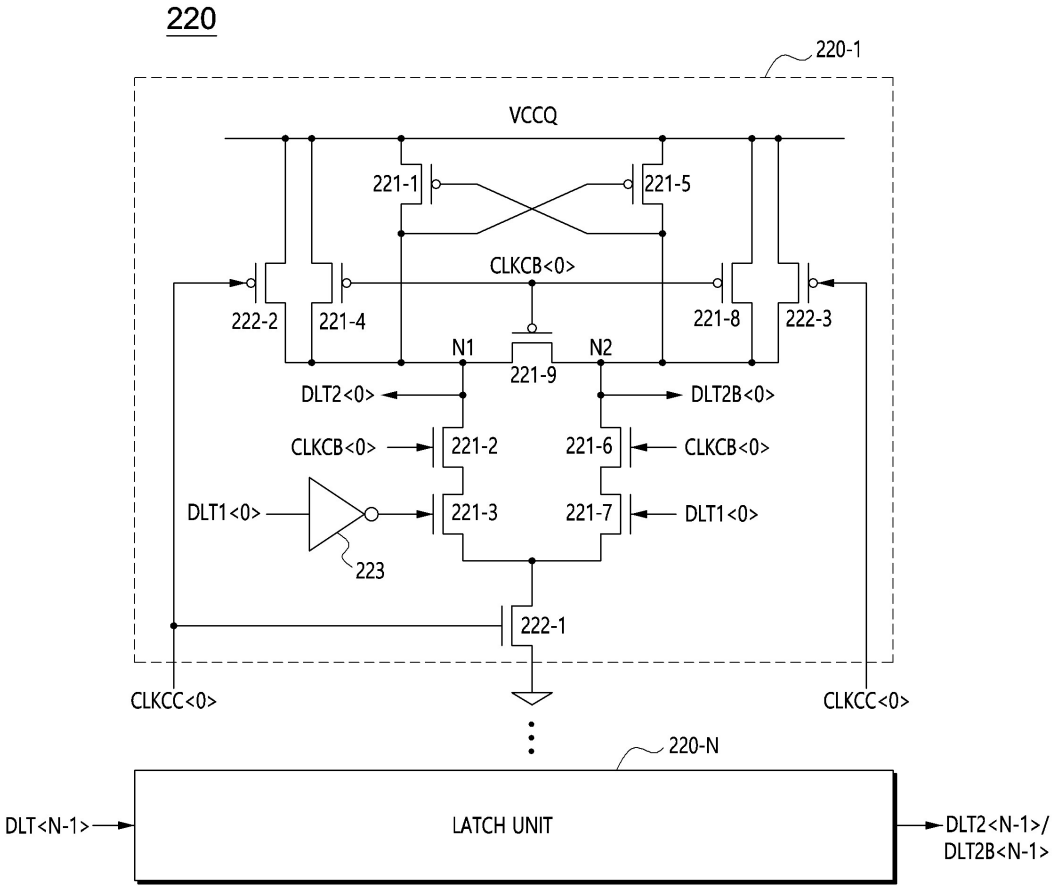

220
220-1
VCCQ
221-1
221-5
CLKCB<0>
222-2
221-4
221-8
222-3
N1
N2
221-9
DLT2<0>
DLT2B<0>
CLKCB<0>
221-2
221-6
CLKCB<0>
DLT1<0>
221-3
221-7
DLT1<0>
223
222-1
CLKCC<0>
CLKCC<0>
220-N
DLT<N-1>
LATCH UNIT
DLT2<N-1>/
DLT2B<N-1>

FIG. 6

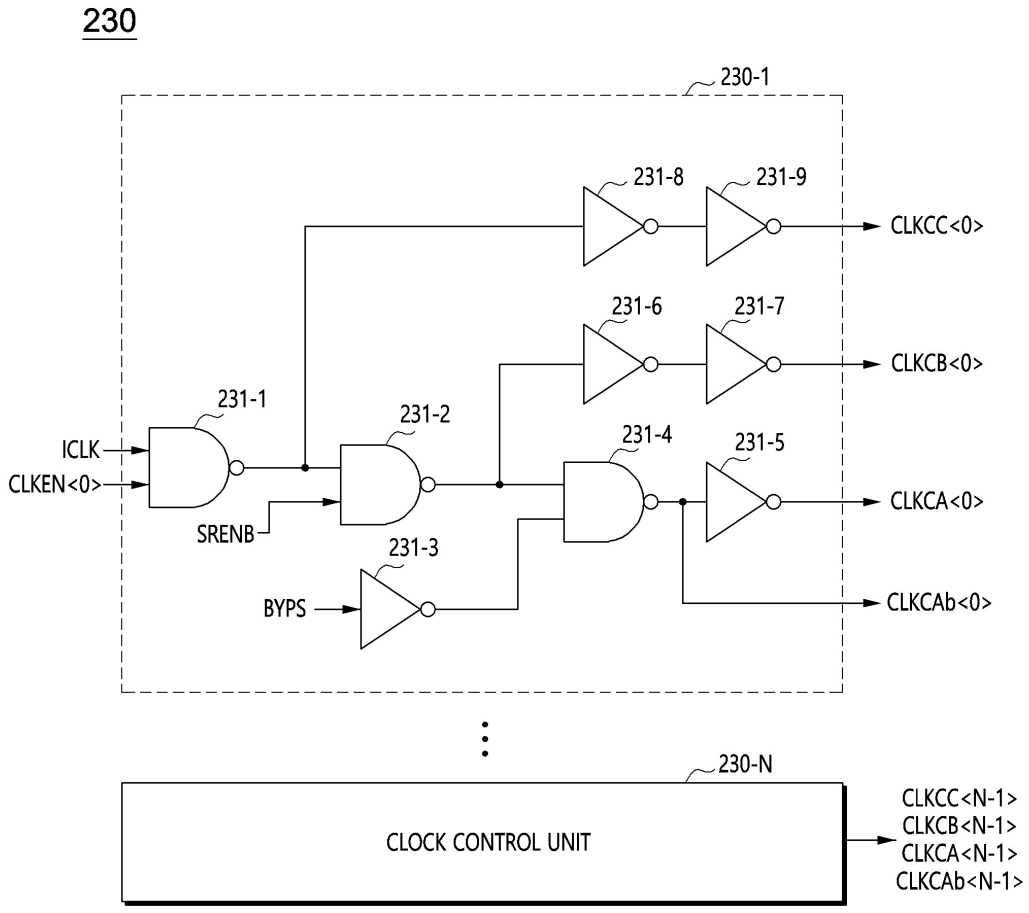

230
230-1
231-8
231-9
CLKCC<0>
231-6
231-7
CLKCB<0>
231-1
231-2
231-4
231-5
ICLK
CLKEN<0>
CLKCA<0>
SRENB
231-3
BYPS
CLKCAb<0>
230-N
CLOCK CONTROL UNIT
CLKCC<N-1>
CLKCB<N-1>
CLKCA<N-1>
CLKCAb<N-1>

FIG. 7

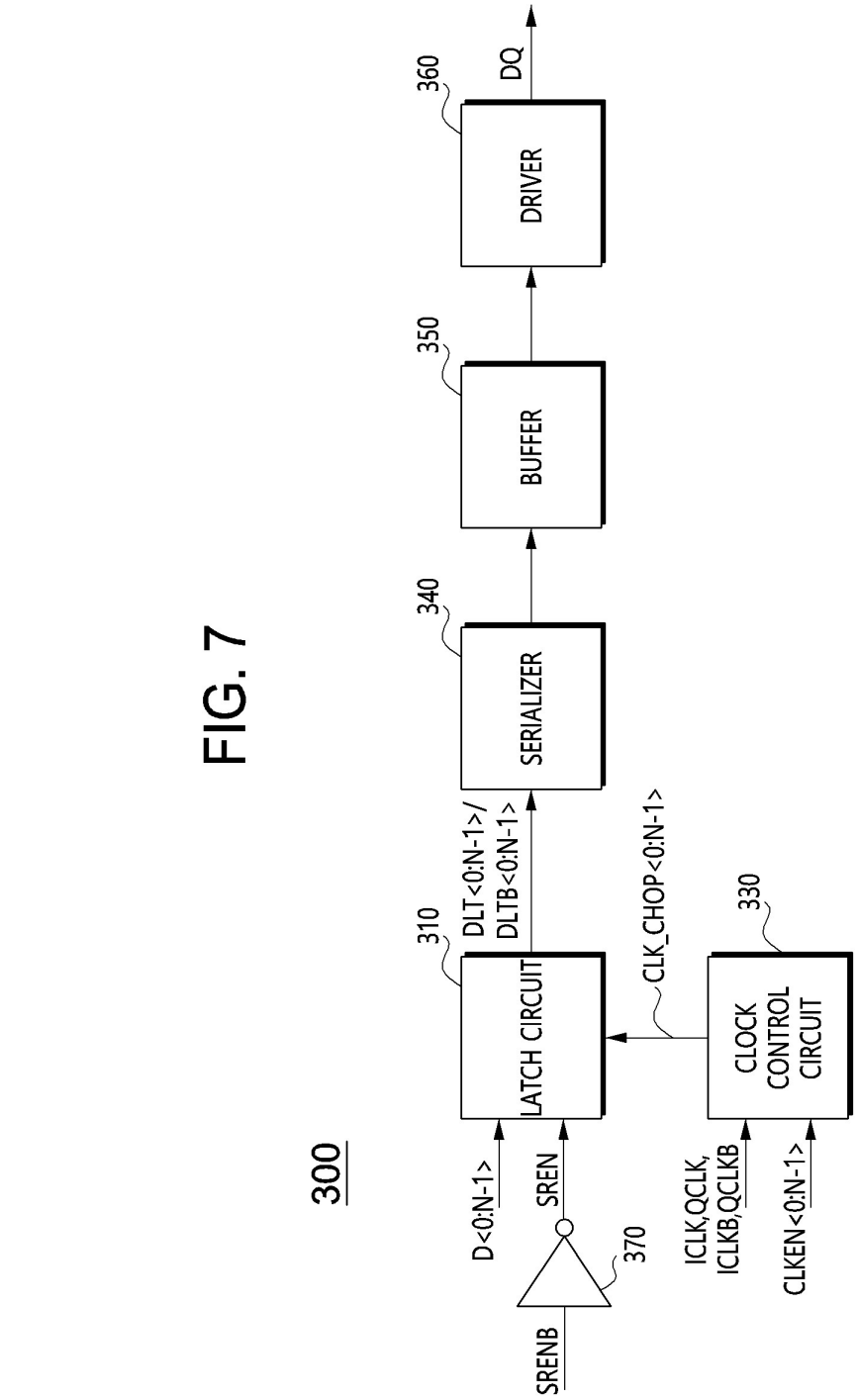

300
310
LATCH CIRCUIT
340
SERIALIZER
350
BUFFER
360
DRIVER
DQ
DLT<0:N-1>/
DLTB<0:N-1>
CLK_CHOP<0:N-1>
330
CLOCK
CONTROL
CIRCUIT
D<0:N-1>
SREN
SRENB
370
ICLK,QCLK,
ICLKB,QCLKB
CLKEN<0:N-1>

FIG. 8

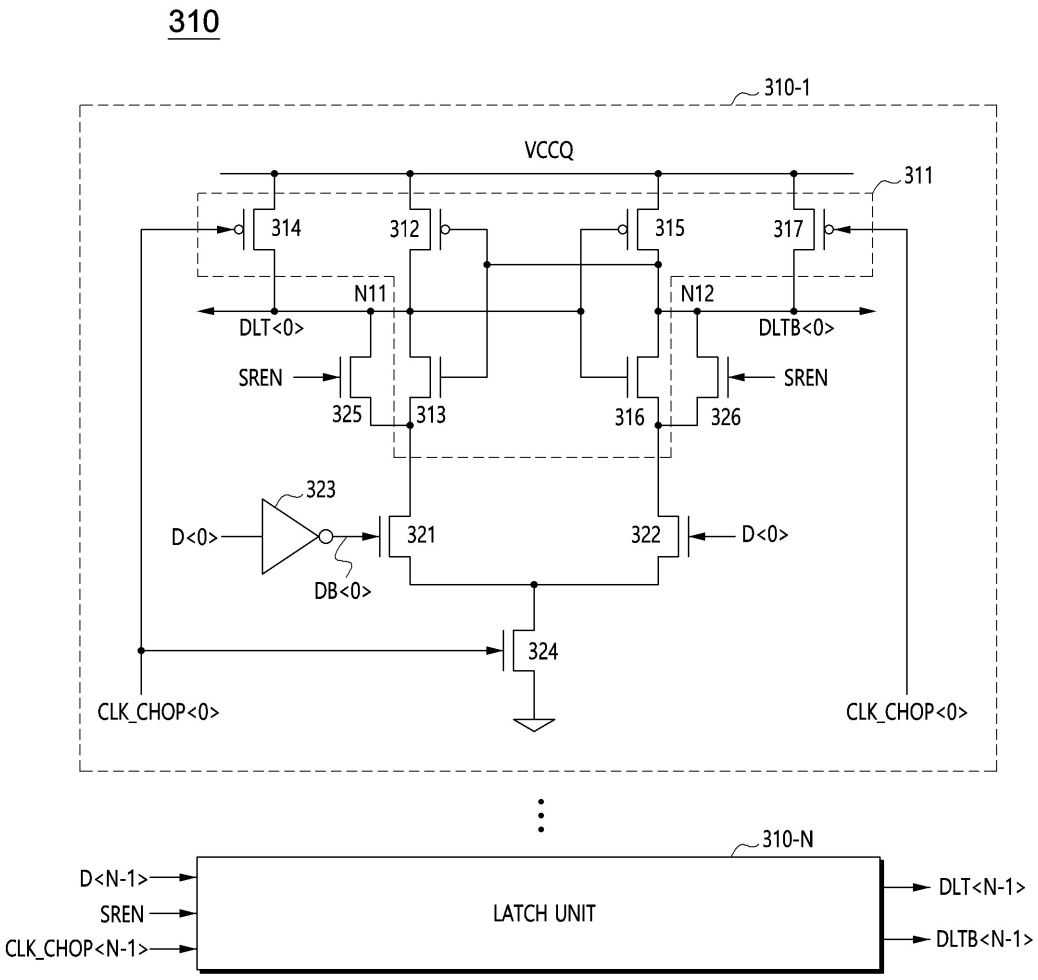

310
310-1
VCCQ
311
314
312
315
317
N11
N12
DLT<0>
DLTB<0>
SREN
SREN
325
313
316
326
323
D<0>
321
322
D<0>
DB<0>
324
CLK_CHOP<0>
CLK_CHOP<0>
310-N
D<N-1>
SREN
CLK_CHOP<N-1>
LATCH UNIT
DLT<N-1>
DLTB<N-1>

FIG. 9

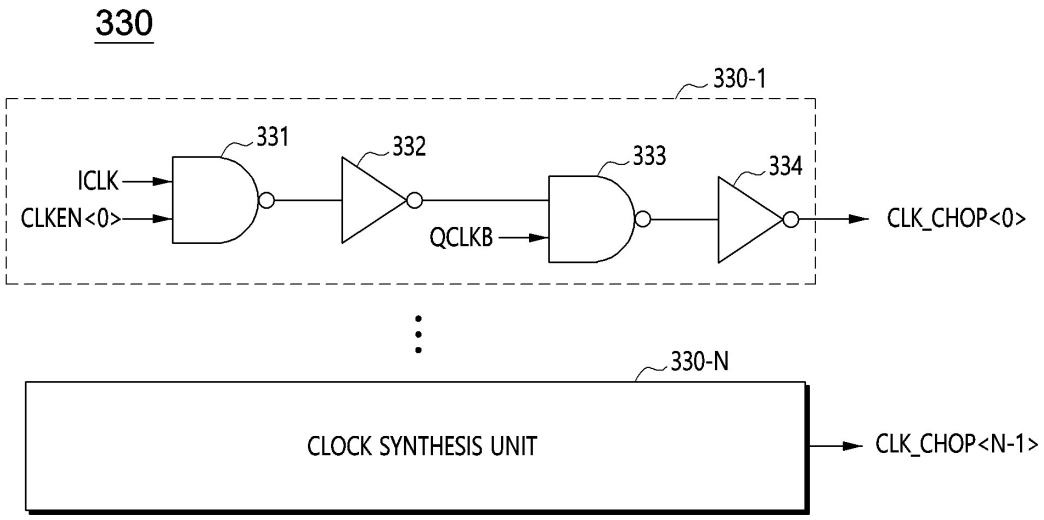
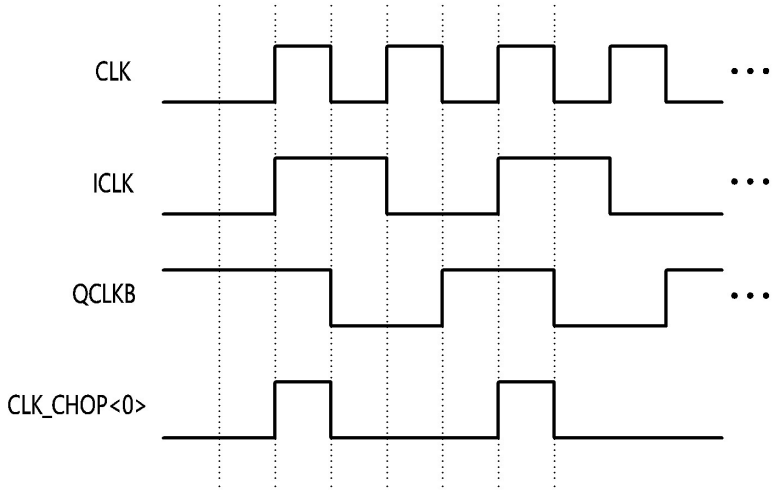

330
330-1
331
332
333
334
ICLK
CLKEN<0>
QCLKB
CLK_CHOP<0>
330-N
CLOCK SYNTHESIS UNIT
CLK_CHOP<N-1>

FIG. 10


CLK
ICLK
QCLKB
CLK_CHOP<0>