

CLOCK SYNCHRONIZATION SCHEME FOR FRACTIONAL
MULTIPLICATION SYSTEMS

ABSTRACT

A circuit for synchronizing a multiplied system clock signal includes a device for generating a system clock signal (10, 34), a first device (30) that receives the system clock signal and generates a synchronization signal (20) and at least one second device (31, 32) that receives the system clock signal and the synchronization signal. Each of the second devices includes a device (40, 71, 74, 81, 84) for multiplying the system clock signal to produce the multiplied system clock signal and a device for synchronizing the multiplied system clock signal with each other multiplied system clock signal produced by the other second devices based on the synchronization signal.

Figure 3

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