

Description

The invention relates to a sample-and-hold circuit arrangement comprising an input terminal, at least first and second switches, a first capacitor, a differential amplifier and a second amplifier of an inverting type, said second amplifier having an input terminal connected to an output terminal of said differential amplifier, the input terminal of the arrangement being connected to an input of the differential amplifier via the first switch and an output of the second amplifier being connected to said input of the differential amplifier via the second switch.

Such a sample-and-hold circuit arrangement is known from United States Patent Specification 3,696,305. During the hold intervals the output voltage of this circuit arrangement is hardly influenced by the offset voltage of the differential amplifier.

In this respect the offset voltage of the differential amplifier is to be understood to mean that voltage between the inputs of the differential amplifier which yields a zero signal on the output terminal of this amplifier.

However, a disadvantage of the known circuit arrangement is that its output voltage decreases to substantially zero volts during the sampling intervals. If such circuit arrangements are employed for example in combination with electrical memories for data processing equipment it is often desirable that the output voltage of the arrangement during a specific sampling interval remains substantially the same as in the directly preceding hold interval.

It is the object of the invention to provide a sample-and-hold circuit arrangement of the type defined in the opening paragraph, in which the output voltage during a hold interval is not influenced by the offset voltage of the differential amplifier and in which the output voltage during a sampling interval is substantially equal to that during the directly preceding hold interval.

A sample-and-hold circuit arrangement in accordance with the invention is characterized in that the first capacitor is arranged in the connection from the first switch to the differential amplifier, and in that the arrangement also comprises a third amplifier whose input is connected to the output of the differential amplifier via a third switch, which third amplifier has an output terminal connected, via a fourth switch, to that side (electrode) of the first capacitor which is connected to the first switch, the input terminal and the output terminal of the third amplifier being interconnected via a branch including a second capacitor.

An advantage of the circuit arrangement in accordance with the invention is that during a hold interval the output voltage of the arrangement being the voltage of the output terminal of the third amplifier is hardly influenced by the offset voltage of the differential amplifier and during a sampling interval the output voltage of the arrangement is substantially the same as in the directly preceding hold interval.

The invention is based on the idea of using the second amplifier only for eliminating the offset voltage of the differential amplifier. The third amplifier

across which the branch including the second capacitor is connected, serves for maintaining the output voltage during a succeeding sampling interval.

In an embodiment of the invention the second amplifier and the third amplifier are constructed in such way that their transfer characteristics are substantially identical.

An advantage of this improvement is that when the second amplifier and the third amplifier are employed alternately in conformity with the sampling interval and the hold interval respectively, the offset voltage of the differential amplifier is substantially the same in the two intervals. This means that also during the sampling interval the voltage on the output terminal of the third amplifier is practically independent of this offset voltage.

The invention will now be described in more detail, by way of example, with reference to the drawing. In the drawing:

Fig. 1 is a basic diagram of a sample-and-hold circuit arrangement in accordance with the invention; and

Fig. 2 shows a practical example of the sample-and-hold circuit arrangement shown in Fig. 1.

The arrangement shown in Fig. 1 comprises an input terminal 1 which is connected to the terminal A of a capacitor 3 via a switch 2, the other terminal B of said capacitor being connected to the non-inverting input 4 of a differential amplifier 5, whose inverting input 6 is connected to a point carrying a reference voltage V_R . The output terminal of the differential amplifier is connected to an input of a second amplifier 8 of an inverting type via a switch 7, the output of said amplifier 8 being connected to its input by a capacitor 9. This output is also connected to the non-inverting input 4 of the differential amplifier 5 via a switch 10.

Further, the output terminal of the differential amplifier 5 is connected to the input of a third amplifier 12 of an inverting type via a switch 11, the output 13 of this amplifier 12 being connected to its input by a capacitor 14. The output 13 is also connected to the terminal A of the capacitor 3 via a switch 15. The output terminal 16 connected to the output 13 constitutes the output of the circuit arrangement.

The arrangement operates as follows. An analog voltage V_{IN} is applied to the input terminal 1. During a sampling interval the switches 2, 7 and 10 are closed. The other switches are then open. During a hold interval the switches 11 and 15 are closed. The other switches are then open.

In the sampling interval the amplifier 5 is connected to the amplifier 8 to form a voltage follower. Terminal B of the capacitor 3 is then at a potential $V_R + V_{offset}$, where V_{offset} is the offset voltage of the differential amplifier 5. This results in a voltage $V_{IN} - (V_R + V_{offset})$ across the capacitor 3, because the potential on terminal A of the capacitor 3 is V_{IN} .

In the succeeding hold interval the amplifier 8 is disconnected from 5 and the amplifier 12 is connected to the amplifier 5. The input voltage to the differ-

ential amplifier 5 is then changed because terminal A of the capacitor 3 (see Fig. 1) is connected to the output 13 of the third amplifier 12. However, the charge of the capacitor 3 remains the same.

The potential on the output 13 and hence that on output terminal 16 now changes until the potential on terminal B is restored to the value during the sampling interval. This also means that the potential on terminal A of the capacitor 3 and hence that on the output 16, is restored to the value V_{IN} in the preceding hold interval.

As a result of the presence of the capacitor 14 V_{IN} on the output 16 is also maintained during the succeeding sampling interval. This will be explained with reference to Fig. 2.

In Fig. 2, which shows a practical embodiment of the invention, circuit elements corresponding to those in Fig. 1 bear the same reference numerals. The three amplifiers including the capacitors are shown in separate boxes.

The differential amplifier 5 comprises two N-channel MOS transistors 34 and 35 which are arranged as a differential pair whose common-source terminal is connected to the negative power-supply terminal 31 by means of a current source 36. The gate of the transistor 34 is connected to capacitor 3 and the gate of the transistor 35 is connected to a point for carrying a reference voltage V_R . The drain of the transistor 34 is connected to the output of the differential amplifier 5 by a current mirror comprising P-channel MOS transistors 32 and 33, and the drain of the transistor 35 is connected directly to said output. By means of a switch 7 said output can be connected to the input of the amplifier 8 which comprises a P-channel MOS transistor 40 loaded by a current source 41. The output of this amplifier is fed back to the input by the series arrangement of a resistor 37 and a capacitor 9. The resistor 37 serves to improve the stability of the amplifier.

The amplifier 12 comprises a P-channel MOS transistor 53 which is driven directly by the output of the amplifier 5 when the switch 11 is closed. An N-channel MOS transistor 55 is arranged in series with the transistor 53 and is driven in phase opposition with the latter. For this purpose the amplifier 12 comprises a first current mirror comprising P-channel MOS transistors 51 and 52. The current gain of this current mirror is, for example, two. The input of this current mirror is connected to a current source 56 and to the drain of a P-channel MOS transistor 50 arranged in parallel with the transistor 53. The area of this transistor 50 is, for example, 1/5 of that of the transistor 53. The output of the first current mirror is connected to the input of a second current mirror comprising the transistors 54 and 55. The current gain of this current mirror is, for example, ten. The output 13 of the amplifier 12 is connected to the input of the amplifier 12, by the series arrangement of a resistor 56 and a capacitor 14. The resistor 56 serves to improve the stability of the amplifier.

If the current, from the current source 56 is 25 μA , the negative feedback via the resistor 56 and

the capacitor 14 ensures that the voltage on the input becomes such that the quiescent current through the transistors 53 and 55 is substantially 100 μA . The current from the current source 56 is then distributed between the transistors 50 and 51 in such a way that the current in the transistor 50 is 20 μA and that in the transistor 51 is 5 μA . The voltage on the input of the amplifier 12 can now increase until the transistor 50 is cut off and the transistor 51 carries the full current from the current source 56. The maximum output current is then 500 μA , which is relatively large in comparison with the quiescent current.

As already stated in the description with reference to Fig. 1, the switches 7 and 11 are closed alternatively, so that voltage is applied to the capacitor 9 and the capacitor 14, alternatively.

The voltage on the capacitor 14 is maintained during a sampling interval. Consequently, the potential on the output 13 is maintained during the sampling interval.

In the present example the reference voltage V_R is approximately 5 V,

the capacitor 3 is approximately 10 pF,
the capacitor 9 is approximately 10 pF,
the capacitor 14 is approximately 10 pF,
the resistor 37 is approximately 20 kOhms, and
the resistor 56 is approximately 20 kOhms,
the current sources 36 and 41 approximately 25 μA .

The switches 2, 7, 10 and 15 may be, for example, solid-state switching devices. The switches 2 and 15 may be combined to form a change-over switch.

In the embodiment of Fig. 2 the offset voltage of the differential amplifier in the switched-in condition of the inverting amplifier 8 is substantially equal to that in the switched-in condition of the amplifier 12. This is because the transfer characteristics of the amplifiers 8 and 12 are substantially identical.

By means of the circuit arrangement shown in the Figures an analog voltage (on 1) is converted into a sampled voltage (on 16), which conversion is hardly influenced by the offset voltage of the differential amplifier 5, whilst during a sampling interval the sampled voltage is maintained at the level which it had in the directly preceding hold interval.

Claims

1. A sample-and-hold circuit arrangement comprising an input terminal, at least first and second switches, a first capacitor, a differential amplifier and a second amplifier of an inverting type, said second amplifier having an input terminal connected to an output terminal of said differential amplifier, the input terminal of the arrangement being connected to an input of the differential amplifier via the first switch and an output of the second amplifier being connected to said input of the differential amplifier via the second switch, characterized in that the first capacitor is arranged in the connection from the first switch to the differential amplifier, and in that the arrangement also comprises a third amplifier whose input is connected to the output of the differential amplifier via a third switch which

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third amplifier has an output terminal connected, via a fourth switch, to that side (electrode) of the first capacitor which is connected to the first switch, the input terminal and the output terminal of the third amplifier being interconnected via a branch including a second capacitor.

2. A sample-and-hold circuit arrangement as claimed in Claim 1, characterized in that the second amplifier and the third amplifier are constructed in such a way that their transfer characteristics are substantially identical.

Patentansprüche

1. Abtast- und Halteschaltungsanordnung mit einer Eingangsklemme, wenigstens ersten und zweiten Schaltern, einem ersten Kondensator, einem Differenzverstärker und einem zweiten Verstärker von einem invertierenden Typ, dessen Eingangsklemme mit einer Ausgangsklemme des Differenzverstärkers verbunden ist, wobei die Eingangsklemme der Anordnung über den ersten Schalter an den Eingang des Differenzverstärkers und ein Ausgang des zweiten Verstärkers über den zweiten Schalter an den Eingang des Differenzverstärkers angeschlossen sind, dadurch gekennzeichnet, daß der erste Kondensator in der Verbindung vom ersten Schalter zum Differenzverstärker angeordnet ist, und daß die Anordnung noch einen dritten Verstärker enthält, dessen Eingang mit dem Ausgang des Differenzverstärkers über einen dritten Schalter verbunden ist, wobei der dritte Verstärker mit einer Ausgangsklemme über einen vierten Schalter an jene Seite (Elektrode) des ersten Kondensators angeschlossen ist, die mit dem ersten Schalter verbunden ist, wobei die Eingangsklemme und die Ausgangsklemme des dritten Verstärkers über einen zweiten Kondensator enthaltenden Abzweig miteinander verbunden sind.

2. Abtast- und Halteschaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß der zweite Verstärker und der dritte Verstärker derart aufgebaut sind, daß ihre Übergangskennlinien im wesentlichen gleich sind.

Revendications

1. Circuit d'échantillonnage et de maintien muni d'une borne d'entrée, d'au moins un premier et un deuxième commutateur, d'un premier condensateur, d'un amplificateur différentiel et d'un deuxième amplificateur du type inverseur, ledit deuxième amplificateur comportant une borne d'entrée reliée à une borne de sortie dudit amplificateur différentiel, ladite borne d'entrée du circuit étant connectée à une entrée de l'amplificateur différentiel par l'intermédiaire du premier commutateur et une sortie du deuxième amplificateur étant connectée à ladite entrée de l'amplificateur différentiel par l'intermédiaire du deuxième commutateur, caractérisé en ce que le premier condensateur est disposé dans la connexion entre le premier commutateur et l'amplificateur différentiel et en ce que le circuit comporte également un troisième amplificateur dont l'entrée est connectée à la sortie de l'amplificateur différen-

tiel par l'intermédiaire d'un troisième commutateur, lequel troisième amplificateur est muni d'une borne de sortie connectée par l'intermédiaire d'un quatrième commutateur au côté (électrode) du premier condensateur qui est connecté au premier commutateur, la borne d'entrée et la borne de sortie du troisième amplificateur étant interconnectées par l'intermédiaire d'une dérivation comportant un deuxième condensateur.

2. Circuit d'échantillonnage et de maintien selon la revendication 1, caractérisé en ce que le deuxième amplificateur et le troisième amplificateur sont réalisés de façon que leurs caractéristiques de transfert soient pratiquement identiques.

