METHOD FOR PACKAGING CIRCUITS AND PACKAGED CIRCUITS

Technical Field

The present invention relates generally to circuit packaging, and in particular to apparatus and methods for packaging integrated circuits.

Background

Wafers are fabricated with a plurality of dies each having a plurality of integrated circuit elements therein. A die represents one individual chip that must be separated from adjacent dies before packaging. Contacts are added to the die before packaging. One type of contact is a bond pad. Wafer level packaging (WLP) refers to the integrated circuit packaging formed at the wafer level, usually at the wafer foundry. WLP is normally considered as a true chip size package. WLP thus provides lower cost and smallest size of commercial packaging. It is desired to reduce the profile and/or thickness of packaged components using a commercially viable process.

For the reasons stated above, for other reasons stated below, and for other reasons which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an improved electronic component package and methods of packaging electronic components.

Summary

The present invention is directed to forming a wafer-scale, integrated circuit package. That is, the present invention is directed to chip-scale packages An embodiment of the present invention includes fixing a die on a substrate, forming electrical connections from die to terminals on the substrate, and removing a backside of substrate to expose the terminals. In an embodiment, removing the backside of the substrate includes backgrinding the substrate to expose a backside of the terminals. In an embodiment, fixing the die to the

substrate includes applying an adhesive to the top surface of the substrate and placing the die on the adhesive. The adhesive is cured to fix the die to the substrate. In an embodiment, the die is placed vertically over the terminals for that die. The electrical connections are formed from the die through the adhesive layer to the terminals. In an embodiment, the terminals are conductive pads formed on the top surface of the substrate. In an embodiment, the electrical connections are metal traces from the die to the conductive pads. In an embodiment, the adhesive layer is removed from around the periphery of the die to expose the terminals. In an embodiment, terminals on the substrate are interconnected to provide greater functionality of chip-scale package. In an embodiment, the die is singulated from adjacent die with a portion of the substrate remaining with the die. The singulated die package forms individual chip scale packages that include at least one active device and a portion of the second substrate.

An embodiment of the present invention further provides the ability to expand the functionality of the present invention to a multi-chip module. Dice are fixed to a substrate, for example, as described above and further described below. The gaps between the die are filled with an insulator. In an embodiment, the insulator is a rigid material, when cured, to assist in the mechanical strength of the multi-chip module. In an embodiment, terminals in the substrate are electrically connected to provide inter-chip electrical communication. This expands the functionality of them multi-chip module. In an embodiment, the dice in the multi-chip module each include an integrated circuit memory. In an embodiment, a first die includes an integrated circuit memory and a second die includes an integrated circuit. In an embodiment, the second die includes a processor. In an embodiment, the second die includes logic circuits.

An embodiment of the present invention includes fixing an active device substrate that has a plurality of dice to a base substrate. Electrical communication lines are formed between the die and respective package level terminals or pads on the base substrate. The backside of the base substrate remote from the active device substrate is removed to expose the package level

terminals. The dice are separated with its respective portion of the base substrate, which at least partially includes package level terminals. In an embodiment, a top surface of the base substrate is coated with an adhesive. In an embodiment, the removing the backside of the base substrate includes back grinding the base substrate. In an embodiment, separating the dice includes singulation, for example by laser. In an embodiment, forming electrical connections includes forming a conductive trace from a top bond pad of a die along the side of the die to contact a package level terminal. In an embodiment, the conductive trace is formed by a metal redistribution process.

An embodiment of the present invention is directed to a chip-scale-packaging method including fixing two substrates together and forming electrical contacts between active devices on the two substrates. In an embodiment, the two substrates each include a plurality of dice that contain the active integrated circuits. The dice are singulated to form discrete packages with contacts on each die and along the sides of the package. In an embodiment, fixing the two substrates together includes coating the top surface of the second substrate with an adhesive and curing the adhesive to fix the second substrate on the first substrate. In an embodiment, the first substrate is placed on the adhesive layer such that the saw streets of the first substrate align with the saw streets of the second substrate. In an embodiment, a plurality of through apertures are formed in the aligned first and second saw streets. The electrical connections from the first dice on the first substrate are formed through the through apertures to the second dice on the second substrate. In an embodiment, forming electrical connections from the first dice on the first substrate to the second dice on the second substrate includes routing a conductive trace from a first bond pad on an active device surface of the first substrate to a second bond pad on an active device surface of the second substrate through the through aperture. In an embodiment, singulating dice includes mechanically cutting the saw streets. In an embodiment, singulating dice includes lazing the saw streets. In an embodiment, cutting the saw streets includes partially cutting the electrical connection in the through apertures such that a portion of the electrical

connection in a specific through aperture remains with each of the dice adjacent the through aperture. In an embodiment, forming electrical connections includes forming metal traces including at least one metal from a group consisting essentially of copper and aluminum. In an embodiment, forming through apertures and/or cutting the saw streets include cutting a kerf in at least one of the saw streets

Embodiments of the present invention further include connecting the chip-scale package to a further substrate such as a circuit board. The chip-scale-package of an embodiment of the present invention includes contacts at the top of the die, along the side of the die and at the terminals formed in the substrate.

The present invention also includes substrates, wafers, integrated circuit packages, electrical devices, memory devices, memory units, memory modules, electrical systems, computers, which include a chip-scale- package according to the present invention.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 is a flow chart of a method according to an embodiment of the present invention.

Figure 2 is a plan view of a substrate during a method step according to the teachings of the present invention.

Figure 3 is a cross-sectional view taken generally along line 3-3 of Figure 2.

Figure 4 is a further cross-sectional view after s further method step according to the teachings of the present invention.

Figure 5 a plan view of a substrate during a method step according to the teachings of the present invention.

Figure 6 is a cross-sectional view taken generally along line 6-6 of Figure 5.

Figure 7 is an enlarged cross-sectional view taken generally along line 7-7 of Figure 5.

Figure 8 is a cross-sectional view of during a method step according to the teachings of the present invention.

Figure 9 is a cross-sectional view of during a method step according to the teachings of the present invention.

Figure 10 is a cross-sectional view of during a method step according to the teachings of the present invention.

Figure 11 is a cross-sectional view of during a method step according to a multi-chip package of the present invention.

Figure 12 is a cross-sectional view of during a method step according to the multi-chip package according to the teachings of the present invention.

Figure 13 is a cross-sectional view of an electrical system according to the teachings of the present invention.

Figure 14 is a flow chart of a method according to an embodiment of the present invention.

Figure 15 is an elevational view of an embodiment of the present invention.

Figure 16 is a fragmentary top view after a step according to an embodiment of the present invention.

Figure 17 is a fragmentary top view after a step according to an embodiment of the present invention.

Figure 18 is a cross-sectional view taken generally along line 18-18 of Figure 17.

Figure 19 is a schematic view of a die stack according to the embodiment shown in Figures 15-18.

Figure 20 is a view of a circuit module according to the teachings of the present invention.

Figure 21 is view of a memory module according to the teachings of the present invention.

Figure 22 is a view of an electronic system according to the teachings of the present invention.

Figure 23 is a view of an embodiment of an electronic system according to the teachings of the present invention.

Figure 24 is a view of a computer system according to the teachings of the present invention.

Detailed Description of the Embodiments

In the following detailed description of the embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that process, electrical or mechanical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and their equivalents.

The present description uses the relative terms "top" and "back" when referring to the substrate on which integrated circuits are formed. The term "top" herein refers to the surface on which the layers that form an active

integrated circuit structure are fabricated. The term "back" herein refers to the region of the substrate beneath the surface on which active circuit structures are fabricated.

Figure 1 shows a flowchart of a method for packaging according to an embodiment of the present invention. The method is generally directed to wafer level packaging that achieves a chip scale package. A plurality of dies are formed on a top surface of a substrate, 101. One type of a substrate is a wafer. The wafer is crystalline silicon in an embodiment. Each die includes an active integrated circuit such as a memory device, processor, logic circuits, or application specific integrated circuits. Memory devices include read only memory, dynamic random access memory, static random access memory, EEPROM, and flash memory. Additionally, the memory device could be a synchronous memory device such as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging memory technologies as known in the art. Such active devices are tested to identify and remove faulty active devices from further fabrication and to identify possible error-inducing fabrication processes, 103. The dice are singulated from each other, 105. In an embodiment, the testing occurs at the wafer level prior to singulation. The dice identified as good dice are selected and ready for further fabrication and/or packaging.

A base substrate is formed separately from the active die substrate. The base substrate is adapted to provide electrical communication terminals for the active dice in a wafer level package. The base substrate is composed of a non-conductive material. In an embodiment, the base substrate is crystalline silicon. In an embodiment, the base substrate is a wafer. Package level terminals are formed on a top surface of the base substrate, 107. Such package level terminals are patterned, discrete conductive pads. In an embodiment, the package level terminals are formed of a metal. In an embodiment, the metal is copper. In an embodiment, the metal is aluminum. If electrical communication is required

between the package level terminals, then conductive lines or traces are formed on the base substrate between the package level terminals, 109.

The top surface of the base substrate is coated with an adhesive, 111. In an embodiment, the adhesive is spin coated on the base substrate top surface. In an embodiment, the adhesive is pattern coated on the base substrate top surface. Examples of patterning the adhesive include screen printing and jet printing. The adhesive includes a polymide (PI) in an embodiment. The adhesive includes a benzocyclobutene (BCB) in an embodiment.

The singulated dice are picked and placed on the adhesive layer generally over the package level terminals, 113. The adhesive is cured to fix the dice to the base substrate. In an embodiment with the adhesive covering the package level terminals, the adhesive is removed from over at least a portion of the package level terminals. That is, the package level terminals extend outwardly from the footprint of the die. Thus, the adhesive that is not beneath the die is at least partially removed to expose a portion of the terminal.

Conductive lines are formed from the input/output pads of the dice to the package level terminals, 115. The die input/output pads are on the top surface. The conductive lines extend outwardly from the die input/output pads and down the side of the die through the adhesive layer to physically and electrically contact the package level terminals. In an embodiment, the conductive lines include castellation lines. In an embodiment, the conductive lines are formed by a redistribution layer process. The redistribution layer process includes blanket depositing a metal redistribution layer on the die and on at least the package level terminals of the base substrate. Next, a radiant sensitive film, such as a wet film resist, or a dry film resist, is blanket deposited on the redistribution layer. The radiant sensitive film is then exposed to a radiant source, e.g., a light source or laser, to the pattern of conductor lines. Development of the exposed radiant sensitive film forms a mask that can be used to etch the pattern of conductor lines. Such an etching process is known in the art as a "subtractive" process. An "additive" process could also be used where the mask is patterned and then the conductor for the redistribution layer is deposited in the spaces in the mask. The

mask and any conductive material on the mask is then removed. In an embodiment, the conductive material for the conductive lines is a metal. In an embodiment, the metal includes copper. In an embodiment, the metal includes aluminum.

In an embodiment of the present invention, a plurality of the die remain joined on the base substrate to form a multi-chip module. Such a multi-chip module increases the functionality of the individual die. For example, different types of integrated circuits are in different die in the multi-chip module such as logic circuits or processors and memory devices. The gaps between the die on the base substrate are filled with a non-conductive material, 117. This increases the mechanical strength of the multi-chip module.

The backside of the package level terminals remain covered by the backside of the base substrate. The backside of the base substrate is removed, 119, to expose the back of the package level terminals, which are connected to a die input/output pad through the conductive lines. In an embodiment, either a wet or dry etching process can be used to etch the backside of the substrate to form a thinned substrate. For thinning by wet etching, an etchant solution containing a mixture of KOH (Potassium Hydroxide) and H_2O can be utilized. A one to one solution at a temperature of about 60 degrees to 80 degrees C. will etch monocrystalline silicon at an etch rate of about 300 to 800 angtroms/min. Another wet etching process can be performed using an isotropic etch of HNO_3 and HF producing an etch rate of 55-60 μm/min. A dry etch process with an etchant such as a species of chlorine can also be utilized. In this case, the etch rate will be much slower than specified above. Alternately, thinning can be performed using chemical mechanical polishing (CMP). CMP includes a mechanical pad and a silica based slurry composition to back polish or back grind the substrate without chemical etching. The back surface of the package level terminals are now exposed.

A very thin sliver of the base substrate remains connecting the package level terminals to each other. This remaining base substrate sliver is cut to singulate the wafer level packages, 121, which include a die and a portion of the

base substrate and portions of the package level terminals. Each packaged die is singulated from the other packaged dies in an embodiment. In an embodiment, a plurality of die remain together to form a multi-chip module that is singulated from other die and/or other multi-chip modules.

In an embodiment, the singulated die or singulated multi-chip modules are attached to a further electronic base, 123. One type of electronic base is a circuit board such as a PCB. The exposed package level terminals are electrically connected to conductors, such as land patterns, on the further electronic base. In an embodiment, the singulated die or multi-chip module are fixed to a further electronic base using surface mount technology.

Figure 2 shows a plan view of an active device substrate 200. As shown the substrate 200 is a wafer, however, the present invention is not limited to only a wafer. A plurality of input/output or bond pads 202 are on the top surface of the individual die that include active devices and are formed on the substrate 200. Figure 2 shows a schematic representation of the position of pads 202 to better illustrate the present invention. It will be recognized that the bond pads 202 are typically much smaller and greater in number with respect to the substrate 200. An array of bond pads 204 define an attachment location 206 for a die. The bond pad array 204 provides the external, backside connections for an attached die. Conductive traces 208 are formed in the substrate 200 between certain bond pads 202 in an embodiment. The traces 208 provide electrical communication lines between bond pad arrays, e.g., trace 208B connecting a pad in array 204B to a pad in array 204C, trace 208C connecting a pad in array 204C to a pad in array 204D, and trace 208E connecting a pad in array 204D to a pad in array 204E. The traces 208 can also connect pads with an array, e.g., trace 208D connecting two pads together in array 204D.

Figure 3 shows a cross sectional view of substrate 200 taken generally along line 3-3 of Figure 2. A base layer 210 is provided. In an embodiment, the base layer is a bare wafer. In an embodiment, the base layer is formed of monocrystalline silicon. A plurality of conductive bond pads 202 are formed on the top surface of the substrate 210. In an embodiment, the bond pads 202

include metal. In an embodiment, the bond pads are aluminum. In an embodiment, the bond pads are copper. The bond pads 202 are separated by insulative material 211. In an embodiment, the insulative material is silicon dioxide. The top surface 212 of substrate 200 is essentially planar. In an embodiment, the top surface 212 is planarized after the bond pads 202 are formed. Planarizing the top surface 212 may include chemical-mechanical polishing.

Figure 4 shows a cross sectional view of substrate 200 after a further process step of the present invention. An adhesive layer 214 is deposited on the surface 212. The adhesive layer 214 is spin coated on substrate 200. The adhesive layer 214 covers the entire surface 212. In an embodiment, the adhesive layer includes a polymide. In an embodiment, the adhesive layer includes benzocyclobutene (BCB). In an embodiment, the adhesive layer 214 is patterned such that it covers at least the attachment locations 206 for the die. The adhesive layer 214 could be patterned by printing techniques.

Figure 5 shows a fragmentary plan view of substrate 200 after a further process step. A plurality of die 215, which include active devices such as integrated circuits, are fixed to the attachment locations 206 by adhesive layer 214 to form a dice/substrate assembly 220. Each die 215 includes a plurality of die bond pads 217 on top of the die and in electrical communication with the active devices in the die. The die bond pads 217 provide electrical contacts for the active devices and electrical circuits outside the die.

Referring now to Figures 6 and 7, Figure 6 shows a cross sectional view taken generally along line 6-6 in Figure 5. Figure 7 shows a cross sectional view taken generally along lin 7-7 of Figure 5 and with an increased scale. Figures 6 and 7 show the assembly 220 of dice 215 with the base substrate 200. The dice 215 are pressed onto the adhesive layer 214. Adhesive layer 214 is cured to fix the dice 215 to the base substrate 200. Figure 8 shows a view similar to Figure 7 after a further process step of removing the adhesive layer 214 except the portion of adhesive layer fixing the dice 215 to substrate 200. The adhesive is selectively removed from on top of portions of wafer level terminals 202 to

thereby create trenches 221 extending from the top of dice 215 to the top surface of terminals 202. Figure 9 shows a view similar to Figure 8 of assembly 220 after a further process step of forming a redistribution layer. The redistribution layer forms conductive lines 223 from the die pads 217 to the wafer level terminals 202. Figure 10 shows a view similar to Figure 9 of assembly 220 after a further process step of singulating the assembly 220 into wafer level packages 220A and 220B. This singulation step is accomplished by mechanically cutting through the insulative layer 211 and the wafer level terminals 202 that are intermediate the dice 215. In an embodiment, a saw blade is used to mechanically cut the die from each other. In an embodiment, a laser is used to mechanically cut the die from each other. In an embodiment, a laser/water jet is used mechanically cut the die from each other. An embodiment of the laser/water jet is described in U.S. patent application serial number 10/118,666, titled "WAFER DICING DEVICE AND METHOD" and having the same assignee as the present application, which application is incorporated herein by reference for any purpose. The singulated wafer level packages now have electrical contacts on the back surface, i.e., the wafer level terminals 202; on the top surface, i.e., the top portion of conductive line 223 and/or bond pad 217; and on the side surface, i.e., the conductive line 223. These singulated wafer level packages 220A and 220B could now be stacked on top of each other or contact other circuits on one, two or, three sides to improve the functionality of the active circuit within the wafer level package 220A, 220B.

Figure 11 shows an alternate embodiment of the present invention. An assembly 220 is prepared as describe above through Figure 9. After the conductive lines 223 are formed, the trenches 221 are filled with a non-conductive layer 227. Dice connected physically together by layer 227 remain together as a multi-chip module. In an embodiment, the trench filling material of layer 227 includes a polymide (PI). The trench filling material of layer 227 includes a benzocyclobutene (BCB) in an embodiment. After layer 227 is formed the backside of substrate 200 is removed (Figure 12). A wafer level package 220C is formed. It will be recognized that layer 227 covers the top

portion of dice 215 in an embodiment. In an embodiment, layer 227 only filles the trenches 221 leaving the top of conductive lines 223 and bond pads 217 exposed and available to connect to external electrical circuits.

Figure 13 shows a final assembly 230 including a wafer level package 220A of the present invention. A wafer level package 220A is mounted to an electrical system substrate 231 using surface mount technology. In an embodiment, substrate 231 is a PCB. Electrical system substrate 231 includes a plurality of land contacts 233. The plurality of land contacts 233 are covered by a conductive solder 234. Wafer level terminals 202 of wafer level package 220A are placed on the solder 234. The solder 234 is cured to mechanically and electrically connect wafer level package 220A to substrate 231. While shown and described with a single die wafer level package 220A, the same assembly is used for a multi-chip module 220C which would require additional contacts.

Figure 14 shows a flowchart of a method for packaging according to an embodiment of the present invention. Processes 101, 103, 107, 109 and 111 are the same as those described above with reference to Figure 1. The active device die are not singulated in this embodiment prior to adhering the active device substrate to the base substrate. This embodiment includes bonding the active device substrate to the base substrate. 330. An embodiment includes joining a wafer containing the active devices to a base wafer that includes the wafer level terminals and is coated with an adhesive layer. The adhesive is cured. The active device substrate is then cut to a depth at least equal to the height of the active device substrate, 332. An example of this type of partial cutting (creating kerfs) is described in U.S. patent application serial no. 10/232,226, titled "WAFER LEVEL PACKAGING", filed August 28, 2002, and incorporated by reference herein for any purpose. The active device dies are now separated by trenches. The adhesive that remains at the bottom of the trench on the base substrate and not under the die of the active device is removed to expose the wafer level terminals. Conductive lines are formed from the input/output pads of the dice to the package level terminals, 115. The die input/output pads are on the top surface. The conductive lines extend outwardly from the die input/output

pads and down the side of the die through the adhesive layer to physically and electrically contact the package level terminals. In an embodiment, the conductive lines include castellation lines. In an embodiment, the conductive lines are formed by a redistribution layer process. The package level terminals remain covered by the backside of the base substrate. The backside of the base substrate is removed, 119, to expose the back of the package level terminals, which are connected to a die input/output pad through the conductive lines. In an embodiment, either a wet or dry etching process can be used to etch the backside of the substrate to form a thinned substrate. Alternately, thinning can be performed using chemical mechanical polishing (CMP). CMP includes a mechanical pad and a silica based slurry composition to back polish or back grind the substrate without chemical etching. The back surface of the package level terminals are now exposed. Other mechanically grinding processes related to integrated circuit processes are within the scope of the present invention. The dice/base substrate is now singulated, 121. If needed the singulated dice with a portion of the base substrate is connected to a further electronic substrate, 123.

Figures 15-19 show a further embodiment of the present invention. In this embodiment, two substrates 300 each having active devices formed on an respective, active side are joined togther at the substrate level. In an embodiment, both substrates 300 are wafers and are joined together at the wafer level. Each substrate 300 includes a substrate base layer 350 on which is formed an active device layer 352. The substrate base layer 350 is monocrystalline silicon in an embodiment. The active areas 352 each include a plurality of die 315 that include the active circuits electrically connected to bond pads 317. Dice 315 are substantially similar to dice 215 described herein. Bond pads 317 are substantially similar to bond pads 217 described herein. The bond pads 317 are formed on the top of the dice 315 remote from the substrate base layer 350. Individual die are separated from each other by saw streets 355. The top and bottom substrates 300 are mirror images of each other so that corresponding die 315 in each of the top and bottom substrate 300 align with each other as well as the saw streets 355 aligning with each other. The saw streets 355 of the top

substrate would lie directly above the saw streets 355 of the bottom substrate. In joining the top substrate to the bottom substrate, the bottom substrate is flipped so that its backside 357 faces upward. The backside 357 of the bottom substrate 300 is coated with an adhesive 314. Adhesive 314 is substantially similar to adhesive 214 described herein. Backside 357 of the top substrate is brought into contact with the adhesive 314. The adhesive is cured to fix the substrates together. The saw streets 355 are vertically aligned. A plurality of through vias or apertures 360 are formed in the saw streets through both the top substrate and the bottom substrate. Vias 360 are formed by lazing the saw streets to burn through the two substrates 300 and the adhesive layer 314. In an embodiment, the laser is adapted for cutting substrate structures fabricated according to known techniques. In an embodiment, the laser is a solid state laser. In an embodiment, the laser is a yttrium-aluminum-garnet (YAG) laser. In an embodiment, the laser is a neodymium-YAG laser. The laser wavelength, in an embodiment, is about 1 micrometer. In an embodiment, the laser power is about 300 watts. In an embodiment, the laser power is less than about 300 watts. In an embodiment, the laser power is greater than about 100 watts. In an embodiment, the laser refresh rate is about 3,000 Hz. In an embodiment, the laser refresh rate is less than about 3,000 Hz. In an embodiment, the laser refresh rate is greater than 1,000 Hz. In an embodiment, the laser is an excimer laser. The laser is desirable for use in scribing or cutting the workpiece (here, the stacked substrates 300) as the laser does not apply mechanical stress onto the workpiece. A plurality of conductive lines 323 are formed from the top die bond pads 317 to the edge of the die and through a respective via 360 to the bottom die bond pads 317 (Figures 17 and 18). The conductive lines 323 are formed by a redistribution layer process as described herein. Conductive lines 323 are substantially similar to conductive lines 232. Now the vertically aligned dice that are joined by the adhesive are electrically connected togther through a conductive line 323. The individual joined die assembly 365 can now be singulated. Singulated die assembly 365 are schematically shown in Figure 19 with the conductive line 323

remaining in part of via 360 after cutting the adjacent die assemblies apart during singulation.

Circuit Modules

As shown in Figure 20, two or more substrate level packaged dice 2001 of the present invention may be combined, with or without protective casing, into a circuit module 2000 to enhance or extend the functionality of an individual die 2001. Circuit module 2000 may be a combination of dies 2001 representing a variety of functions, or a combination of dies 2001 containing the same functionality. In an embodiment, circuit module 2000 includes at least one socket, slot, recess or the like 2052 into which the die 2001 is received. One or more dies 2001 of circuit module 2000 include I/O structures in accordance with the invention and/or are fabricated in accordance with the present invention. In an embodiment, dies 2001 are inserted into a slot 2052 in a circuit board 2050 such that the package level terminals 202 or conductive traces 323 are in electrical communication with the contacts in the slot 2052. In an embodiment, package level terminals 202 or conductive traces 323 are in physical contact with contacts in the slot 2052. In an embodiment, the contacts package level terminals 202 or conductive traces 323 are press fit into the slot 2052 against the contacts of the slot.

Numeral 2052 in Figure 20, in another embodiment, represents a mount including land patterns whereat the contacts according to the present invention are mounted. The mounting process includes an SMT process. For example, circuit module 2000 is a printed circuit board having land patterns on which solder paste is applied, e.g., by printing the solder paste. A substrate level packaged die 2001 of the present invention is picked and placed at the mount with the package level terminals 202 or conductive traces 323 aligned with the paste covered contacts of the mount. Either the package level terminals 202 or conductive traces 323 or the mount contacts are reflowed to create a physical and electrical connection.

Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules, and may include multilayer, multichip modules. Such modules will have a chip receiver in which a chip according to the present invention is inserted. Circuit module 2000 may be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft and others. Such modules will have a circuit module receiver in which a circuit module according to the present invention is inserted. Circuit module 2000 will have a variety of leads 2005_1 through 2005_N extending therefrom and coupled to the package level terminals 202 or conductive traces 323 of substrate level packaged dice 2001 providing unilateral or bilateral communication and control.

Figure 21 shows one embodiment of a circuit module as memory module 2100. Memory module 2100 contains multiple memory devices 2101 contained on support 2161. In an embodiment, support 2161 includes slots 2152 for receiving memory devices 2101 as described herein. The number of memory devices generally depends upon the desired bus width and the desire for parity. Memory devices 2101 include at least die in accordance with to the present invention. The support 2161 includes sockets, slots, recesses or the like 2152, each adapted to receive a memory device 2101 and provide electrical communication between a bus and memory device 2101. Memory module 2100 accepts a command signal from an external controller (not shown) on a command link 2163 and provides for data input and data output on data links 2165. The command link 2163 and data links 2165 are connected to leads 2167 extending from the support 2161. Leads 2167 are shown for conceptual purposes and are not limited to the positions shown in Figure 21.

Electronic Systems

Figure 22 shows an embodiment of an electronic system 2200 containing one or more circuit modules 2000. At least one of the circuit modules 2000 contains a die in accordance with the present invention. Electronic system 2200

generally contains a user interface 2269. User interface 2269 provides a user of the electronic system 2200 with some form of control or observation of the results of the electronic system 2200. Some examples of user interface 2269 include the keyboard, pointing device, monitor or printer of a personal computer; the tuning dial, display or speakers of a radio; the ignition switch, gauges or gas pedal of an automobile; and the card reader, keypad, display or currency dispenser of an automated teller machine. User interface 2269 may further describe access ports provided to electronic system 2200. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules 2000 may be a processor providing some form of manipulation, control or direction of inputs from or outputs to user interface 2269, or of other information either preprogrammed into, or otherwise provided to, electronic system 2200. In an embodiment, electronic system 2200 includes memory modules 2100. As will be apparent from the lists of examples previously given, electronic system 2200 will often be associated with certain mechanical components (not shown) in addition to circuit modules 2000 and user interface 2269. It will be appreciated that the one or more circuit modules 2000 in electronic system 2200 can be replaced by a single integrated circuit. Furthermore, electronic system 2200 may be a subcomponent of a larger electronic system.

Figure 23 shows one embodiment of an electronic system as memory system 2300. Memory system 2300 contains one or more memory modules 2100 and a memory controller 2370. At least one of the memory modules 2100 includes a die in accordance with the present invention. Memory controller 2370 provides and controls a bidirectional interface between memory system 2300 and an external system bus 2372. Memory system 2300 accepts a command signal from the external bus 2372 and relays it to the one or more memory modules 2100 on a command link 2374. Memory system 2300 provides for data input and data output between the one or more memory modules 2100 and external system bus 2372 on data links 2376.

Figure 24 shows a further embodiment of an electronic system as a computer system 2400. Computer system 2400 contains a processor 2401 and a memory system 2300 housed in a computer unit 2480. In an embodiment, the memory system 2300 includes a die in accordance with the present invention. In an embodiment, processor 2401 includes a die in accordance with the present invention. In an embodiment, the memory system and processor dies are combined according to the present invention. Computer system 2400 is but one example of an electronic system containing another electronic system, i.e., memory system 2300, as a subcomponent. Computer system 2400 optionally contains user interface components. Depicted in Figure 11 are a keyboard 2481, a pointing device 2483 such as a mouse, trackball, or joystick, a monitor 2485, a printer 2487 and a bulk storage device 2489. It will be appreciated that other components are often associated with computer system 2400 such as modems, device driver cards, additional storage devices, etc. These other components, in an embodiment, include a die in accordance with the present invention. It will further be appreciated that the processor 2401 and memory system 2300 of computer system 2400 can be incorporated on a single integrated circuit. Such single package processing units reduce the communication time between the processor and the memory circuit.

Conclusion

It is desired to reduce the size of packaged components. This results in packaging material savings and increases throughput by reducing packaging fabrication times. Moreover, with the growing popularity of smaller electronic device the electronic components must be as small as possible. The present invention further provides methods for producing a packaged die. In an embodiment, dice are fixed on a base substrate that has contacts or terminals formed thereon. The dice are electrically connected to the terminals. For example, top level I/O pads of the dice are connected to the terminals by conductive traces running from the top of the dice along its side to the terminals below the dice. The backside of the base substrate is removed to expose the

backside of the terminals thereby forming a true chip-size package. The die can now be singulated. This process can be performed at the wafer foundry thereby increasing fabrication throughput. Wafer foundries have fabrication and substrate handling equipment to facilitate the present process.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. For example, other integrated circuit processing equipment may be utilized in conjunction with the invention. For another example, other integrated circuit fabrication processes are adapted to produce the dies and chips according to the present invention. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

The invention claimed is:

1. A method, comprising:

providing a die;

providing a substrate having electrical signal terminals thereon;

fixing the die on the substrate;

forming electrical connections from die to the terminals; and

removing a backside of substrate to expose the terminals.

2. The method of claim 1, wherein providing a die includes providing a die including an integrated circuit memory device.

3. The method of claim 1, wherein fixing the die on the substrate includes applying adhesive to a top surface of the substrate, placing the die on the adhesive, and curing the adhesive to fix the die on the substrate top surface.

4. The method of claim 1, wherein providing the die includes providing a die having I/O pads on a top surface of the die.

5. A method, comprising:

forming active devices on a first substrate;

singulating the active devices;

forming electrical terminals on a second substrate;

coating the second substrate with an adhesive;

placing a plurality of active devices on the adhesive;

curing the adhesive;

electrically connecting the active devices to respective electrical terminals;

removing a backside of the second substrate to expose a backside of the electrical terminals; and

singulating the second substrate to form individual chip scale packages that include at least one active device and a portion of the second substrate.

6. The method of claim 5, wherein forming electrical terminals includes patterning a conductive layer on a top surface of the second substrate.

7. The method of claim 6, wherein patterning the conductive layer includes patterning a metal layer.

8. The method of claim 6, wherein forming electrical terminals includes planarizing the top surface of the second substrate.

9. The method of claim 6, wherein removing a backside of the second substrate includes backgrinding the second substrate.

10. The method of claim 9, wherein electrically connecting the active devices to respective electrical terminals includes routing a metal trace from a bond pad on top of the active device to the electrical terminal below the active device.

11. The method of claim 10, wherein routing the metal trace includes routing the metal trace to an electrical terminal at least partially beneath the active device.

12. The method of claim 5, wherein electrically connecting the active devices to respective electrical terminals includes filling gaps between the active devices with a non-conductive material.

13. The method of claim 12, wherein singulating the second substrate includes cutting through non-conductive material in the gaps between the active devices.

14. A method, comprising:

providing a substrate having electrical signal terminals thereon;

placing adhesive on a top surface of the substrate;

placing a die having top surface bond pads on adhesive to fix the die to the substrate;

forming castellation electrical connections from top surface bond pads to the substrate terminals; and

removing a backside of substrate to expose terminals.

15. The method of claim 14, wherein removing the backside of the substrate includes backgrinding the substrate.

16. The method of claim 14, wherein removing the backside of the substrate includes etching the back surface of the substrate.

17. The method of claim 14, wherein forming castellation electrical connections includes removing adhesive uncovered by a die from the top surface of the substrate and forming a trace from the top surface bond pads along the sides of the die to contact the substrate electrical signal terminal.

18. The method of claim 17, wherein forming the trace includes using metal redistribution to join the top surface bond pad and the substrate electrical signal terminal.

19. A method, comprising:

fixing a plurality of dice on a substrate over a plurality of package I/O terminals;

forming electrical connections from die bond pads to the package I/O terminals; and

removing a backside of the substrate to expose the package I/O terminals.

20. The method of claim 19, wherein forming electrical connections includes forming electrical connections between some of the package I/O terminals.

21. The method of claim 20, wherein forming electrical connections between some of the package I/O terminals includes interconnecting at least a first of the plurality of dice to at least a second of the plurality of dice.

22. The method of claim 21, wherein interconnecting includes interconnecting the first die that has a processor to the second die that has a memory.

23. The method of claim 22, wherein removing the backside includes singulating the first and second die from a remainder of the substrate to form a multi-chip module.

24. A method, comprising:

fixing a plurality of dice on a substrate over a plurality of package terminals such that adjacent die overlie common package terminals;

electrically connecting I/O pads of the dice to the plurality of package terminals;

removing a backside of the substrate to expose the plurality of package terminals; and

singulating the plurality of dice with a portion of the substrate directly beneath each die to form a chip scale package.

25. The method of claim 24, wherein singulating includes cutting through the common package terminals such that a first portion remains with a first of the plurality of dice and a second portion remains with a second of the plurality of die.

26. A method, comprising:

providing a sensor die having a sensing device and an I/O pad at a top surface;

providing a substrate having electrical signal terminals thereon;

fixing the die on the substrate;

forming electrical connections from the I/O pad of the die to the substrate terminals; and

removing a backside of substrate to expose the terminals.

27. The method of claim 26, wherein providing the sensor die includes providing a sensor die with an optical sensor in electrical communication with the I/O pad.

27. The method of claim 26, wherein fixing the die includes applying adhesive over the substrate, and curing the adhesive.

28. The method of claim 26, wherein forming electrical connections includes forming an aperture through the adhesive to the electrical signal terminals, and forming a conductive trace from the I/O pad down the side of the die to the electrical signal terminal of the substrate.

29. The method of claim 28, wherein removing the backside of the substrate includes singulating the die from the remainder of the substrate.

30. A method, comprising:

providing a die;

providing a substrate having electrical signal terminals thereon;

applying adhesive to a top surface of the substrate;

positioning the die on the adhesive at least partially over a first group of the electrical signal terminals;

curing the adhesive to fix the die to the substrate;

forming a via through the adhesive to the first group of electrical signal terminals;

forming electrical connections from die through the via to substrate terminals; and

removing a backside of substrate to expose a backside of the terminals.

31. The method of claim 30, wherein applying adhesive includes applying a polymide material on the top surface of the substrate.

32. The method of claim 30, wherein forming electrical connections includes forming a metal trace from I/O pads on a top surface of the die down the side of the die to the substrate terminals.

33. The method of claim 32, wherein forming the metal trace includes forming a metal trace from one of a group including copper and aluminum.

34. A chip-scale-packaging method, comprising:

singulating dice from a first wafer;

testing the singulated dice;

forming final I/O locations on a second wafer;

applying adhesive to a top surface of the second wafer;

placing a singulated die on the adhesive over the final I/O locations;

removing a back surface of the second wafer to expose the final I/O locations; and

connecting the singulated die to an electric circuit through the final I/O location.

35. The chip-scale-packaging method of claim 34, wherein removing the backside of the second wafer includes backgrinding the second wafer.

36. The chip-scale-packaging method of claim 34, wherein removing the backside of the second wafer includes etching the back surface of the second wafer.

37. The chip-scale-packaging method of claim 34, wherein removing the back surface of the second wafer includes separating the singulated die and a portion of the second wafer from a remainder of the second wafer.

39. A method, comprising:

providing a plurality of integrated circuit dice;

providing a substrate having electrical signal terminals thereon with at least two of the electrical signal terminals being interconnected;

fixing a first die on the substrate over a first group of the electrical signal terminals;

fixing a second die on the substrate over a second group of the electrical signal terminals;

forming electrical connections from first die to first group of electrical signal terminals;

forming electrical connections from second die to second group of electrical signal terminals;

removing a backside of substrate to expose the terminals; and

separating the first and second die from a remainder of the substrate with the first and second die being adapted to electrically communicate through at least the interconnected electrical signal terminals.

40. The method of claim 39, wherein separating the first and second die includes filling the gap between the first die and the second die with an insulative material.

41. The method of claim 40, wherein filling the gap includes filling the gap with an encapsulant.

42. The method of claim 40, wherein filling the gap includes filling the gap with a benzocyclobutene material.

43. The method of claim 40, wherein separating the first and second die includes forming a memory module.

44. A chip-scale-packaging method, comprising:

providing a first substrate having a plurality of dice;

providing a second substrate having a plurality of package level terminals on a top surface;

coating the top surface of the second substrate with an adhesive;

curing the adhesive to fix the second substrate on the first substrate;

forming electrical connections from dice on the first substrate to the package level terminals; and

removing a backside of second substrate to expose the backside of the package level terminals.

45. The method of claim 44, wherein removing the backside of the second substrate includes singulating the plurality of dice into chip-level-packages.

46. The method of claim 45, wherein singulating includes lazing the second substrate intermediate adjacent dice.

47. The method of claim 46, wherein lazing includes water jetting the second substrate.

48. The method of claim 45, wherein forming electrical connections includes forming a conductive trace from a top bond pad of a die along the side of the die to contact a package level terminal.

49. The method of claim 48, wherein forming the conductive trace includes forming a redistribution layer on the plurality of dice.

50. The method of claim 48, wherein forming the conductive trace includes forming a copper conductor from the top bond pad to the package level terminal.

51. The method of claim 48, wherein forming electrical connections includes removing the adhesive from in between adjacent dice to partially expose the package level terminals and thereafter forming the conductive trace.

52. A method, comprising:

providing a first substrate with a plurality of first dice separated by first saw streets;

providing a second substrate with a plurality of second dice separated by second saw streets;

applying an adhesive to a backside of the second substrate;

placing the first substrate on the adhesive such that the first saw streets align with the second saw streets;

curing the adhesive to fix the first substrate to the second substrate;

forming a plurality of through apertures in the aligned first and second saw streets;

forming electrical connections from the first dice on the first substrate to the second dice on the second substrate; and

singulating aligned first and second dice from a remainder of the fixed first and second substrates.

53. The method of claim 52, wherein forming electrical connections from the first dice on the first substrate to the second dice on the second substrate includes routing a conductive trace from a first bond pad on an active device surface of the first substrate to a second bond pad on an active device surface of the second substrate through the through aperture.

54. The method of claim 52, wherein placing the first substrate on the adhesive includes placing a backside of the first substrate on the adhesive.

55. The method of claim 52, wherein forming electrical connections includes forming metal traces.

56. The method of claim 55, wherein forming metal traces includes forming a copper trace.

57. The method of claim 55, wherein forming metal traces includes forming an aluminum trace.

58. The method of claim 52, wherein singulating includes mechanically cutting the saw streets.

59. The method of claim 52, wherein mechanically cutting the saw streets includes partially cutting the electrical connection in the through apertures such that a portion of the electrical connection in a specific through aperture remains with each of the dice adjacent the through aperture.

60. A method, comprising:

providing a first substrate with a plurality of first dice separated by first saw streets;

providing a second substrate with a plurality of second dice separated by second saw streets;

applying an adhesive to a backside of the second substrate;

placing the first substrate on the adhesive such that the first saw streets align with the second saw streets;

curing the adhesive to fix the first substrate to the second substrate;

lazing the first saw street, the adhesive layer and the second saw street to form through holes;

forming electrical connections from the first dice on the first substrate to the second dice on the second substrate through the through holes; and

singulating aligned first and second dice from a remainder of the fixed first and second substrates.

61. The method of claim 60, wherein forming electrical connections includes forming metal traces including at least one metal from a group consisting essentially of copper and aluminum.

62. The method of claim 60, wherein lazing the first substrate, adhesive and second substrate includes excimer lazing the first substrate, the adhesive and the second substrate.

63. A method, comprising:

providing a first substrate with a plurality of first dice separated by first saw streets;

providing a second substrate with a plurality of second dice separated by second saw streets;

applying an adhesive to a backside of the second substrate;

placing the first substrate on the adhesive such that the first saw streets align with the second saw streets;

curing the adhesive to fix the first substrate to the second substrate;

cutting a kerf in the first saw streets of the first substrate through the first substrate;

removing the adhesive intermediate the plurality of first dice;

lazing the second saw street to form through holes;

forming electrical connections from the first dice on the first substrate to the second dice on the second substrate through the through holes; and

singulating aligned first and second dice from a remainder of the fixed first and second substrates.

64. The method of 63, wherein removing the adhesive intermediate the plurality of first dice includes chemically etching the adhesive.

65. The method of claim 63, wherein forming electrical connections includes forming a metal trace from a top surface bond pad of the first die to a top surface bond pad of the second die through the through hole.

66. The method of claim 63, wherein singulating the aligned first and second die includes mechanically cutting the aligned first and second saw streets.

67. The method of claim 66, wherein singulating the aligned fist and second die includes exposing the electrical connection along the side of the fixed first and second substrates.

68. A method of forming an integrated circuit (IC) package component, comprising:

fabricating a non-conductive base substrate having electrical conductors vertically extending from a top surface of the base substrate into the substrate and terminating within the base substrate, the top surface of the base substrate includes an interconnect area sized to receive an IC die; and

removing a portion of a bottom surface of the base substrate to expose the electrical conductors such that the electrical conductors are exposed on both the top and bottom surfaces of the base substrate.

69. The method of claim 68, further comprising:

attaching the IC die to the top surface of the base substrate; and

electrically connecting the IC die to the electrical conductors.

70. The method of claim 68, wherein removing the portion of the bottom surface of the base substrate is performed by either an etching operation or abrasive removal operation.