

## NOISE REDUCTION SCHEME FOR OPERATIONAL AMPLIFIERS

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## BACKGROUND OF THE INVENTION

The present invention relates to the use of operational amplifiers (op amps) in differential signal architectures. More specifically, the present invention provides techniques by which the performance of op amps which generate differential signals may be enhanced.

In analog integrated circuits, electrical signals are often processed in differential form, i.e., each signal has a paired counterpart of equal amplitude and opposite phase. Differential architectures are employed for a number of reasons including, for example, the fact that differential architectures exhibit significantly better power supply noise rejection than single-ended designs. Op amps are among the most common circuit components in differential systems. Fig. 1 shows an op amp circuit which is commonly employed in differential designs.

Fig. 1 shows a circuit 100 for converting an incoming single-ended signal  $V_{in}$  to a differential signal represented by  $V+$  and  $V-$ . Such circuits are common where, for example, an integrated circuit with a differential architecture is embedded in a larger system where it must interface with single-ended signals. The conversion from a single-ended to a differential signal involves using a first op amp 1 as an input buffer and a second op amp 2 to create a phase-inverted counterpart of  $V_{in}$ . Both the original in-phase signal ( $V-$ ) and the phase-inverted version ( $V+$ ) are then fed to subsequent differential circuitry (e.g., op amp 3). The buffering provided by op amp

1 provides a low impedance signal to subsequent circuits. While this is desirable, it does not come without a cost. That is, the addition of a stage of amplification adds noise, distortion, offset, and possibly other undesirable effects.

As shown in Fig. 1 with reference to op amp 1 and assumed for the op amps in each of the figures described herein, the noise voltage associated with each op amp is modeled as an input referred noise voltage source  $V_n$ . The input-referred noise sources for specific op amps will be identified by a reference number subscript. That is, the noise source for op amp 1 is denoted  $V_{n1}$ . The noise values are given in squared noise voltage, e.g.,  $V_{n1}^2$ . As will be understood and assuming the noise sources are uncorrelated, a weighted sum of these noise voltages is calculated as the square root of the sum of the squares. As will also be understood, the input gain is set by the ratio of resistor value  $R_2$  to resistor value  $R_1$ . Resistor values for  $R_3$  and  $R_4$  are equal in value to ensure that  $V_+$  is equal in amplitude to  $V_-$  as well as being opposite in phase. Op amp 3 and resistors  $R_5 - R_8$  are shown as representative of differential circuitry which might follow the single-ended to differential conversion, but will not be further discussed here. The key parameter of interest is the noise voltage presented to the equivalent input of the differential circuitry, i.e.,  $V_{diff} = (V_+ - V_-)$ .

The expression for the noise voltage at  $V_-$  is:

$$V_n^2(V_-) = V_{n1}^2(1 + R_2/R_1) \quad (1)$$

The expression for the noise voltage at  $V_+$  is:

$$V_n^2(V_+) = V_{n2}^2(1 + R_4/R_3) - V_{n1}^2(1 + R_2/R_1)(R_4/R_3) \quad (2)$$

Since  $R3 = R4$ :

$$V_n^2(V+) = 2V_{n2}^2 - V_{n1}^2(1 + R2/R1) \quad (3)$$

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Then the noise presented at the input to op amp 3 may be represented as follows:

$$V_{ndiff}^2 = V_n^2(V+) - V_n^2(V-) \quad (4)$$

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$$= 2V_{n2}^2 - V_{n1}^2(1 + R2/R1) - V_{n1}^2(1 + R2/R1) \quad (5)$$

$$= 2V_{n2}^2 - 2V_{n1}^2(1 + R2/R1) \quad (6)$$

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It can be seen that the noise voltage of the input buffering amplifier,  $V_{n1}^2$ , is amplified by the non-inverting gain configuration of op amp 1, and applied to the V- input of the differential circuitry. This same amplifier noise voltage is also phase-inverted and applied to the V+ input of the differential circuitry. Thus,  $V_{n1}^2$  is effectively amplified by both op amp 1 and op amp 2. This then calls for a particularly low-noise op amp in the op amp 1 position in order to minimize its noise contribution. As will be understood, low-noise op amps are expensive both in terms of money and silicon.

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It is therefore desirable to provide techniques by which the noise performance of op amps in differential architectures may be improved.

## SUMMARY OF THE INVENTION

According to the present invention, a technique is provided by which the performance of operational amplifiers (op amps) in differential architectures is significantly improved. According to the various embodiments described, first and second op amps are configured to generate a differential signal, the first op amp generating one end of the differential signal and the second op amp generating the other. The op amps may be configured to receive a single-ended signal and convert it to a differential signal. Depending upon the single-ended to differential application, the op amps may be configured in either an inverting or noninverting configuration.

The op amps may also be configured in a "pseudo" differential arrangement in which each receives half of a differential signal and buffers and/or amplifies it to generate a differential output signal. In each configuration, the inverting input of one of the op amps coupled to the noninverting input of the other. That is, instead of biasing the noninverting input of the second op amp to ground or a constant bias voltage, it is tied to the signal input of its companion device. According to a specific embodiment, a number of switches are provided which effect the various configurations of the two op amps depending upon the application.

As will be described in detail below, the effect of this configuration is that a significant component of the input referred noise of the first op amp is presented as a common mode signal on the differential output, this component thus being eliminated by downstream devices, e.g., other op amps, which presumably have excellent common mode rejection. In fact, noise improvement is not the only advantage gained by the present invention. That is, as will be discussed, the deleterious effects of any anomalous op amp behavior which may be modeled as an input referred voltage source, e.g., distortion, is likewise diminished by the technique described herein.

Thus, the present invention provides methods and apparatus for generating a differential signal. The output of a first operational amplifier corresponds to one end of the differential signal. The output of a second operational amplifier corresponds to the other end of the differential signal. The inverting input of the first operational  
5 amplifier is coupled to the noninverting input of the second operational amplifier.

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified schematic of circuit for converting a single-ended signal into a differential signal:

Fig. 2 is a simplified schematic of a specific embodiment of the present invention:

Fig. 3 is a simplified schematic of a circuit for buffering and/or amplifying a differential signal:

Fig. 4 is a simplified schematic of another specific embodiment of the present invention: and

Fig. 5 is a detailed schematic of yet another specific embodiment of the present invention.

## DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Fig. 2 is a simplified schematic of a circuit 200 for converting a single-ended signal to a differential signal designed according to a specific embodiment of the present invention. Instead of grounding the noninverting input of op amp 2' as shown in Fig. 1, the noninverting input of op amp 2' is instead connected to the inverting input of op amp 1'.

Calculating the circuit noise for this configuration, we have:

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$$V_n^2(V_-) = V_{n1}^2(1 + R2'/R1') \quad (7)$$

As can be seen this term remains unchanged from the circuit shown in Fig. 1 (see equation (1)). However,

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$$V_n^2(V+) = V_{n2}^2(1 + R4'/R3') - V_{n1}^2(1 + R2'/R1')(R4'/R3') + V_{n1}^2(1 + R4'/R3') \quad (8)$$

and because  $R3 = R4$ :

$$V_n^2(V+) = 2V_{n2}^2 - V_{n1}^2(1 + R2'/R1') + 2V_{n1}^2 \quad (9)$$

$$V_{ndiff}^2 = V_n^2(V+) - V_n^2(V-) \quad (10)$$

$$= 2V_{n2}^2 - V_{n1}^2(1 + R2'/R1') + 2V_{n1}^2 - V_{n1}^2(1 + R2'/R1') \quad (11)$$

$$= 2V_{n2}^2 - 2V_{n1}^2(1 + R2'/R1') + 2V_{n1}^2 \quad (12)$$

$$= 2V_{n2}^2 - 2V_{n1}^2(R2'/R1') \quad (13)$$

As can be seen,  $V_{ndiff}^2$  for circuit 200 is less than  $V_{ndiff}^2$  for circuit 100 by one  $2V_{n1}^2$  term. Moreover, as the ratio of  $R2'/R1'$  becomes small, the remainder of the noise contribution due to  $V_{n1}$ , i.e., the input referred noise of the op amp 1', also becomes small and, in fact, depending on the system, can become negligible with respect to the contributions of  $V_{n2}$ . For example, if  $V_{in}$  were driven by a conventional +15V/-15V audio op amp design and the circuitry of Fig. 2 was +5V circuitry, the  $R2'/R1'$  ratio would need to be small to bring the large 30Vpp signal within the 5Vpp constraints. In such a system,  $R2'/R1'$  would approximately equal 1/6 and the residual noise contribution of op amp 1' would be quite small.

A further advantage of this configuration can be seen when the input-referred noise voltage source  $V_{n1}$  is replaced by any other anomalous behavior which could be modeled as an input-referred voltage source such as, for example, offset or distortion. With such a substitution, the above analysis would still hold true, and the deleterious effects of these other anomalies in op amp 1' would be likewise diminished. This could be used to substantial advantage by the circuit designer in that the noise, distortion, offset, etc., requirements of op amp 1' could be relaxed with the use of this invention, allowing for the substitution of a smaller, cheaper, lower power op amp without compromising overall system performance. Alternatively, the invention could be used with no relaxation in the performance requirements on op amp 1' in order to enhance overall system performance essentially for free.

Another embodiment of the present invention will now be described with reference to Figs. 3 and 4. Fig. 3 shows a circuit 300 for buffering and/or amplifying an existing differential signal represented by  $V_{in+}$  and  $V_{in-}$ . The input signal passes through two separate amplifiers, op amp 4 and op amp 5, which are configured to have gains of  $-R_{12}/R_{11}$  and  $-R_{14}/R_{13}$ , respectively. Their outputs together constitute the amplified differential signal which is passed to a generic differential amplifier block 202 representing any generalized differential receiving circuitry.

In this case, the noise contributions of the two amplifiers, op amps 4 and 5, are:

$$V_n^2(V_-) = V_{n4}^2(1 + R_{12}/R_{11}) \quad (14)$$

$$V_n^2(V_+) = V_{n5}^2(1 + R_{14}/R_{13}) \quad (15)$$

$$V_{ndiff}^2 = V_n^2(V+) - V_n^2(V-) = V_{n5}^2(1 + R14/R13) - V_{n4}^2(1 + R12/R11) \quad (16)$$

As with circuit 100 of Fig. 1, there are significant noise contributions from both op amps 4 and 5.

Fig. 4 is a simplified schematic of a circuit 400 for buffering and/or amplifying an existing differential signal according to another specific embodiment of the present invention. Instead of connecting the noninverting input terminal of op amp 5' to ground as shown in Fig. 3, it is instead connected to the inverting input of op amp 4'. The noise summary for the configuration of Figure 4 is as follows:

$$V_n^2(V-) = V_{n4'}^2(1 + R12'/R11') \quad (17)$$

As can be seen this term remains unchanged from the circuit shown in Fig. 3 (see equation (14)). However,

$$V_n^2(V+) = V_{n5'}^2(1 + R14'/R13') + V_{n4'}^2(1 + R13'/R14') \quad (18)$$

$$\begin{aligned} V_{ndiff}^2 &= V_n^2(V+) - V_n^2(V-) \\ &= V_{n5'}^2(1 + R14'/R13') \\ &\quad + V_{n4'}^2(1 + R13'/R14') - V_{n4'}^2(1 + R12'/R11') \end{aligned} \quad (19)$$

For true differential symmetry,  $R14'/R13' = R12'/R11'$ , and thus:

$$V_{ndiff}^2 = V_n^2(V+) - V_n^2(V-) = V_{n5'}^2(1 + R14'/R13') \quad (20)$$

It can be seen that the reconfiguration has caused the noise contribution of op amp 4' to vanish. If  $V_{n4}^2$  and  $V_{n5}^2$  are uncorrelated, this constitutes a 3dB reduction in noise contribution from this (pseudo) differential amplification stage. Additionally, as in the case above with the single-ended to differential conversion circuitry, any non-ideality in Opamp1 which can be modeled as an input-referred voltage source will likewise vanish.

Fig. 5 is a detailed schematic of yet another specific embodiment of the present invention. Circuit 500 employs left hand and right hand op amps 502 and 504 which may be configured such that circuit 500 operates in three modes. The three modes are: (1) pseudo-differential amplification; (2) non-inverting single-ended to differential conversion; and (3) inverting single-ended to differential conversion.

In normal operation, the MUTE input port is at a logic-0 and the CAL\_ONB input port is at a logic-1. The "compress\_in" input port is not material to the invention and should be assumed to be at 0V. The circuit elements designated "spltmux2\_esd" are cmos transmission gates. Their V, G, and S terminals can be ignored for small signal analysis purposes, and their "ent1" input causes conduction between ports "t1" and "t0" when at a logic-1 and opens the path between ports "t1" and "t0" when at a logic-0. VCM is a common mode bias voltage, in this case 2.4V. INP is the non-inverting input of each op amp, INM is the inverting input of each op amp, and OUTP is the output terminal of each op amp. All other terminals on the op amps can be ignored for small signal analysis. Both op amps are shown as having two sections, though this is not material to this invention. The circuit elements designated "fb\_resbank" are banks of 12 feedback resistors which range from 10.62k to 20k with values selected to yield gain control in 0.5dB steps. The particular feedback resistor configuration used here is not critical to the invention, though,

according to a specific embodiment of the invention, the feedback resistance for both op amps remain equal, i.e., track together. Note that some connectivity is established via labels, e.g., INM1 and INM2 "jump" between points in the figure.

The circuit is operated as shown in Table 1.

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| en_P<br>Positive input<br>control | en_M<br>Negative<br>input control | INP<br>Positive input | INM<br>Negative input | Function/comment<br>s                                         | Noise cancellation                                                                                                |
|-----------------------------------|-----------------------------------|-----------------------|-----------------------|---------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|
| Logic 1                           | Logic 1                           | positive input        | Negative input        | pseudo-differential<br>operation                              | Positive input of<br>right op amp fed<br>from negative<br>input of left op<br>amp; left op amp<br>noise canceled  |
| Logic 1                           | Logic 0                           | positive input        | Ignored               | noninverting<br>single-ended to<br>differential<br>conversion | Positive input of<br>right op amp fed<br>from negative<br>input of left op<br>amp; left op amp<br>noise canceled  |
| Logic 0                           | Logic 1                           | ignored               | Negative input        | inverting single-<br>ended to<br>differential<br>conversion   | Positive input of<br>left op amp fed<br>from negative<br>input of right op<br>amp; right op amp<br>noise canceled |
| Logic 0                           | Logic 0                           | ignored               | Ignored               | disallowed<br>condition                                       | Disallowed<br>condition                                                                                           |

Table 1

While the invention has been particularly shown and described with reference to specific embodiments thereof, it will be understood by those skilled in the art that changes in the form and details of the disclosed embodiments may be made without departing from the spirit or scope of the invention. For example, the various  
 10 embodiments of the present invention may be implemented using discrete components, or as an integrated circuit using conventional semiconductor fabrication techniques. Moreover, an integrated circuit implementation of the present invention may employ any appropriate technology such as, for example, CMOS technology. In  
 15 addition, the connections between the operational amplifiers of the present invention

may be permanently hardwired, or programmable as described above with reference to Fig. 5. Therefore, the scope of the invention should be determined with reference to the appended claims.

WHAT IS CLAIMED IS:

1. A circuit for generating a differential signal, comprising:  
a first operational amplifier, the output of the first operational amplifier  
5 corresponding to one end of the differential signal; and  
a second operational amplifier, the output of the second operational amplifier  
corresponding to the other end of the differential signal;  
wherein the inverting input of one of the first and second operational  
amplifiers is coupled to the noninverting input of the other of the first and second  
10 operational amplifiers.
2. The circuit of claim 1 wherein the first and second operational  
amplifiers are configured to receive a single-ended input signal and generate the  
differential signal.  
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3. The circuit of claim 2 wherein the first and second operational  
amplifiers are configured as an inverting circuit.
4. The circuit of claim 2 wherein the first and second operational  
20 amplifiers are configured as a noninverting circuit.
5. The circuit of claim 1 wherein the first and second operational  
amplifiers are configured to receive a differential input signal and generate the  
differential signal.  
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6. The circuit of claim 1 further comprising a plurality of switches for configuring the first and second operational amplifiers into a plurality of configurations.

5 7. The circuit of claim 6 wherein the plurality of configurations includes a first configuration in which the first and second operational amplifiers are configured to receive a single-ended input signal and generate the differential signal.

8. The circuit of claim 7 wherein the first and second operational  
10 amplifiers are configured as an inverting circuit in the first configuration.

9. The circuit of claim 7 wherein the first and second operational amplifiers are configured as a noninverting circuit in the first configuration.

15 10. The circuit of claim 6 wherein the plurality of configurations includes a first configuration in which the first and second operational amplifiers are configured to receive a differential input signal and generate the differential signal.

11. The circuit of claim 6 wherein the plurality of switches are controlled  
20 by switch control logic circuitry coupled to first and second logic inputs.

12. The circuit of claim 11 wherein the switch the switch control logic circuitry corresponds to a truth table, the truth table being as follows:



| First logic input | second logic input | op amp connections                                                                                                                                                                                                                                                                    |
|-------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                 | 1                  | the noninverting input of the second operational amplifier is coupled to the inverting input of the first operational amplifier; the first and second operational amplifiers are configured to receive a differential input signal and generate the differential signal               |
| 1                 | 0                  | the noninverting input of the second operational amplifier is coupled to the inverting input of the first operational amplifier; the first and second operational amplifiers are configured to receive a single-ended signal and generate a non-inverted differential version thereof |
| 0                 | 1                  | the noninverting input of the first operational amplifier is coupled to the inverting input of the second operational amplifier; the first and second operational amplifiers are configured to receive a single-ended signal and generate an inverted differential version thereof    |
| 0                 | 0                  | disallowed condition                                                                                                                                                                                                                                                                  |

13. The circuit of claim 1 wherein the circuit is implemented with discrete  
5 components.

14. The circuit of claim 1 wherein the circuit is an integrated circuit.

15. A circuit for generating a differential output signal, comprising:



a first operational amplifier having an output corresponding to one end of the differential output signal;

a second operational amplifier having an output corresponding to the other end of the differential output signal; and

5 a plurality of switches coupled to the first and second operational amplifiers;

wherein in a first mode the plurality of switches configure the first and second operational amplifiers to receive a single-ended input signal and generate the differential output signal, and in a second mode, the plurality of switches configure the first and second operational amplifiers to receive a differential input signal and  
10 generate the differential output signal, and wherein in each of the first and second modes the inverting input of one of the first and second operational amplifiers is coupled to the noninverting input of the other of the first and second operational amplifiers.

15 16. An electronic device comprising a circuit for generating a differential signal, the circuit comprising:

a first operational amplifier, the output of the first operational amplifier corresponding to one end of the differential signal; and

a second operational amplifier, the output of the second operational amplifier  
20 corresponding to the other end of the differential signal;

wherein the inverting input of the first operational amplifier is coupled to the noninverting input of the second operational amplifier.

17. A circuit for generating a differential signal, comprising:



a first operational amplifier having a signal input and a bias input, the output  
of the first operational amplifier corresponding to one end of the differential signal;  
and

a second operational amplifier having a signal input and a bias input, the  
5 output of the second operational amplifier corresponding to the other end of the  
differential signal;

wherein the signal input of the first operational amplifier is coupled to the bias  
input of the second operational amplifier.

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