Claims

1. A method for design based assessment of a device, comprising: defining, with one or more processors, a plurality of patterns of interest by applying at least one of optical rule checking or process window qualification to design data of the device; generating, with the one or more processors, a design based classification database including design data associated with each of the plurality of patterns of interest; measuring, with one or more inspection tools, one or more inspection results; comparing, with the one or more processors, the one or more inspection results to each of the plurality of patterns of interest to identify an occurrence of at least one of the plurality of patterns of interest in the inspection results; identifying, with the one or more processors, one or more critical patterns within the plurality of patterns of interest based on yield impact of each of the plurality of patterns of interest; identifying, with the one or more processors, a plurality of critical polygons defined via design data of the device and based on the identified one or more critical patterns; determining, with the one or more processors, a normalized polygon frequency for the device based on a frequency of occurrence for each of the plurality of critical polygons defined via design data of the device; determining, with the one or more processors, a device risk level of the device based on the determined normalized polygon frequency and a criticality for each of the plurality of critical polygons; and configuring, with the one or more processors, a process tool of a semiconductor fabrication facility based on the device risk level of the device to improve the end-of-line yield of the semiconductor fabrication facility when producing the device.

2. The method of claim 1, wherein the process yield data comprises: end-of-line process yield data.

3. The method of claim 1, wherein the receiving one or more inspection results comprises: receiving one or more inspection results from an inspection system.

4. The method of claim 3, wherein the inspection system comprises: at least one of a dark field inspection system and a bright field inspection system.

5. The method of claim 1, wherein the plurality of critical polygons is defined utilizing at least one of design rule checking, failure analysis and simulation.

6. The method of claim 1, further comprising: providing feedback to a user interface device indicative of a recommended action, wherein the recommended action is a function of the determined device risk level for the device.

7. The method of claim 6, wherein the recommended action comprises: adjusting a design in order to reduce design for manufacturability (DFM) defects.

8. The method of claim 6, wherein the recommended action comprises: adjusting a process specification.

9. A method for providing dynamic sampling comprising: identifying, with one or more processors, a plurality of critical pattern types on a wafer; determining, with the one or more processors, a device risk level based on a calculated risk level for each of the identified critical pattern types and a frequency of occurrence for each of the identified critical pattern types; identifying, with the one or more processors, one or more relevant excursions of the device based on the device risk level; and configuring an inspection tool to perform a dynamic sampling procedure on one or more of the plurality of identified critical pattern types, wherein the dynamic sampling procedure includes sampling the one or more identified critical pattern types at a rate based on the frequency of occurrence of the one or more identified critical pattern types.

10. The method of claim 9, wherein the dynamically sampling procedure comprises: sampling the one or more identified critical pattern types at a rate based on the frequency of occurrence and the one criticality of the one or more identified critical pattern types.

11. The method of claim 9, wherein the sampling the one or more the identified critical pattern types comprises: inspecting the one or more identified critical pattern types with an inspection tool.

12. A method for monitoring device processing comprising: performing, with one or more inspection tools, an inspection process on one or more devices between process steps performed with one or more process tools to monitor a process variation signature of one or more devices; associating, with one or more processors, one or more patterns of interest of the one or more devices with the monitored process variation signature via a design-based classification process; identifying, with the one or more processors, one or more equipment signatures associated with the one or more process tools based on the one or more associated patterns of interest; subtracting, with the one or more processors, the one or more equipment signatures from a defect map to isolate one or more defects in the reduced defect map; and transferring the one or more devices to a review tool for classification of the one or more defects in the reduced defect map; reviewing, with the review tool, the one or more defects isolated in the reduced defect map to classify the one or more defects of the reduced defect map; and configuring, with the one or more processors, a process tool of a semiconductor fabrication facility based on the classification of the one or more defects in the reduced defect map.

13. An apparatus for design based assessment of a device comprising: an inspection tool for measuring a set of inspection measurements of the illuminated portion of the device; and a

computing system in communication with the inspection tool, the computing system including one or more processors, which, when executing a set of program instructions, cause the one or more processors perform actions to: receive the set of inspection measurements from the inspection tool; define a plurality of patterns of interest by applying at least one of optical rule checking or process window qualification to design data of the device; generate a design based classification database including design data associated with each of the plurality of patterns of interest; compare the received one or more inspection measurements to each of the plurality of patterns of interest in order to identify an occurrence of at least one of the plurality of patterns of interest in the inspection measurements; identify one or more critical patterns within the plurality of patterns of interest based on yield impact of each of the plurality of patterns of interest; identify a plurality of critical polygons defined via design data of the device and based on the identified one or more critical patterns; determine a normalized polygon frequency for the device based on a frequency of occurrence for each of the plurality of critical polygons defined via design data of the device; determine a device risk level of the device based on the determined normalized polygon frequency and a criticality for each of the plurality of critical polygons; and configure, with the one or more processors, a process tool of a semiconductor facility based on the device risk level of the device to improve the end-of-line yield of the semiconductor fabrication facility when producing the device.

14. The apparatus of claim 13, wherein the inspection tool comprises: at least one of a dark field inspection tool and a bright field inspection tool.

15. The apparatus of claim 13, wherein the inspection tool comprises: an electron beam inspection tool.

16. An apparatus for providing dynamic sampling utilizing critical defects, comprising: a computing system including one or more processors, which, when executing a set of program instructions, cause the one or more processors to perform actions to: identify a plurality of critical pattern types on a device; determine a device risk level based on a calculated risk level for each of the identified critical pattern types and a frequency of occurrence for each of the identified plurality of critical pattern types; identify one or more relevant excursions of the device based on the device risk level; and an inspection tool placed in communication with the computing system, the inspection tool configured to perform a dynamic sampling procedure on one or more of the plurality of identified critical pattern types, wherein the dynamic sampling procedure includes sampling the one or more identified critical pattern types at a rate based on the frequency of occurrence of the one or more identified critical pattern types.

17. The apparatus of claim 16, wherein the inspection tool comprises: at least one of a dark field inspection tool and a bright field inspection tool.

18. The apparatus of claim 16, wherein the inspection tool comprises: an electron beam inspection tool.

19. An apparatus for monitoring device processing comprising: an inspection tool for performing inspection measurements on one or more devices between process steps performed with one or more process tools; and a computing system in communication with the inspection tool, the computing system including one or more processors, which, when executing a set of program instructions, cause the one or more processors to perform actions to: receive the inspection measurements of the one or more devices between the one or more process steps from the inspection tool; identify a process variation signature associated with the one or more devices based on the received inspection measurements of the one or more devices between the one or more process steps; associate one or more patterns of interest of the one or more devices with the identified process variation signature via a design-based classification process; and identify one or more equipment signatures associated with the one or more process tools based on the one or more associated patterns of interest; subtract the one or more equipment signatures from a defect map to isolate one or more defects in the reduced defect map; transfer the one or more devices to a review tool for classification of the one or more defects in the reduced defect map; review, with the review tool, the one or more defects isolated in the reduced defect map to classify the one or more defects of the reduced defect map; and configure a process tool of a semiconductor fabrication facility based on the classification of the one or more defects in the reduced defect map.

20. The apparatus of claim 19, wherein the inspection tool comprises: at least one of a dark field inspection tool and a bright field inspection tool.

21. The apparatus of claim 19, wherein the inspection tool comprises: an electron beam inspection tool.