



ABSTRACT

A solid state relay composed of a series connected pair of LDMOSFETs has a minimized output capacitance. Each LDMOSFET is configured to have a silicon layer of a first conductive type, a drain
5 region of the first conductive type diffused in the top surface of the silicon layer, a well region of a second conductive type diffused in the silicon layer in a laterally spaced relation from the drain region, and a source region of the first conductive type diffused within the well region to define a channel extending between the source region and a
10 confronting edge of the well region along the top surface of the silicon layer. Each LDMOSFET is of an SOI (Silicon-On-Insulator) structure composed of a silicon substrate placed on a supporting plate, a buried oxide layer on the silicon substrate, and the silicon layer on the buried oxide layer. The well region is diffused over the full depth of the
15 silicon layer to have its bottom in contact with the buried oxide layer, so that the well region forms with the silicon layer a P-N interface only at a small area adjacent the channel. Because of this reduced P-N interface and also because of the buried oxide layer exhibiting a much lower capacitance than the silicon layer, it is possible to greatly reduce a drain-
20 source capacitance for minimizing the output capacitance of the relay in the non-conductive condition.

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