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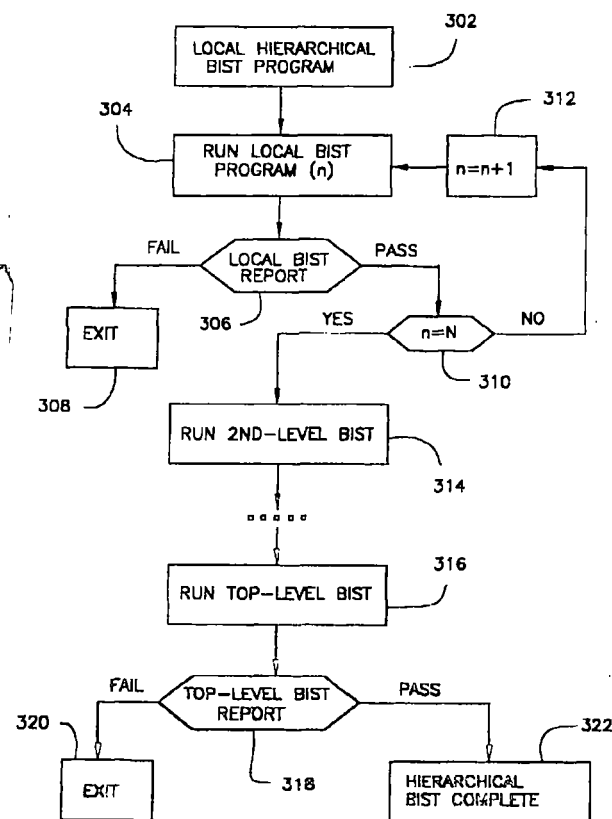
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- (71) Applicant: INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, NY 10504 (US).
- (71) Applicant (for MG only): IBM UNITED KINGDOM LIMITED [GB/GB]; PO Box 41, North Harbour, Portsmouth, Hampshire PO6 3AU (GB).
- (72) Inventors: CHEN, Howard, Hao; 2710 Evergreen Street, Yorktown Heights, NY 10598 (US). HSU, Louis, Lu-Chen; 7 Crosby Court, Fishkill, NY 12524 (US). WANG, Li-Kong; 2 Morgan Court, Montvale, NJ 07645 (US).
- (74) Agent: BURTT, Roger, James; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester, Hampshire SO21 2JN (GB).
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(54) Title: HIERARCHICAL BUILT-IN SELF-TEST FOR SYSTEM-ON-CHIP DESIGN



(57) Abstract: Hierarchical built-in self-test methods and arrangement for verifying system functionality. As a result, an effective built-in self-test methodology is provided for conducting complete system-on-chip testing, to ensure both the circuit reliability and performance of system-on-chip design. As an added advantage, development costs are reduced for system-on-chip applications.

WO 02/095586 A3



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