1 470 587

PATENT SPECIFICATION (11) 1 470 587

(21) Application No. 38068/74 (22) Filed 30 Aug. 1974
(31) Convention Application No. 403244 (32) Filed 3 Oct. 1973 in
(33) United States of America (US)
(44) Complete Specification published 14 April 1977
(51) INT CL² H01L 29/78
(52) Index at acceptance
H1K 11A3 11C1 11C4 11D1 11D 11Y 1C7F1 1C7FY 1D3A 2S20 4C11 4C14 4F17 4F20 5B2 7A4 7E 9R EC
H4F D12X D30K D53D D83B

(19)



(54) LINEAR IMAGING ARRAYS

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California, 94042, United States of America, a Corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to linear imaging arrays.

The invention provides a linear imaging array comprising

a plurality of light sensing means for accumulating a corresponding plurality of charge packets, each charge packet having an amplitude proportional to the amount of light incident on the light sensing means in which the charge packet is accumulated, the plurality of light sensing means being located along a line;

first shift register means located on one side of the line of light sensing means, the first shift register means including a plurality of storage regions for storing packets of charge, the plurality of storage regions corresponding on a one-to-one basis to the plurality of light sensing means;

first control means for controlling the transfer of charge packets accumulated in the plurality of light sensing means to appropriate storage regions in the first shift register means;

first means for shifting the charge packets transferred from the plurality of light sensing means to the first shift register means along the first shift register means to an output means;

second shift register means located on a second side of the plurality of light sensing means, the second shift register means including a plurality of storage regions for storing packets of charge, the plurality of storage regions corresponding on a one-to-one basis to the plurality of light sensing means;

second control means for controlling the transfer of charge packets accumulated in the plurality of light sensing means to appropriate storage regions in the second shift register means; and

second means for shifting the charge packets transferred from the plurality of light sensing means to the second shift register means along the second shift register means to a second output means.

Such an array is particularly useful when the linear imaging array operates as a two- or four-phase system. When the imaging array operates as a two-phase system, the use of two transport arrays avoids the necessity of doubling the read out frequency to obtain interleaved (i.e. interlaced) operation.

The invention will be readily understood from the following illustrative description and the accompanying drawing, in which the single Figure is a schematic plan view of a linear imaging array in which two potential wells (and two electrodes) are associate with a single potential well (i.e. charge storage region) in the line of light sensing means.

In the illustrated linear imaging array, a line of light sensing elements 54*a* to 54*j* comprises regions of semiconductor material 50, for example silicon, underlying a transparent, conductive photogate 52. Photogate 52 is separated from the underlying semiconductor material by insulation, for example an oxide of silicon (for simplicity not shown in the Figure). The potential well associated with light sensing element 54*p* (where *p* is an integer which varies from *a* to *j* and *j* represents the number of light sensing elements in the array) is formed in a region of semiconductor material surrounded on two sides by portions of a channel stop region 51. Thus the potential well in light sensing element 54*p* is separated from the potential wells of the adjacent light sensing element 54 (*p*−1) and 54 (*p*+1) by portions of the channel stop diffusion such as portions 51*a* through 51*i* Portions 51*a* through 51*i* of the channel stop diffusion are not connected to each other. Thus the channel stop diffusion surrounds each region of semiconductor material

containing a potential well on two sides leaving open the two sides facing two shift registers 55 and 56.

A charge packet accumulated in a particular light sensing element 54*p* can thus be read out to the corresponding charge storage region in either shift register 55 or shift register 56. However, in actual operation, the charge packets accumulated in the potential wells associated with light sensing elements 54*a*, 54*c*, 54*e*, 54*g* and 54*i* (hereinafter called the "odd" light sensing elements) will be read out to the right side of the Figure into the corresponding charge storage regions of shift register 55, while the charge packets accumulated in the potential wells associated with light sensing elements 54*b*, 54*d*, 54*f*, 54*h* and 54*j* (hereinafter called the "even" light sensing elements) will be read out to the left to the corresponding charge storage regions in shift register 56. Looking at light sensing element 54*b*, for example, an even light sensing element, the charge packet in this element is read out to the left by lowering the potential ϕ_1 on electrode 56*b* while at the same time raising the potential ϕ_2 on electrode 55*b*. Simultaneously, the potential on a transfer gate 53*a* is lowered to allow this charge packet to transfer from light sensing element 54*b* to the charge storage region in transport array 56 beneath electrode 56*b*. The potential on transfer gate 53*b* is held at its normal level.

Simultaneously with the transfer of the charge packet from light sensing element 54*b*, the charge packets in all of the even light sensing elements are transferred into the corresponding charge storage regions in shift register 56. The charge packets accumulated in the odd light sensing elements are transferred to the corresponding charge storage regions in transport array 55 in a similar manner. Charge from an odd light sensing element is not transferred to the corresponding charge storage region transport array 55 at the same time as the charge from an even element is transmitted to its corresponding charge storage region in transport array 56 because the potential on transfer gate 53*b* (or 53*a*) is kept high when the potential on transfer gate 53*a* (or 53*b*) is lowered.

Accordingly, charge packets are removed from the odd light sensing elements by appropriately controlling the potentials on transfer gate 53*b* and the electrodes in both shift registers 55 and 56 and from the even light sensing elements by appropriately controlling the potentials on transfer gate 53*a* and the electrodes in both shift registers 55 and 56 and from the even light sensing elements by appropriately controlling the potentials on transfer gate 53*a* and the electrodes in both shift registers 55 and 56.

Electrodes 55*a* to 55*j* and 56*a* to 56*j* are operated in response to a two-phase (or four-phase) signal in a manner well known in the CCD arts. Thus a charge packet transferred from light sensing element 54*a* to the charge storage region of semiconductor material beneath electrode 55*a* is subsequently transferred along the transport array 55 to an output diode 58*b* while simultaneously a charge packet accumulated in light sensing element 54*b* is transferred into an adjacent charge storage region in the semiconductor material beneath electrode 56*b* and then transferred to output diode 58*a*. Thus the read out frequency of the signals used in the array of the Figure is precisely that which would be used in the prior art.

Output electrodes 57*a* and 57*b* are formed on the insulation overlying the semiconductor material between the last storage region 56*j* and the output diode 58*a* and between the last storage region 55*j* and the output diode 58*b* respectively for controlling the transfer of charge packets from the last storage regions to the associated diodes.

The array shown in the Figure has the advantage that a charge packet from a given light sensing element can be transmitted to a corresponding charge storage region in either transport array 55 or transport array 56 by properly controlling the potentials applied to transfer gates 53*a* and 53*b* and the electrodes associated with shift registers 55, 56. Alternatively, if this flexibility is not desired, an additional channel stop region can be formed on the left (or right) side of each odd light sensing element and on the right (or left) side of each even light sensing element, for example. Thus the channel stop region will then have a serpentine shape and a charge from a given light sensing element can only be transmitted to one of the two transport arrays.

WHAT WE CLAIM IS:—

1. A linear imaging array comprising

a plurality of light sensing means for accumulating a corresponding plurality of charge packets, each charge packet having an amplitude proportional to the amount of light incident on the light sensing means in which the charge packet is accumulated, the plurality of light sensing means being located along a line;

first shift register means located on one side of the line of light sensing means, the first shift register means including a plurality of storage regions for storing packets of charge, the plurality of storage regions corresponding on a one-to-one basis to the plurality of light sensing means;

first control means for controlling the transfer of charge packets accumulated in the plurality of light sensing means to appropriate storage regions in the first shift register means;

first means for shifting the charge packets

containing a potential well on two sides leaving open the two sides facing two shift registers 55 and 56.

A charge packet accumulated in a particular light sensing element 54*p* can thus be read out to the corresponding charge storage region in either shift register 55 or shift register 56. However, in actual operation, the charge packets accumulated in the potential wells associated with light sensing elements 54*a*, 54*c*, 54*e*, 54*g* and 54*i* (hereinafter called the "odd" light sensing elements) will be read out to the right side of the Figure into the corresponding charge storage regions of shift register 55, while the charge packets accumulated in the potential wells associated with light sensing elements 54*b*, 54*d*, 54*f*, 54*h* and 54*j* (hereinafter called the "even" light sensing elements) will be read out to the left to the corresponding charge storage regions in shift register 56. Looking at light sensing element 54*b*, for example, an even light sensing element, the charge packet in this element is read out to the left by lowering the potential ϕ_1 on electrode 56*b* while at the same time raising the potential ϕ_2 on electrode 55*b*. Simultaneously, the potential on a transfer gate 53*a* is lowered to allow this charge packet to transfer from light sensing element 54*b* to the charge storage region in transport array 56 beneath electrode 56*b*. The potential on transfer gate 53*b* is held at its normal level.

Simultaneously with the transfer of the charge packet from light sensing element 54*b*, the charge packets in all of the even light sensing elements are transferred into the corresponding charge storage regions in shift register 56. The charge packets accumulated in the odd light sensing elements are transferred to the corresponding charge storage regions in transport array 55 in a similar manner. Charge from an odd light sensing element is not transferred to the corresponding charge storage region transport array 55 at the same time as the charge from an even element is transmitted to its corresponding charge storage region in transport array 56 because the potential on transfer gate 53*b* (or 53*a*) is kept high when the potential on transfer gate 53*a* (or 53*b*) is lowered.

Accordingly, charge packets are removed from the odd light sensing elements by appropriately controlling the potentials on transfer gate 53*b* and the electrodes in both shift registers 55 and 56 and from the even light sensing elements by appropriately controlling the potentials on transfer gate 53*a* and the electrodes in both shift registers 55 and 56 and from the even light sensing elements by appropriately controlling the potentials on transfer gate 53*a* and the electrodes in both shift registers 55 and 56.

Electrodes 55*a* to 55*j* and 56*a* to 56*j* are operated in response to a two-phase (or four-phase) signal in a manner well known in the CCD arts. Thus a charge packet transferred from light sensing element 54*a* to the charge storage region of semiconductor material beneath electrode 55*a* is subsequently transferred along the transport array 55 to an output diode 58*b* while simultaneously a charge packet accumulated in light sensing element 54*b* is transferred into an adjacent charge storage region in the semiconductor material beneath electrode 56*b* and then transferred to output diode 58*a*. Thus the read out frequency of the signals used in the array of the Figure is precisely that which would be used in the prior art.

Output electrodes 57*a* and 57*b* are formed on the insulation overlying the semiconductor material between the last storage region 56*j* and the output diode 58*a* and between the last storage region 55*j* and the output diode 58*b* respectively for controlling the transfer of charge packets from the last storage regions to the associated diodes.

The array shown in the Figure has the advantage that a charge packet from a given light sensing element can be transmitted to a corresponding charge storage region in either transport array 55 or transport array 56 by properly controlling the potentials applied to transfer gates 53*a* and 53*b* and the electrodes associated with shift registers 55, 56. Alternatively, if this flexibility is not desired, an additional channel stop region can be formed on the left (or right) side of each odd light sensing element and on the right (or left) side of each even light sensing element, for example. Thus the channel stop region will then have a serpentine shape and a charge from a given light sensing element can only be transmitted to one of the two transport arrays.

WHAT WE CLAIM IS:—

1. A linear imaging array comprising

a plurality of light sensing means for accumulating a corresponding plurality of charge packets, each charge packet having an amplitude proportional to the amount of light incident on the light sensing means in which the charge packet is accumulated, the plurality of light sensing means being located along a line;

first shift register means located on one side of the line of light sensing means, the first shift register means including a plurality of storage regions for storing packets of charge, the plurality of storage regions corresponding on a one-to-one basis to the plurality of light sensing means;

first control means for controlling the transfer of charge packets accumulated in the plurality of light sensing means to appropriate storage regions in the first shift register means;

first means for shifting the charge packets

* C L M S *

transferred from the plurality of light sensing means to the first shift register means along the first shift register means to an output means;

second shift register means located on a second side of the plurality of light sensing means, the second shift register means including a plurality of storage regions for storing packets of charge, the plurality of storage regions corresponding on a one-to-one basis to the plurality of light sensing means;

second control means for controlling the transfer of charge packets accumulated in the plurality of light sensing means to appropriate storage regions in the second shift register means; and

second means for shifting the charge packets transferred from the plurality of light sensing means to the second shift register means along the second shift register means to a second output means.

2. A linear array as claimed in claim 1 in which the plurality of light sensing means comprises N sets of light sensing means, each light sensing means in a set being spaced from the nearest light sensing means in the same set by one light sensing means from each of the other sets.

3. A linear array as claimed in claim 2 in which N=2.

4. A linear array as claimed in claim 2 in which N=4.

5. A linear array as claimed in claim 2, 3 or 4 in which the first and second control means each comprises:

means for simultaneously transferring charge packets from a set of light sensing means to either the first or second shift register means while preventing the charge packets in the remaining sets of light sensing means from being transferred to either the first or second shift register means.

6. A linear array as claimed in any preceding claim in which each light sensing means comprises:

a first region of semiconductor material;

insulation overlying the first region of semiconductor material;

a transparent electrode overlying the insulation and the first region of semiconductor material; and

channel stop regions defining on two sides the lateral extent of the first region of semiconductor material.

7. A linear array as claimed in claim 6 in which the semiconductor material comprises silicon.

8. A linear array as claimed in claim 6 or 7 in which the insulation comprises an oxide of silicon.

9. A linear array as claimed in claim 6, 7 or 8 in which the first control means comprises a first conductive gate placed on the insulation adjacent to, but in non-conductive relation with, each transparent electrode, the first conductive gate being capable of having a potential applied to it to control the potential in the semiconductor material underlying the first conductive gate, the semiconductor material underlying the first conductive gate defining on a third side the lateral extent of each first region of semiconductor material, and

the second control means comprises a second conductive gate placed on the insulation adjacent to, but in non-conductive relation with, each transparent electrode, the second conductive gate being capable of having a potential applied to it to control the potential in the semiconductor material underlying the second conductive gate, the semiconductor material underlying the second conductive gate defining on a fourth side the lateral extent of each first region of semiconductor material.

10. A linear array as claimed in claim 9 in which the plurality of storage regions for storing packets of charge in the first shift register means comprises a plurality of second regions of semiconductor material, each second region being placed adjacent to, but separated by the region of semiconductor material beneath the first conductive gate from a first region of semiconductor material in a corresponding light sensing means, the second region of semiconductor material being arranged to receive a charge packet from said first region of semiconductor material in said corresponding light sensing means; and

the plurality of storage regions for storing packets of charge in said second shift register means comprises a plurality of third regions of semiconductor material, each third region being placed adjacent to, but separated by the region of semiconductor material beneath said second conductive gate from a first region of semiconductor material in a corresponding light sensing means, said third region of semiconductor material being arranged to receive a charge packet from said first region of semiconductor material in said corresponding light sensing means.

11. A linear array as claimed in claim 10 in which the first shift register means includes in addition a separate electrode overlying but insulated from each second region in the semiconductor material, each electrode being capable of having its potential varied in accordance with control signals.

12. A linear array as claimed in claim 10 or 11 in which the second shift register means includes in addition a separate electrode overlying but insulated from each third region in the semiconductor material, each said electrode being capable of having its potential varied in accordance with control signals.

13. A linear array as claimed in any one of claims 6 to 12 in which the first output means is at one end of the first shift register

* C L M S *

means and the second output means is at one end of the second shift register means.

14. A linear array as claimed in claim 13 in which the first output means comprises a first output diode formed in the semiconductor material and a first output electrode formed on the insulation overlying the semiconductor material between the first output diode and the last storage region in the first shift register means for controlling the transfer of charge packets from the last storage region to the output diode; and

the second output means comprises a second output diode formed in the semiconductor material and a second output electrode formed on the insulation overlying the semiconductor material between the second output diode and the last storage region in the second shift register means for controlling the transfer of charge packets from the last storage region to the second output diode.

15. A linear imaging array substantially as herein described with reference to the accompanying drawing.

POLLAK MERCER & TENCH,
Chartered Patent Agents,
Chancery House,
53—64 Chancery Lane,
London WC2A 1HJ,
Agents for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1977
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

* C L M S *