

SEMICONDUCTOR STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese patent application No. 202110116929.0, filed to the China National Intellectual Property Administration on January 28, 2021 and entitled "SEMICONDUCTOR STRUCTURE", the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the technical field of semiconductors, and in particular relates to a semiconductor structure.

BACKGROUND

[0003] Capacitor can store energy, when it is connected between a power end and a grounding end in parallel, fluctuation of a voltage generated by the power end in an operation process of a circuit becomes smooth, and the operation performance of the power end is stable. Therefore, in circuit designs, it is often necessary to add a large number of capacitive structures to enhance the stability of the power end. Not only the power end, the signal end may also be provided with capacitors when high-frequency noise is required to be removed at the signal end.

[0004] In a conventional semiconductor chip, the capacitor structure is usually added in a spare space of the chip, so as to stabilize a power end or a signal end in the chip. In this way, however, the area of the chip is eventually increased, thereby increasing the product cost.

SUMMARY

[0005] According to some embodiments, a semiconductor chip is provided.

[0006] A semiconductor structure may include a pad structure and a capacitor structure.

[0007] The pad structure is disposed above a substrate.

[0008] The capacitor structure is disposed between the substrate and the pad structure, and arranged opposite to the pad structure, and includes at least two capacitor units that are connected in parallel and spaced apart from each other. Each of the capacitor units includes at least one capacitor device.

[0009] The above semiconductor structure may effectively improve a utilization rate of a region where the pad structure is located. Compared with a conventional configuration manner that the capacitor structure is disposed in a spare space of a chip, the present disclosure can effectively prevent the area of the chip from increasing due to disposing of the capacitor structure. Meanwhile, when the pad structure has a larger size, the size of each of the capacitor units is smaller according to the present disclosure. In a manufacturing process, various related films of the capacitor unit having the smaller size may be subjected to uniform film formation easily. Therefore, in the present disclosure, the film formation quality of the various related films can be improved, thereby improving the reliability of the capacitor structure, and stabilizing the power voltage of a related power supply.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In order to describe the technical solutions in the embodiments of the disclosure or a conventional art more clearly, the drawings required to be used in descriptions about the embodiments or the conventional art are simply introduced below. It is apparent that the drawings described below are only some embodiments of the disclosure. Other drawings may further be obtained by those of ordinary skilled in the art according to these drawings without creative work.

[0011] FIG. 1 is a schematic sectional view of a semiconductor structure provided in an embodiment.

[0012] FIG. 2 is a schematic plan view of a semiconductor structure provided in an embodiment.

[0013] FIG. 3 is a schematic view of a local structure of a semiconductor structure provided in an embodiment.

[0014] FIG. 4 is a schematic view of electrical connection between a conductive layer and a capacitor device provided in an embodiment.

[0015] FIG. 5 is a schematic view of a conductive layer in FIG. 3.

[0016] FIG. 6 is a schematic view of a first metal layer, a first conductive part and a third conductive part in FIG. 3.

[0017] FIG. 7 is a schematic view of a capacitor of a transistor type.

[0018] FIG. 8 is a schematic view of a capacitor structure in FIG. 3.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] In order to make the disclosure convenient to understand, the disclosure will be described more comprehensively below with reference to the drawings. The drawings show preferred embodiments of the disclosure. However, the disclosure may be implemented in various forms and is not limited to the embodiments described herein. Instead, these embodiments are provided to make the contents disclosed in the disclosure understood more thoroughly and comprehensively.

[0020] Unless otherwise defined, all technical and scientific terms used herein have the same meanings as commonly understood by those skilled in the art that the disclosure belongs to. Herein, terms used in the description of the disclosure are used only for describing specific embodiments and not intended to limit the disclosure.

[0021] It is to be understood that description that an element or layer is "above", "adjacent to", "connected to", or "coupled to" another element or layer may refer to that the element or layer is directly above, adjacent to, connected to or coupled to the other element or layer, or an intermediate element or layer may exist therebetween. On the contrary, description that an element is "directly on", "directly adjacent to", "directly connected to" or "directly coupled to" another element or layer refers to that there is no intermediate element or layer therebetween. It is to be understood that, although various elements, components, regions,

layers, doping types and/or parts may be described with terms first, second, third, etc., these elements, components, regions, layers, doping types and/or parts should not be limited to these terms. These terms are used only to distinguish one element, component, region, layer, doping type or part from another element, component, region, layer, doping type or part. Therefore, a first element, component, region, layer, doping type or part discussed below may represent a second element, component, region, layer or part without departing from the teaching of the disclosure. For example, a first conductive part may become a second conductive part. Similarly, the second conductive part may become a first doping type.

[0022] Spatially relational terms such as "below", "under", "lower", "beneath", "above", and "upper" may be used herein for describing a relationship between one element or feature and another element or feature illustrated in the drawings. It is to be understood that, in addition to the orientation shown in the drawings, the spatially relational terms further include different orientations of devices in use and operation. For example, if the device in the drawings is turned over, elements or features described as being "under" or "beneath" or "below" other elements or features will be oriented to be "on" the other elements or features. Therefore, the exemplary terms "under" and "below" may include both upper and lower orientations. Moreover, the device may include other orientation (such as rotation by 90 degrees or in other orientations) and the spatial descriptors used herein may be interpreted accordingly.

[0023] As used herein, singular forms "a/an", "one", and "the" may include the plural forms, unless otherwise specified types in the context. It is also to be understood that, when terms "composed of" and/or "including" are used in this specification, the presence of the features, integers, steps, operations, elements and/or components may be determined, but the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups is not exclusive. Also, as used herein, term "and/or" includes any and all combinations of the related listed items.

[0024] Referring to FIG. 1 and FIG. 2, a semiconductor structure is provided according to an embodiment, which includes a substrate 100, a pad structure 200, and a capacitor structure 300. Specifically, the semiconductor structure can be an upper structure on a semiconductor chip.

[0025] The substrate 100 can be, but not limited to, a silicon substrate.

[0026] The pad structure 200 is disposed above the substrate 100, and can be for example, a power pad or a signal pad or a grounding pad. The specific type of the pad structure 200 is not limited.

[0027] Specifically, when the pad structure 200 is the power pad, it can be electrically connected to a packaging substrate via a lead, so as to acquire a corresponding power voltage (such as VDDQ, VPP and VDD). When the pad structure 200 is the signal pad, it can be electrically connected to the packaging substrate via a lead, so as to acquire a control signal (such as a Chip Select (CS) signal and a RESET signal). When the pad structure 200 is the grounding pad, it can be electrically connected to the packaging substrate via a lead, so as to be connected in parallel and to be grounded.

[0028] The capacitor structure 300 is connected in parallel between a power end and a grounding end of a chip circuit, and is configured to enable fluctuation of 1 voltage generated by a power supply in an operation process of a circuit to be smooth and to remove high-frequency noise on the power supply, so as to stabilize the operation performance of the power supply.

[0029] Specifically, the capacitor structure 300 is disposed between the substrate 100 and the pad structure 200, and is arranged opposite to the pad structure 200. Therefore, the capacitor structure 300 is disposed below the pad structure 200.

[0030] Therefore, a utilization rate of a region where the pad structure 200 is located can be effectively improved in the embodiment. Compared with a conventional configuration manner that a capacitor structure is disposed in a spare space of a chip, the embodiment can effectively prevent the area of the chip from increasing due to disposing of the capacitor structure.

[0031] Also, referring to FIG. 3, the capacitor structure 300 in the embodiment includes at least two capacitor units 310 that are connected in parallel and spaced apart from each other. Each of the capacitor units may include one or more capacitor devices 311.

[0032] Therefore, when the pad structure 200 has a larger size, the size of each of the capacitor units 310 is smaller. In a manufacturing process, various related films of the capacitor unit having the smaller size can be subjected to uniform film formation easily. Therefore, in the present disclosure, the film formation quality of the various related films can be improved,

thereby improving the reliability of the capacitor structure, and stabilizing the power voltage of a related power supply.

[0033] It can be understood that the “related power supply” herein refers to a power end to which the capacitor structure 300 is connected.

[0034] In an embodiment, an orthographic projection of the capacitor structure 300 on the substrate 100 is located within an orthographic projection of the pad structure 200 on the substrate 100.

[0035] In this case, the capacitor structure 300 is completely located below the pad structure 200, thereby utilizing the utilization rate of a region where the pad structure 200 is located more effectively. Therefore, the area of the chip is completely unaffected by disposing the capacitor structure 300, thereby facilitating miniaturization of the chip.

[0036] Of course, the present disclosure is not limited thereto. The orthographic projection of the capacitor structure 300 on the substrate 100 may also be partially located outside the orthographic projection of the pad structure 200 on the substrate 100. Alternatively, the orthographic projection of the capacitor structure 300 on the substrate 100 can be coincided with the orthographic projection of the pad structure 200 on the substrate 100.

[0037] In an embodiment, a center of the orthographic projection of the capacitor structure 300 on the substrate 100 is coincided with a center of the orthographic projection of the pad structure 200 on the substrate 100.

[0038] At this time, the capacitor structure 300 is aligned with the pad structure 200, so that the capacitor structure 300 has a uniform performance at various positions.

[0039] It is to be noted that the center of the orthographic projection of the capacitor structure 300 on the substrate 100 may also not be coincided with the center of the orthographic projection of the pad structure 200 on the substrate 100 in the present disclosure, which is not limited in the present disclosure.

[0040] In an embodiment, referring to FIG. 4, the capacitor device 311 in the capacitor unit 310 includes a first polar plate 3111 and a second polar plate 3112. The first polar plate 3111 and the second polar plate 3112 are arranged opposite to each other, so as to store charges.

[0041] Also, referring to FIG. 1, the semiconductor structure may further include a conductive layer 400. The conductive layer 400 may include a first conductive portion 410 and a second conductive portion 420. The first conductive portion 410 and the second conductive portion 420 are mutually insulated.

[0042] The first conductive portion 410 is electrically connected to the first polar plates 3111 of each of the capacitor devices 311, i.e., the first polar plate 3111 of the capacitor device 311 in each of the capacitor units 310 is electrically connected to the first conductive portion 410. Therefore, due to the configuration of the first conductive portion 410, the first polar plates 3111 of the capacitor devices 311 in each of the capacitor units 310 are all electrically connected to the same circuit node.

[0043] Similarly, the second conductive portion 420 is electrically connected to the second polar plate 3112 of each of the capacitor devices 311, i.e., the second polar plate 3112 of the capacitor device 311 in each of the capacitor units 310 is electrically connected to the second conductive portion 420. Therefore, due to the configuration of the second conductive portion 420, the second polar plates 3112 of the capacitor devices 311 in each of the capacitor units 310 are all electrically connected to the same circuit node.

[0044] Therefore, due to the configuration of the conductive layer 400, the capacitor devices 311 in each of the capacitor units 310 can be conveniently and effectively connected in parallel, so as to form the capacitor structure 310.

[0045] Meanwhile, one of the first conductive portion 410 and the second conductive portion 420 is electrically connected to the power end, and the other one is electrically connected to the grounding end. That is, the first conductive portion 410 is electrically connected to the power end in the chip circuit, and the second conductive portion 420 is electrically connected to the grounding end in the chip circuit. Alternatively, the second conductive portion 420 is electrically connected to the power end in the chip circuit, and the first conductive portion 410 is also electrically connected to the grounding end in the chip circuit.

[0046] In this way, the capacitor structure 310 formed by parallel connection of the capacitor devices 311 can be conveniently and effectively introduced into the chip circuit.

[0047] Specifically, the capacitor device 311 can be a transistor-type capacitor,

referring to FIG. 4 and FIG. 7, a gate of the transistor-type capacitor forms the first polar plate 3111 of the capacitor device, and a source and a drain of the transistor-type capacitor and corresponding parts of the substrate 100 form the second polar plate 3112 of the capacitor device 311.

[0048] In this way, the first polar plate 3111 (i.e., the gate of the transistor-type capacitor) of each of the capacitor devices 311 can be electrically connected to the first conductive portion 410 via a first capacitor through hole 410a. The second polar plate 3112 (i.e., the source and the drain of the transistor-type capacitor and the corresponding parts of the substrate 100) of each of the capacitor devices 311 can be electrically connected to the second conductive portion 420 via a second capacitor through hole 420a.

[0049] Also, the first conductive portion 410 can be electrically connected to the power end in the chip circuit, and the second conductive portion 420 can be electrically connected to the grounding end in the chip circuit.

[0050] When the capacitor device 311 can be a transistor-type capacitor, the gate of the transistor-type capacitor forms the second polar plate 3112 of the capacitor device, and the source and the drain of the transistor-type capacitor and the corresponding parts of the substrate 100 form the first polar plate 3111 of the capacitor device 311, which are not limited in the present disclosure.

[0051] Alternatively, the capacitor device 311 may also be a capacitor of other types (such as a parallel-plate capacitor formed by two metal plates which are oppositely arranged), which is not limited in the disclosure.

[0052] In an embodiment, referring to FIG. 5 and FIG. 3, the second conductive portion 420 of the conductive layer 400 is in an integrated structure, and spans the various capacitor devices 311 in the capacitor structure 300, so that the second polar plates 3112 of each of the capacitor devices 311 in the capacitor structure 300 can be electrically connected to the second conductive portion 420 via interconnected through holes.

[0053] The first conductive portion 410 is in a separated structure, and includes a plurality of sub-conductive portions 411 electrically connected. The sub-conductive portions 411 span the adjacent capacitor devices 311 in the capacitor structure 300, so that the first polar plate 3111 of the adjacent capacitor devices 311 can be electrically connected to the same sub-

conductive portion 411 via interconnected through holes. Also, the sub-conductive portions 411 of the first conductive portion 410 are mutually and electrically connected. Therefore, in this way, the first polar plates 3111 of each of the capacitor devices 311 in the capacitor structure 300 can be electrically connected together.

[0054] Also, orthographic projections of each of the sub-conductive parts 411 of the first conductive portion 410 on the substrate 100 are spaced apart from the orthographic projection of the second conductive portion 420 on the substrate 100. That is, the orthographic projection of the first conductive portion 410 is spaced apart from the orthographic projection of the second conductive portion 420 on the substrate 100.

[0055] In this way, the first conductive portion 410 and the second conductive portion 420 of the embodiment can be formed synchronously in a film formation process, which can effectively simplify the process, and production efficiency can be increased.

[0056] Specifically, during the process, a layer of conductive material layer can be formed at first, and then the conductive material layer is patterned, so as to form the second conductive portion 420 and the plurality of sub-conductive portions 411.

[0057] Of course, the first conductive portion 410 and the second conductive portion 420 of the embodiment may also be formed step by step in different film formation processes. In this way, orthographic projections of each of the sub-conductive portions 411 of the first conductive portion 410 on the substrate 100 are spaced apart from orthographic projection of the second conductive portion 420 on the substrate 100.

[0058] It is to be noted that the orthographic projection of the first conductive portion 410 is spaced apart from the orthographic projection of the second conductive part 420 on the substrate 100 in the embodiment, but the present disclosure is not limited thereto.

[0059] For example, in some embodiments, the first conductive portion 410 and the second conductive portion 420 can be formed step by step. In this way, the first conductive portion 410 and the second conductive portion 420 can be disposed to be in an integrated structure. In this case, the orthographic projection of the first conductive part 410 on the substrate 100 and the orthographic projection of the second conductive part 420 on the substrate 100 may also be completely or partially coincided with each other.

[0060] For another example, in some embodiments, the first conductive portion 410 and the second conductive portion 420 can be formed step by step. In this way, the orthographic projection of the first conductive portion 410 in the separated structure on the substrate 100 and the orthographic projection of the second conductive portion 420 in the integrated structure on the substrate 100 may also be mutually connected.

[0061] Moreover, in the embodiment, if the first conductive portion 410 of the separated structure of the conductive layer 400 is electrically connected to the power end, the second conductive part 420 of the integrated structure is electrically connected to the grounding end. Furthermore, when the semiconductor chip is provided with the plurality of semiconductor structures in the embodiment, the second conductive portions 420 of the conductive layers 200 of the plurality of semiconductor structures can be connected together to form an integrated structure.

[0062] Of course, when the semiconductor chip is provided with the plurality of semiconductor structures of the embodiment, the second conductive portions 420 of the conductive layers 200 of the plurality of semiconductor structures may also be disposed separately, while the second conductive portion 420 in each semiconductor structure is in an integrated structure.

[0063] Meanwhile, in the embodiment, the first conductive portion 410 of the separated structure may also be electrically connected to the grounding end, and the second conductive portion 420 of the integrated structure is electrically connected to the power end. Then, when the semiconductor chip is provided with the plurality of semiconductor structures of the embodiment, the conductive layers 200 of the plurality of semiconductor structures can be independently disposed.

[0064] In an embodiment, referring also to FIG. 3, on the basis of the above embodiments, each capacitor unit 310 includes at least two capacitor devices 311 disposed in parallel. Each of the capacitor devices 311 in the capacitor structure 300 are arranged in M-row N-column array, where both the M and the N are integers greater than or equal to 2.

[0065] Arranging the capacitor devices 311 in array can facilitate layout design of sub-conductive portions 411 of the first conductive portion 410 and the second conductive portion 420.

[0066] In the embodiment, referring to FIG. 3 and FIG. 5 at the same time, the sub-conductive portions 411 includes a first sub-portion 4111. The same first sub-portion 4111 spans four capacitor devices 311 which are adjacent in pairs and distributed symmetrically around a center. At this time, the same first sub-portion 4111 can be electrically connected to the four capacitor devices 311 at the same time, so as to provide power end signals for the four capacitor devices 311, thus implementing the multi-function performance. As an example, the first sub-portion 4111 can be “工” shaped.

[0067] At this time, furthermore, four corners of each capacitor device 311 can be electrically connected to the sub-conductive portion 411, so that each capacitor device 311 may obtain electrical signals stably and reliably.

[0068] It is to be understood that besides the first sub-portion 4111, the sub-conductive portion 411 may further include a second sub-portion 4112 only spans adjacent two capacitor devices 311. The second sub-portion 4112 can span adjacent two capacitor devices 311 located at the edge of the capacitor structure 300, and the first sub-portion 4111 can be located in an annular region formed by the first sub-portion 4112.

[0069] Also, the conductive layer 400 may also include a third conductive portion 430, which can be disposed above the capacitor structure 311 located in the corner, so as to be electrically connected to the capacitor structure 311 located in the corner.

[0070] In an embodiment, referring to FIG. 3 and FIG. 6, the pad structure 200 includes a first metal layer 210. One end of the first metal layer 210 is electrically connected to the power end. Moreover, the other end of the first metal layer 210 is electrically connected to each of the sub-conductive portions 411 via a first through hole 210a.

[0071] By disposing the first metal layer 210, each of the sub-conductive portions 411 can be electrically connected together simply and effectively, and are also electrically connected to the power end. In this case, the first conductive portion 410 of the separated structure is electrically connected to the power end, and the second conductive portion 420 of the integrated structure is electrically connected to the grounding end.

[0072] In an embodiment, similarly referring to FIG. 3 and FIG. 6, the pad structure 200 includes a first metal layer 210. One end of the first metal layer 210 is electrically connected to the grounding end. Moreover, the other end of the first metal layer 210 is electrically

connected to each of the sub-conductive portions 411 via a first through hole 210a.

[0073] By disposing the first metal layer 210, each of the sub-conductive portions 411 can be electrically connected together simply and conveniently, and are electrically connected to the grounding end. In this case, the first conductive portion 410 of the separated structure is electrically connected to the grounding end, and the second conductive portion 420 of the integrated structure is electrically connected to the power end.

[0074] In an embodiment, referring to FIG. 1, the pad structure 200 may further include a second metal layer 220, a third metal layer 230, and a fourth metal layer 240. The third metal layer 230 is connected to the second metal layer 220 via a third through hole 230a, and the fourth metal layer 240 is connected to the third metal layer 230 via a fourth through hole 240a.

[0075] By disposing the plurality of metal layers, mechanical strength of the pad structure 200 can be effectively improved, so that the pad structure 200 can not be damaged when being electrically connected to the packaging substrate through a wire bonding process.

[0076] Moreover, a shape of an orthographic projection of the second metal layer 220 on the substrate 100 can be set as a ring, and the orthographic projection of the second metal layer 220 on the substrate 100 surrounds the orthographic projection of the capacitor structure 300 on the substrate 100.

[0077] In this case, on the one hand, the ring-shaped second metal layer 220 can ensure the mechanical strength of the pad structure 200, on the other hand, the ring-shaped second metal layer 220 can bear pressure in the wire bonding process, which can effectively prevent the capacitor structure 300 surrounded by the ring-shaped second metal layer 220 from being damaged in the wire bonding process.

[0078] Moreover, the orthographic projection of the third metal layer 230 on the substrate 100 can be coincided with the orthographic projection of the second metal layer 200 on the substrate 100, which further enhances the effect of the second metal layer 230.

[0079] In an embodiment, the pad structure 200 is a power pad. At this time, as stated above, the pad structure 200 (specifically the fourth metal layer 240) can be electrically connected to the packaging substrate via a lead, so as to acquire corresponding power voltage (such as VDDQ, VPP, and VDD).

[0080] Therefore, at this time, the pad structure 200 is configured to input the power voltage to the chip circuit, thus it can be used as a power end of the chip circuit. The fourth metal layer 240 of the pad structure 200 receives a corresponding power signal on the packaging substrate, and inputs the power signal to the chip circuit through the third metal layer 230 and the second metal layer 220 in sequence.

[0081] Also, in the embodiment, the second metal layer 220 is electrically connected to the first metal layer 210 via a second through hole, and further electrically connected to each of the sub-conductive portions 411. Each of the sub-conductive portions 411 are also electrically connected to each of the capacitor devices 311 of the capacitor structure 300.

[0082] Therefore, one end of the capacitor structure 300 can be electrically connected to the pad structure 200 above the capacitor structure 300, so as to stabilize the power supply inputted by the pad structure 200.

[0083] In an embodiment, the pad structure 200 is a grounding pad. In this case, as stated above, the pad structure 200 (the fourth metal layer 240) can be electrically connected to the packaging substrate via a lead, so as to be grounded.

[0084] Therefore, in this case, the pad structure 200 can be used as a grounding end of the chip circuit. The second metal layer 220, the third metal layer 230, and the fourth metal layer 240 of the pad structure 200 are electrically connected in sequence, and are electrically connected to the packaging substrate through the fourth metal layer 240, so as to be grounded.

[0085] Also, in the embodiment, the second metal layer 220 is also electrically connected to the first metal layer 210 via a second through hole, and further electrically connected to each of the sub-conductive portions 411. Each of the sub-conductive portions 411 are also electrically connected to each of the capacitor devices 311 of the capacitor structure 300.

[0086] Therefore, one end of the capacitor structure 300 can be effectively grounded, so as to stabilize the power supply inputted by the power end.

[0087] Of course, in other embodiments, the pad structure 200 can also not be a power pad and/or grounding pad. In this case, the power end and/or grounding end can be disposed in an external circuit outside the pad structure 200.

[0088] Alternatively, when the pad structure 200 is a power pad, the power end can also be disposed in the external circuit outside the pad structure 200. When the pad structure 200 is a grounding pad, the grounding end can also be disposed in the external circuit outside the pad structure 200, which is not limited in the present disclosure.

[0089] It is to be understood that the external circuit outside the pad structure 200 refers to a circuit having no electrical connection relationship with the pad structure 200 in the chip circuit.

[0090] In an embodiment, the capacitor device 311 includes a transistor-type capacitor. Referring to FIG. 7, the gate 10 of the transistor-type capacitor forms the first polar plate 3111 of the capacitor device, and the source and the drain of the transistor-type capacitor and the corresponding parts of the substrate 100 form the second polar plate 3112 of the capacitor device. The first conductive portion 410 of a separated structure is electrically connected to the power end, and the second conductive portion 420 of the integrated structure is electrically connected to the grounding end.

[0091] Referring to FIG. 1, FIG. 2, and FIG. 3, the semiconductor structure may further include a protection ring 500. One end of the protection ring 500 is connected to the substrate 100, the other end of the protection ring 500 is connected to the second conductive portion 420, so as to be grounded through the second conductive portion.

[0092] Moreover, an orthographic projection of the protection ring 500 on the substrate 100 surrounds the orthographic projection of the capacitor structure 300 on the substrate 100. It is to be understood that FIG. 3 is a schematic view of a local structure of the semiconductor structure, so that only the right-side part in FIG. 3 shows the protection ring 500.

[0093] Therefore, in the embodiment, the protection ring 50 may effectively prevent the latch-up effect from occurring in the transistor-type capacitor.

[0094] Also, by disposing the protection ring 500, substrate parts of each of the transistor-type capacitors as the second polar plates 3112 can be electrically connected to the second conductive portion 420 through the protection ring 500 in a unified manner.

[0095] In an embodiment, referring to FIG. 3 and FIG. 8, the capacitor unit 310 includes at least two transistor-type capacitors. The adjacent two transistor-type capacitors in the same

capacitor unit 310 share the source 20 or the drain 30. In this case, when the area is a constant, a relatively larger capacitance value can be generated.

[0096] Of course, the two adjacent transistor-type capacitors can also not share the source or the drain, which is not limited in the present disclosure.

[0097] In description of the specification, description of referring terms such as "some embodiments", "other embodiments" and "an embodiment" refers to that specific features, structures, materials or features described in combination with the embodiments or examples are involved in at least one embodiment or example of the disclosure. In the specification, schematic description on the above terms not always refers to same embodiments or example.

[0098] All the technical features of the above mentioned embodiments can be combined freely. For simplicity of description, not all possible combinations of all the technical solutions in the above mentioned embodiments are described. However, any combination of these technical features shall fall within the scope recorded in the specification without conflicting.

[0099] The above mentioned embodiments only describe some implementation modes of the disclosure and are specifically described in detail, but are not understood as limits to the patent scope of the disclosure. It is to be pointed out that those of ordinary skill in the art may further make various transformations and improvements without departing from the concept of the disclosure and all of these shall fall within the scope of protection of the disclosure. Therefore, the scope of patent protection of the disclosure should be subject to the appended claims.

CLAIMS

1. A semiconductor structure, comprising:

a pad structure disposed above a substrate; and

a capacitor structure disposed between the substrate and the pad structure, and arranged opposite to the pad structure, the capacitor structure comprising at least two capacitor units that are connected in parallel and spaced apart from each other, wherein each of the capacitor units comprises at least one capacitor device;

wherein the capacitor device comprises a first polar plate and a second polar plate that are arranged oppositely, the semiconductor structure further comprises a conductive layer, the conductive layer comprises a first conductive portion and a second conductive portion that are mutually insulated, the first conductive portion is electrically connected to the first polar plate of each of the capacitor devices; the second conductive portion is electrically connected to the second polar plate of each of the capacitor devices; and one of the first conductive portion and the second conductive portion is also electrically connected to a power end, and the other of the first conductive portion and the second conductive portion is also electrically connected to a grounding end;

wherein the second conductive portion is in an integrated structure and spans each of the capacitor devices in the capacitor structure, the first conductive portion is in a separated structure and comprises a plurality of sub-conductive portions that are electrically connected to each other, the sub-conductive portion spans adjacent capacitor devices in the capacitor structure, and orthographic projections of each of the sub-conductive portions on the substrate are spaced apart from an orthographic projection of the second conductive portion on the substrate.

2. The semiconductor structure according to claim 1, wherein an orthographic projection of the capacitor structure on the substrate is within an orthographic projection of the pad structure on the substrate.

3. The semiconductor structure according to claim 2, wherein a center of the orthographic projection of the capacitor structure on the substrate is coincided with a center of the orthographic projection of the pad structure on the substrate.

4. The semiconductor structure according to claim 1, wherein each of the capacitor units comprises at least two capacitor devices that are connected in parallel; the capacitor devices in the capacitor structure is arranged in M-row N-column array, wherein both M and N are integers greater than or equal to 2;

the sub-conductive portion comprises a first sub-portion, and the same sub-portion spans four capacitor devices that are adjacent in pairs and distributed symmetrically around a center.

5. The semiconductor structure according to claim 1, wherein the pad structure comprises a first metal layer, one end of the first metal layer is electrically connected to the power end or the grounding end, and the other end of the first metal layer is electrically connected to each of the sub-conductive portions via a first through hole.

6. The semiconductor structure according to claim 5, wherein the pad structure further comprises a second metal layer, a third metal layer, and a fourth metal layer, the third metal layer is connected to the second metal layer via a third through hole; and the fourth metal layer is connected to the third metal layer via a fourth through hole.

7. The semiconductor structure according to claim 6, wherein an orthographic projection of the second metal layer on the substrate is ring-shaped, and the orthographic projection of the second metal layer on the substrate surrounds an orthographic projection of the capacitor structure on

the substrate.

8. The semiconductor structure according to claim 7, wherein an orthographic projection of the third metal layer on the substrate is coincided with the orthographic projection of the second metal layer on the substrate.

9. The semiconductor structure according to any one of claims 6 to 8, wherein the pad structure is a power pad or a grounding pad, and the second metal layer is electrically connected to the first metal layer via a second through hole.

10. The semiconductor structure according to any one of claims 1 to 8, wherein the power end and/or the grounding end is located in an external circuit outside the pad structure.

11. The semiconductor structure according to claim 1, wherein the capacitor device comprises a transistor-type capacitor, a gate of the transistor-type capacitor forms the first polar plate of the capacitor device, and a source and a drain of the transistor-type capacitor and the substrate form the second polar plate of the capacitor device.

12. The semiconductor structure according to claim 11, wherein the first conductive portion is electrically connected to the power end, and the second conductive portion is electrically connected to the grounding end;

the semiconductor structure further comprises a protection ring, both ends of the protection ring are connected to the substrate and the second conductive portion, respectively, and an orthographic projection of the protection ring on the substrate surrounds an orthographic

projection of the capacitor structure on the substrate.

13. The semiconductor structure according to claim 11, wherein the capacitor unit comprises at least two transistor-type capacitors, and adjacent two transistor-type capacitors in the same capacitor unit share the source or the drain.