CLAIMS

1. A method for detecting and correcting an error in a digital circuit comprising a plurality of logic gates on a path between two flip-flops, receiving an input signal and clocking the input signal with a rising and falling timing signal, the method comprising:

detecting late arrival signal transition of the input signal at an intermediate point of [[a]]the path, the intermediate point of the path being ~~one through which the input signal transits~~an output of one of the plurality of logic gates and an input of a subsequent one of the plurality of logic gates;

predicting an error in the input signal in response to detecting the late arrival signal transition of the input signal at the intermediate point of the path; and

correcting the error in the input signal by manipulating the timing signal and/or a supply voltage.

2. The method according to claim 1, further comprising preventing the error in the input signal by gating the timing signal when it is predicted that there is an error in the input signal.

3. The method according to claim 1, further comprising counting the number and/or frequency of errors in the input signal.

4. The method according to claim 3, further comprising determining if the number and/or frequency of errors in the input signal is above a threshold.

5. The method according to claim 4, wherein correcting the error in the input signal comprises reducing a frequency of the timing signal when it is determined that the number of errors in the input signal is above the threshold.

6. The method according to claim 4, wherein correcting the error in the input signal comprises by reducing a frequency of the timing signal when it is determined that the frequency of errors in the input signal is above the threshold.

7. The method according to claim 5, wherein the frequency of the timing signal is reduced by an adaptive clock and voltage tuning circuit.

8. The method according to claim 6, wherein the frequency of the timing signal is reduced by an adaptive clock and voltage tuning circuit.

9. The method according to claim 5, wherein correcting the error in the input signal comprises increasing the supply voltage when it is determined that the number of errors in the input signal is above the threshold.

10. The method according to claim 6, wherein correcting the error in the input signal comprises increasing the supply voltage when it is determined that the frequency of errors in the input signal is above the threshold.

11. The method according to claim 9, wherein the input voltage is increased by an adaptive clock and voltage tuning circuit.

12. The method according to claim 10, wherein the input voltage is increased by an adaptive clock and voltage tuning circuit

13. A circuit for detecting and correcting an error in a digital circuit receiving an input signal and clocking the input signal with a rising and falling timing signal, the circuit comprising:

a path through which the input signal transits comprising two flip-flops and a plurality of logic gates connected between the two flip-flops;

a means for detecting late arrival signal transition of the input signal at an intermediate point of [[a]] the path, the intermediate point of the path being ~~one through~~ a point at which the input signal ~~transits~~ has transited through at least one of the plurality of logic gates and has yet to transit through at least a subsequent one of the plurality of logic gates;

a means for predicting an error in the input signal in response to detecting the late arrival signal transition at the intermediate point of the path; and

a means for correcting the error in the input signal by manipulating the timing signal and/or a supply voltage.

14. The circuit according to claim 13, wherein the means for correcting the error in the input signal is further configured to prevent the error in the input signal by gating the timing signal when it is predicted that there is an error in the input signal.

15. The circuit according to any of claims 13 or 14, wherein the means for correcting the error in the input signal is further configured to count the number and/or frequency of errors in the input signal.

16. The circuit according to claim 15, wherein the means for correcting the error in the input signal is further configured to determine if the number and/or frequency of errors in the input signal is above a threshold.

17. The circuit according to claim 16, wherein the means for correcting the error in the input signal ~~correcting~~ corrects the error in the input signal comprises by reducing a frequency of the timing signal when it is determined that the number and/or frequency of errors in the input signal is above the threshold.

18. The circuit according to claim 17, further comprising an adaptive clock and voltage tuning circuit configured to reduce the frequency of the timing signal

19. The circuit according to claim 16, wherein the means for correcting the error in the input signal ~~correcting~~ corrects the error in the supply signal ~~comprises~~ by increasing the supply voltage when it ~~is determined~~ determines that the number or frequency of errors in the input signal is above the threshold.

20. The circuit according to claim 19, further comprising an adaptive clock and voltage tuning circuit configured to increase the supply voltage.