CLAIMS

WHAT IS CLAIMED IS:

1. A data backup method of a storage device which includes a storage controller, a buffer memory, and a plurality of nonvolatile memory devices, the method comprising:

detecting a power-off event of an external power provided to the storage device;

deactivating a host interface of the storage controller in response to the detection of the power-off event;

moving data stored in the buffer memory to a cache memory of the storage controller;

blocking or deactivating a power of the buffer memory;

setting an interleaving mode of the plurality of nonvolatile memory devices to reduce power consumption; and

programming the data stored in the cache memory to at least one of the plurality of nonvolatile memory devices.

2. The method of claim 1, wherein, when the power-off event is detected, a device power of the storage device is changed from the external power to a power of an auxiliary power supply.

3. The method of claim 1 or claim 2, wherein, in the deactivating of the host interface, a power of a direct memory access (DMA) engine included in the storage controller is blocked.

4. The method of any one of claims 1 to 3, further comprising:

blocking or deactivating a power of a buffer controller controlling the buffer memory

after the power of the buffer memory is blocked or deactivated.

5. The method of any one of claims 1 to 4, wherein the deactivating of the host interface includes:

deactivating a clock generator generating a clock signal for driving the host interface.

6. The method of any one of claims 1 to 5, wherein, in the setting of the interleaving mode of the plurality of nonvolatile memory devices, a channel or way interleaving unit between the plurality of nonvolatile memory devices and the storage controller is set to a minimum unit of a plurality of interleaving units.

7. The method of claim 6, wherein the data are programmed to a single level cell (SLC) area of a nonvolatile memory device selected by the channel or way interleaving unit.

8. A storage device which includes an auxiliary power supply, comprising:

a power loss prevention circuit for monitoring an external power to detect a power-off event, generating a power-off detection signal when the power-off event is detected, and selecting the auxiliary power supply as a device power when the power-off event is detected;

a plurality of nonvolatile memory devices provided in the storage device;

a buffer memory for temporarily storing data exchanged between the plurality of nonvolatile memory devices and a host; and

a storage controller,

wherein, in response to the power-off detection signal, the storage controller moves data stored in the buffer memory to a working memory of the storage controller,

wherein the storage controller deactivates a host interface and then blocks or deactivates

a power of the buffer memory after the data has been moved from the buffer memory, and

wherein the storage controller programs the data stored in the working memory to at least one of the plurality of nonvolatile memory devices.

9. The storage device of claim 8, wherein the storage controller includes:

a central processing unit for performing a backup operation in response to the power-off detection signal;

a buffer controller for controlling the buffer memory in response to the central processing unit; and

a flash interface connected with the plurality of nonvolatile memory devices in channel units and accessing the plurality of nonvolatile memory devices in a channel or way interleaving manner,

wherein, after the data are moved from the buffer memory, the central processing unit blocks or deactivates a power of the buffer controller.

10. The storage device of claim 9, wherein the storage controller further includes:

a direct memory access (DMA) engine for controlling a DMA operation with the host, and

wherein the central processing unit deactivates the DMA engine together with the host interface.

11. The storage device of claim 9 or claim 10, wherein the host interface further includes:

a clock generator for providing a clock signal for communication with the host, and

wherein the central processing unit turns off the clock generator and deactivates the host

interface.

12. The storage device of any one of claims 9 to 11, wherein the flash interface changes an interleaving mode to reduce power consumption in the backup operation.

13. The storage device of claim 12, wherein, in the changed interleaving mode, the flash interface programs the data to a single level cell (SLC) area of the plurality of nonvolatile memory devices.

14. The storage device of claim 12 or claim 13, wherein, in the changed interleaving mode, a power of unselected nonvolatile memory devices is blocked or deactivated.

15. A data backup method of a storage device which performs data backup by using an auxiliary power supply when a power-off event occurs, the method comprising:

deactivating a host interface of a storage controller in response to the power-off event;

moving data stored in a buffer memory to a static random access memory (SRAM);

changing an interleaving mode of a nonvolatile memory device to reduce power consumption, from among a plurality of interleaving modes for accessing the nonvolatile memory device; and

programming the data stored in the SRAM to the nonvolatile memory device depending on the changed interleaving mode.

16. The method of claim 15, wherein, in the deactivating of the host interface, a power of a direct memory access (DMA) engine included in the storage controller is blocked.

17. The method of claim 15 or claim 16, wherein, in the deactivating of the host interface, a clock generator generating a clock signal for driving the host interface is deactivated.

18. The method of any one of claims 15 to 17, further comprising:

blocking or deactivating a power of the buffer memory or a buffer controller for controlling the buffer memory after the backup data are completely moved to the storage controller.

19. The method of any one of claims 15 to 18, wherein the backup data are programmed to a single level cell (SLC) area of the nonvolatile memory device.