

Description

Title of Invention: BONDING METHOD AND BONDING DEVICE USE METHOD

Technical Field

[0001] The present invention relates to a bonding method and a method using a bonding device, in particular, to a bonding method and a method using a bonding device, each for manufacturing a board-on-chip (BOC) type electronic component (semiconductor device).

Background Art

[0002] Electronic components include a board-on-chip (BOC) type electronic component. Specifically, examples of the BOC-type electronic component include a semiconductor package illustrated in FIG. 9. The semiconductor package includes a substrate 1. The substrate 1 has one surface serving as a pattern formation surface 1a and another surface serving as a chip joining surface 1b. Substrate-side electrodes on the pattern formation surface 1a and chip-side electrodes of a chip 4, which is joined to the chip joining surface 1b, are connected to each other with use of wires 5 through slit holes (through holes) 3 formed in the substrate 1.

[0003] In FIG. 9, solder balls 6 are formed on the pattern formation surface 1a. An adhesion layer 7 is provided so as to join the chip joining surface 1b of the substrate 1 and the chip

4 to each other. Further, the chip 4 and the wires 5 are sealed with a sealing body 8.

[0004] Thus, the electronic component described above needs a step (bonding step) of joining the chip 4 to the chip joining surface 1b of the substrate 1. An ordinary related-art bonding method in such a case is described with reference to FIG. 8.

[0005] After the substrate 1 is held at a predetermined position under a state in which the pattern formation surface 1a including the electrodes on the substrate 1 side (substrate-side electrodes) is directed upward, the chip 4 is placed on an upper surface of a movable stage 10 so that the electrodes on the chip 4 side (chip-side electrodes) are directed upward. The movable stage 10 is moved to a position below the substrate 1, and the chip 4 is brought into contact with the chip joining surface 1b (lower surface at this time) of the substrate 1, which is opposite to the pattern formation surface 1a, from below (arrow A shown in FIG. 8). Subsequently, a thermocompression bonding tool 11 presses the substrate 1, from above the substrate 1 (arrow B shown in FIG. 8), against the chip 4 placed on the movable stage 10 to thereby join the chip 4 to the substrate 1. According to such a method, the pattern formation surface 1a of the substrate 1 and an electrode formation surface 4a of the chip 4 can be recognized from above with cameras (a substrate-side recognition camera 12 that allows recognition of the pattern formation surface 1a of the substrate 1, and a chip-side recognition camera

13 that allows recognition of the electrode formation surface 4a
of the chip 4). Thus, the chip 4 is aligned with the substrate
1. As illustrated in FIG. 8, the pattern formation surface 1a
has a substrate-side pattern (substrate-side electrode portions)
14.

[0006] With the above-mentioned bonding method, after the
chip is picked up via a pickup arm, it is required that the chip
be transferred onto a bonding arm with a suction surface directed
upward. Under this state, it is required that the electrode
formation surface 4a of the chip 4 be recognized and the chip be
joined to the chip joining surface of the substrate, which is
directed downward. In this case, an adhesive on a back side of
the substrate is heated, and a load is applied from each of the
bonding arm, arranged below the substrate, and the pattern
formation surface of the substrate, and thus the chip is
sandwiched between the bonding arm and the pattern formation
surface to thereby be joined to the chip joining surface.

[0007] For the method of performing bonding from a position
below the substrate as described above, however, a commonly used
general-purpose bonding device (device for performing bonding
from above a substrate) cannot be used.

[0008] Thus, in the related art, there have been proposed
a die bonding device and a die bonding method, which use a
related-art type die bonding device to enable a die bonding step
for a BOC-type electronic component (Patent Literature 1).

[0009] The die bonding device (method) described in Patent Literature 1 joins a chip to a chip joining surface (surface opposite to a pattern formation surface) of a substrate while the chip joining surface is directed upward. In this case, the chip is picked up from a wafer with use of a reversing tool, and the thus picked-up chip is reversed by the reversing tool. In this manner, an electrode formation surface of the chip is turned and directed downward. After that, a transfer tool sucks a counter-electrode formation surface of the chip from above. Under this state, the electrode formation surface of the chip is directed downward. Thus, the electrode formation surface of the chip can be joined, from above, to a chip joining surface (surface opposite to the pattern formation surface) of the substrate, which is directed upward.

[0010] According to Patent Literature 1, the pattern formation surface (downwardly directed surface) of the substrate is observed with a camera arranged thereabove. Specifically, a mirror member is provided on a substrate placement table on which the substrate is to be placed while a transparent member is interposed between the mirror member and the substrate placement table, and a reflected image on a mirror surface of the mirror member is viewed. In this case, the reflected image is reflected on the mirror surface through a wire insertion hole formed in the substrate and the transparent member.

[0011] Then, the substrate and the chip are aligned with

each other based on a position of a substrate-side pattern in the reflected image, and then the electrode formation surface of the chip is joined to the chip joining surface of the substrate.

Citation List

[0012] Patent Literature 1: JP 2009-200203 A

Summary of Invention

Technical Problem

[0013] However, the die bonding device and the die bonding method described in Patent Literature 1 use the reflected image. When the reflected image is used, the reflected image is obtained through the wire insertion hole and the transparent member. Thus, there are problems in that, for example, an observation range is limited and an accurate reflected image cannot be obtained when the mirror surface has low accuracy. In addition, the reflected image is acquired in an area where the substrate is heated. Thus, the acquisition of the reflected image is affected by a gas that is generated when the adhesive melts. The gas may be accumulated on the mirror and may cause, for example, fogging of the mirror. Accordingly, the image is not acquired stably.

[0014] The device described in Patent Literature 1 requires the substrate placement table on which the transparent member and the mirror member are provided. The use of the member (substrate placement table on which the transparent member and

the mirror member are provided) that is required to be formed with high accuracy as a whole device is required. When a size of the wire insertion hole formed in the substrate or a width of the substrate is changed, the substrate placement table on which the transparent member and the mirror member are provided is required to be replaced. Thus, productivity is poor.

[0015] Thus, in view of the problems described above, the present invention provides a bonding method and a method using a bonding device, which enable stable alignment and allow use of an existing bonding device as a device to be used.

Solution to Problem

[0016] According to the present invention, there is provided a bonding method which involves conveying a substrate, which has a wire insertion hole passing therethrough in a thickness direction of the substrate and has fiducial marks for alignment formed on a pattern formation surface, conveyed from an upstream side to a downstream side along a substrate conveyance path and joining, at a bonding position on a downstream side in a substrate conveyance path, an electrode formation surface of a chip onto a chip joining portion of a chip joining surface, which is located on a side opposite to a substrate-side electrode portion of a pattern formation surface of the substrate. The bonding method comprises: a substrate recognition step of recognizing a positional relationship among

the fiducial marks for alignment and the wire insertion hole from below on the upstream side in the substrate conveyance path under a state in which the substrate is disposed with the pattern formation surface directed downward; a pickup step of picking up the chip with use of a pickup-side collet; a reversing step of reversing the chip picked up by the pickup-side collet so that the electrode formation surface of the chip is directed downward; a receiving step of receiving the chip, which has been reversed in the reversing step, while the electrode formation surface is kept directed downward, with use of a bonding-side collet; an alignment step of aligning the chip and the chip joining portion of the substrate based on the positional relationship among the fiducial marks for alignment and the wire insertion hole, which has been recognized in the recognition step, and recognition of a position of the wire insertion hole, which is performed from above the bonding position; and a joining step of joining, at the bonding position on the downstream side in the substrate conveyance path, the chip, which has been received in the receiving step, to the chip joining portion of the substrate, which has been aligned in the alignment step.

[0017] According to the bonding method of the present invention, in the substrate recognition step, the positional relationship among the fiducial marks for alignment and the wire insertion hole can be recognized based on a direct image of the pattern formation surface, which has been observed from below.

In the pickup step, the chip can be picked up. In the reversing step, the chip, which has been picked up, can be brought into a state in which the chip electrode formation surface is directed downward. In the receiving step, the chip can be received by the bonding-side collet while the electrode formation surface is kept directed downward. In the alignment step, the alignment can be performed based on the positional relationship among the fiducial marks for alignment and the wire insertion hole and the recognition of the position of the wire insertion hole, which has been performed from above the bonding position. In the joining step, the chip, which has been received in the receiving step, can be joined to the chip joining portion of the substrate aligned in the alignment step.

[0018] In the substrate recognition step, the pattern formation surface of the substrate, which is directed downward, can be observed from below the substrate. Thus, an observed surface is not an indirect image. Hence, a field of view for observation is not restricted, and the positional relationship among the fiducial marks for alignment and the wire insertion hole can be stably observed with high accuracy. In addition, the image is observed on the upstream side in the substrate conveyance path, which is an unheated area. Thus, a heater (for example, an electric heater provided to a backup plate) can be arranged on the downstream side in the substrate conveyance path without being disturbed by, for example, cameras that are used

in the substrate recognition step. Specifically, a substrate recognition area and a substrate heating area can be arranged at separate positions. In the substrate recognition area, there is no influence of heating of the substrate (for example, influence on the optical system, which may be caused by a gas or the like generated when the adhesive melts). In the substrate heating area, the wire insertion hole of the substrate is recognized from above. However, the substrate recognition is not performed at a position close to the substrate. Thus, the substrate can be continuously heated. Further, in the joining step of joining the chip, the chip can be brought from a position above the substrate. This bonding method can be used for ordinary face-up bonding (a case in which the electrode surface of the chip is to adhere).

[0019] Further, in the bonding method, the adhesive configured to join the chip and the chip joining surface of the substrate is provided on the chip joining surface in an upwardly directed state. Thus, even when the adhesive has relatively high fluidity, there is no risk of dripping downward. Thus, application work for the adhesive is easy. In addition, various adhesives can be used as the adhesive, which contributes to a reduction in cost.

[0020] In particular, the alignment is performed based on: the recognition of the positional relationship among the fiducial marks for alignment and the wire insertion hole, which

is performed at a position on the upstream side, the position being separate from the bonding position; and the recognition of the position of the wire insertion hole, which is performed from above the bonding position. Thus, the alignment with high accuracy is enabled. Specifically, the positional relationship among the fiducial marks and electrodes on the pattern formation surface is set with high accuracy. Thus, when the position of the wire insertion hole is checked from the joining surface side (counter-pattern formation surface side) of the chip, the positions of the electrodes (substrate-side electrode portion) on the pattern formation surface can be detected from the positional relationship among the fiducial marks and the wire insertion hole. Thus, precise bonding and joining onto the chip joining portion on the chip joining surface of the substrate are enabled. In this case, the chip joining portion is an area corresponding to the substrate-side electrode portion.

[0021] The bonding method may further comprise a chip recognition step of performing position recognition for the chip before bonding. As described above, when the chip recognition step is provided, improvement in alignment accuracy can be achieved.

[0022] In the joining step, the substrate may be received by a backup plate from below. As described above, when the substrate is received by the backup plate from below and the chip is joined to the chip joining surface of the substrate, the

chip can be sandwiched between the bonding-side collet and the backup plate. Thus, stable joint can be obtained without, for example, curving the substrate.

[0023] Further, the backup plate may be configured to be heated by a heater so as to heat an adhesive on the substrate. With the configuration described above, the heater is not required to be provided as an additional member, which contributes to downsizing of the device as a whole.

[0024] It is preferred that positional information for one substrate be acquired in the substrate recognition step. With the configuration described above, the chips can be continuously joined to all the chip joining portions of one substrate in the bonding step. Thus, productivity can be improved.

[0025] According to the present invention, there is provided a method using a bonding device configured to pick up a chip at a pickup position with use of a pickup-side collet, reverse the chip picked up at the pickup position, and bond the reversed chip at a bonding position with use of a bonding-side collet. The method enables the above-mentioned bonding method.

[0026] An existing general-purpose bonding device can be used for the method using a bonding device according to the present invention. Thus, a reduction in cost can be achieved.

Advantageous Effects of Invention

[0027] According to the present invention, the pattern

formation surface is observed not based on an indirect image. Thus, the field of view for observation is not restricted, and the pattern formation surface can be stably observed with high accuracy. Accordingly, the chips can be stably joined to the substrate with high accuracy. Further, the chips can be joined to the substrate at low cost without complicating a device configuration. Further, in the joining step of joining the chip, the chip can be brought from above the substrate. This bonding method can be used for ordinary face-up bonding (a case in which an electrode surface of the chip is to be adhered).

Brief Description of Drawings

[0028] FIG. 1 is a schematic perspective view of a bonding device to be used for a bonding method according to the present invention.

FIG. 2 is a schematic enlarged view of a main part of a pattern formation surface of a substrate.

FIG. 3A is a schematic view of a chip joining portion of a chip joining surface.

FIG. 3B is a schematic view for illustrating the substrate under a state in which adhesives are applied onto the chip joining portion of the chip joining surface.

FIG. 4 is a schematic plan view for illustrating a conveying mechanism for the substrate.

FIG. 5 is a block diagram for illustrating the bonding

method according to the present invention.

FIG. 6 is a flowcharts for illustrating steps in a first half of the bonding method according to the present invention.

FIG. 7 is a flowcharts for illustrating steps in a second half of the bonding method according to the present invention.

FIG. 8 is a perspective view for illustrating a related-art bonding method.

FIG. 9 is a sectional view of a semiconductor device (BOC-type semiconductor package).

Description of Embodiments

[0029] Now, description is made of embodiments of the present invention with reference to FIG. 1 to FIG. 7.

[0030] In FIG. 1, a bonding device to be used for a bonding method according to the present invention is illustrated. This bonding device enables implementation of a bonding method of joining an electrode formation surface 32a of a chip 32 onto a chip joining portion 34 of a chip joining surface 31b of a substrate 31, which is located on a side opposite to a substrate-side electrode portion 38 of a pattern formation surface 31a of the substrate 31.

[0031] A plurality of wire insertion holes 33, each being an elongated hole extending in a width direction of the substrate, are formed in the substrate 31. In this case, the plurality of wire insertion holes 33 are arranged in the width direction of

the substrate to form a wire insertion hole group 35. A plurality of wire insertion hole groups 35 are arranged at predetermined intervals in a longitudinal direction of the substrate.

[0032] As illustrated in FIG. 2, the substrate-side pattern (substrate-side electrode portion) 38 is formed on the pattern formation surface 31a of the substrate 31. The substrate-side pattern 38 includes comprises substrate-side electrodes 36 and pads 37 arranged on both sides of the wire insertion hole 33. Further, as illustrated in FIG. 3B, adhesives S are provided (applied) onto the chip joining portion 34 of the chip joining surface 31b (surface opposite to the pattern formation surface 31a) of the substrate 31. In this case, for one wire insertion hole 33, a pair of adhesives S, S are applied such that the wire insertion hole 33 is located therebetween. The adhesive S may be a paste type adhesive or a die attach film (DAF).

[0033] Fiducial marks 40 for alignment (see FIG. 3A) are formed on the pattern formation surface 31a of the substrate 31. In this embodiment, each of the fiducial marks 40 for alignment (hereinafter also referred to simply as "fiducial marks 40") is defined by a corner portion of a metal film formed on the pattern formation surface 31a of the substrate 31. However, the fiducial mark 40 is not limited to the above-mentioned one, and may be a mark such as a colored mark or a recessed or protruding portion, which is specially provided.

[0034] The substrate 31 is conveyed by a substrate conveyor 41 as illustrated in FIG. 4 in a direction indicated by an arrow X of FIG. 1. The substrate conveyor 41 comprises a pair of conveyance rails 42, 42. The substrate 31 placed on the conveyance rails 42, 42 is conveyed by a feeding mechanism comprising a gripping mechanism (not shown; for example, a chuck mechanism) from an upstream side to a downstream side in the direction indicated by the arrow X.

[0035] Further, a backup plate (adapter plate) 43 is disposed between the conveyance rails 42, 42 so as to be located below a bonding position on a downstream side in a conveyance path for the substrate 31. The backup plate 43 can be heated by a heater (not shown). Specifically, when the backup plate 43 is heated, the adhesives S on the chip joining surface 31b of the substrate 31, which correspond to the bonding position, can be heated. Various types of electric heating systems can be used as the heater (not shown).

[0036] It is preferred that the backup plate 43 to be heated by the heater be set as follows. A center portion of the backup plate 43 in a substrate conveying direction forms a joint-temperature zone in which the substrate 31 can be heated to a temperature at which the adhesives S melt to provide an effective joining force during bonding. An upstream-side portion and a downstream-side portion with respect to the center portion in the substrate conveying direction form low-temperature heating

zones in which heating to a temperature lower than the heating temperature in the joint-temperature zone can be achieved. By the setting described above, the joint-temperature zone can cover the bonding position. Further, when the chip joining portion 34 of the substrate 31 is located at the bonding position, the chip joining portion 34 of the substrate 31 can be heated to a temperature that allows the adhesives S to provide an effective joining force. In addition, before the chip joining portion 34 of the substrate 31 is located at the bonding position, the chip joining portion 34 passes over the low-temperature heating zone. Thus, the chip joining portion 34 of the substrate 31 can be preliminarily heated. As a result, improvement in work efficiency can be achieved.

[0037] Further, the bonding device comprises, for example, a pickup mechanism 50, a bonding mechanism 51, and an observation part 53. The pickup mechanism 50 is configured to pick up the chip 32 being a workpiece. The bonding mechanism 51 is configured to join the chip 32, which has been picked up by the pickup mechanism 50, to the chip joining portion 34 of the chip joining surface 31b of the substrate 31. The observation part 53 is configured to allow the pattern formation surface 31a on the back side of the substrate 31 to be observed from below on the upstream side in the substrate conveyance path.

[0038] The chips 32 are formed of a wafer material. The wafer material is cut into rectangular shapes so that the chips

32 are obtained as final products. Thus, examples of the chip 32 include a square one and a strip-shaped one. Specifically, the wafer has a circular shape as a whole, and is divided into individual chips 32 by dicing.

[0039] The pickup mechanism 50 comprises a pickup head 56. A pickup arm 55 is provided on a distal end side of the pickup head 56. A collet 57 is mounted to a distal end of the pickup arm 55. A plurality of suction holes (not shown) are formed in the distal end surface of the collet 57 so as to be opened thereon. The chip 32 is vacuum sucked through the suction holes, and the chip 32 is sucked onto the distal end surface of the collet 57. When the vacuum suction (evacuation) is released, the chip 32 is separated from the collet 57. Further, the vacuum suction (evacuation) is performed in a vacuum mechanism (not shown). As the vacuum mechanism, for example, a vacuum pump or a vacuum ejector is used.

[0040] Further, the pickup head 56 comprises a reversing mechanism 58 and can reverse the collet 57 mounted to the distal end of the pickup arm 55. The reversing mechanism 58 comprises a drive mechanism (for example, a motor) that turns the pickup head 56 about its axis. The reversing mechanism 58 can change a posture of the pickup arm 55 so that the distal end surface being the suction surface of the collet 57 is directed downward and so that the distal end surface being the suction surface of the collet 57 is directed upward. Further, the pickup head 56

of the pickup mechanism 50 can be moved upward and downward by an upward and downward movement mechanism (not shown) as indicated by arrows Z1 and Z2. The upward and downward movement mechanism may be formed of various reciprocation mechanisms such as a cylinder mechanism, a ball screw mechanism, and a linear motor mechanism. The pickup mechanism 50 can be moved in directions indicated by arrows X3 and X4 and arrows Y1 and Y2 so as to correct a position of the collet 57 based on a recognition unit (recognition part) (not shown) configured to recognize the chip 32 and located above the wafer. The arrows X3 and X4 represent reciprocating movement in directions parallel to the longitudinal direction of the substrate 31 (direction in which the substrate is conveyed), and the arrows Y1 and Y2 represent reciprocating movement in directions orthogonal to the directions indicated by the arrows X3 and X4.

[0041] The bonding mechanism 51 comprises a bonding head 60. A collet 62 is mounted to a distal end of a bonding arm 61. A plurality of suction holes (not shown) are formed in the lower surface (distal end surface) of the collet 62 so as to be opened on the distal end surface. The chip 32 is vacuum sucked through the suction holes, and the chip 32 is sucked onto the distal end surface of the collet 62. When the vacuum suction (evacuation) is released, the chip 32 is separated from the collet 62. Further, the vacuum suction (evacuation) is performed in a vacuum mechanism (not shown). As the vacuum mechanism, for example, a

vacuum pump or a vacuum ejector is used.

[0042] Further, the bonding head 60 can be moved in the directions indicated by arrows X1 and X2 corresponding to the longitudinal direction of the substrate 31, the directions indicated by arrows A and B corresponding to the width direction, and directions indicated by arrows C and D corresponding to up-and-down directions, via a movement mechanism (not shown). The movement mechanism may be formed of various reciprocation mechanisms such as a cylinder mechanism, a ball screw mechanism, and a linear motor mechanism.

[0043] The observation part 53 comprises a camera mechanism 65 arranged below the upstream side in the substrate conveyance path. Specifically, the camera mechanism 65 comprises a camera main body 66 and an optical system 67. The camera main body 66 is formed of an image recognition camera (for example, a CCD camera or a CMOS camera). The optical system 67 is configured to define a field of view of an image for the camera main body 66. The optical system 67 in this case comprises a mirror member 68 configured to allow an image of the pattern formation surface 31a of the substrate within a predetermined field of view to enter the camera main body 66. A field of view for observation by the observation part 53 is a range indicated by a double-dotted line.

[0044] Further, the bonding device comprises an insertion-hole recognition part 71 arranged above the bonding position for

the chip 32. The insertion-hole recognition part 71 is configured to recognize the wire insertion hole 33 of the substrate 31. Further, a first chip recognition part 72 is arranged above the pickup mechanism 50. The first chip recognition part 72 is configured to check the chip 32, which has been picked up by the pickup mechanism 50 and is in a reversed state. A second chip recognition part 73 is provided on the bonding mechanism 51 side. The second chip recognition part 73 is configured to recognize the chip 32 that is sucked and held onto the bonding-side collet 62.

[0045] The insertion-hole recognition part 71 and the first chip recognition part 72 may be each formed of, for example, a CCD camera or a CMOS camera. Further, the second chip recognition part 73 comprises a camera main body 74 and an optical system 75. The camera main body 74 is formed of an image recognition camera (for example, a CCD camera or a CMOS camera). The optical system 75 is configured to define a field of view of an image for the camera main body 74. The optical system 75 in this case comprises a mirror member 76 configured to allow an image of the chip 32 to enter the camera main body 74.

[0046] Position recognition for the chip 32 before bonding, that is, chip recognition steps 87 and 88 described later can be implemented through the observation of the chip 32 by the first chip recognition part 72 and the observation of the chip 32 by the second chip recognition part 73. Specifically, the first

chip recognition part 72 performs position recognition for the chip 32 sucked onto the pickup-side collet 57, and the second chip recognition part 73 performs position recognition for the chip 32 sucked onto the bonding-side collet 62. The position recognition described above is used for alignment performed when the chip 32 is bonded.

[0047] The substrate conveyor 41, the pickup mechanism 50, and the bonding mechanism 51 are controlled by a computer (not shown). In this case, the computer basically comprises an input part having an input function, an output part having an output function, a storage part having a storing function, a calculation part having a calculating function, and a controller having a control function.

[0048] The input function enables information from an outside to be read into the computer. The read data and program are converted into signals in a format suitable for a computer system. The output function enables, for example, a result of calculation and stored data to be displayed on the outside. The storage part stores and saves, for example, a program, data, and a result of processing. The calculating function enables processing of data through a calculation or comparison in accordance with a command in the program. The control function enables the command in the program to be deciphered and an instruction to be issued to each of the parts. The control function enables overall control of all the parts of the computer.

Examples of the input part include a keyboard, a mouse, a tablet, a microphone, a joystick, a scanner, and a capture board. Further, examples of the output part include a monitor, a speaker, and a printer. Examples of the storage part include a memory, a hard disk, a CD, a CD-R, a PD, and an MO. Examples of the calculation part include a CPU, and examples of the control part includes a CPU and a motherboard.

[0049] Next, description is made of a bonding method of joining the electrode formation surface 32a of the chip 32 onto the chip joining portion 34 of the chip joining surface 31b of the substrate 31, which is located on the side opposite to the substrate-side electrode portion 38 of the pattern formation surface 31a, with use of the bonding device having the configuration described above. In this case, the chip joining portion 34 corresponds to the substrate-side electrode portion 38 on the opposite side. As illustrated in FIG. 5, this bonding method comprises a substrate recognition step 81, a pickup step 82, a reversing step 83, a receiving step 84, an alignment step 85, and a joining step 86. Further, in this embodiment, a first chip recognition step 87 is provided between the reversing step 83 and the receiving step 84, and a second chip recognition step 88 is provided between the receiving step 84 and the alignment step 85.

[0050] In the substrate recognition step 81, a position of the substrate-side pattern of the pattern formation surface 31a

is recognized based on a direct image of the pattern formation surface 31a, which is observed from below, under a state in which the substrate 31 is disposed with the pattern formation surface 31a directed downward. In the pickup step 82, the chip 32 is picked up via the pickup-side collet 57. In the reversing step 83, the chip 32, which has been picked up by the pickup-side collet 57, is reversed so that the electrode formation surface 32a is directed downward. In the receiving step 84, the chip 32, which has been reversed in the reversing step 83, is received by the bonding-side collet 62 while the electrode formation surface 32a is kept directed downward. In the alignment step 85, the substrate 31 and the chip 32 received in the receiving step 84 are aligned with each other based on the position of the substrate-side pattern (substrate-side electrode portion 38) of the pattern formation surface 31a, which has been recognized in the recognition step 81. In the joining step 86, the chip 32, which has been aligned with the substrate 31 in the alignment step, is joined to the chip joining portion 34 of the chip joining surface 31b of the substrate 31 with use of the bonding-side collet 62.

[0051] In the first chip recognition step 87, the chip 32, which is sucked onto the pickup-side collet 57 in a state in which counter-chip-side electrodes are directed upward, is observed from above with use of the first chip recognition part 72. In the second chip recognition step 88, the chip 32, which

is sucked onto the bonding-side collet 62 in a state in which the electrode formation surface 32a is directed downward, is observed from below with use of the second chip recognition part 73.

[0052] Next, the bonding method comprising the steps 81, 82, 83, 87, 84, 88, 85, and 86 is described with reference to flowcharts of FIG. 6 and FIG. 7. First, the substrate is arranged on the upstream side in the substrate conveyance path under a state in which the pattern formation surface 31a is directed downward. Under this state, the substrate recognition step 81, that is, substrate recognition is implemented (Step S1). In this case, the wire insertion holes 33 are not generally formed with high accuracy. Thus, the positions of the wire insertion holes 33 are recognized based on the fiducial marks provided on the pattern formation surface 31a as references. In this case, positional information of the chip joining portions 34 on one substrate 31 is acquired. Specifically, the positions of all the wire insertion holes 33 are checked. This positional information is stored in the storage part of the computer.

[0053] Next, the pickup step is carried out, that is, the chip 32 is picked up at a pickup position by the pickup mechanism 50 (Step S2). Specifically, the pickup-side collet 57 located above the pickup position is moved downward as indicated by the arrow Z2 of FIG. 1 so that one chip 32 is sucked onto the collet 57, and then the collet 57 is moved upward as indicated by the

arrow Z1 of FIG. 1. In this manner, the chip 32 can be picked up.

[0054] After that, the reversing step 83 is carried out. Specifically, the chip 32 is reversed by reversing the pickup head 56 of the pickup mechanism 50 by 180 degrees (Step S3). In this case, the reversing may be performed either in a clockwise manner or in a counterclockwise manner. In this case, the electrode formation surface 32a of the chip 32 is directed downward.

[0055] Next, the procedure proceeds to Step S4 where determination is made on whether or not to perform the position recognition for the chip 32. When it is determined in Step S4 not to perform the position recognition, the procedure proceeds to Step S5 where the receiving step of receiving the chip 32 that has been reversed is carried out. When it is determined in Step S4 to perform the position recognition, the procedure proceeds to Step S6 where the position recognition for the chip 32 is performed. Specifically, an image of the chip 32 is captured by the first chip recognition part 72, and the position of the chip 32 is checked.

[0056] In Step S5, the chip 32 that has been reversed is received by the bonding mechanism 51. Specifically, the bonding-side collet 62 is located above the chip 32 that has been reversed, and the chip 32 is sucked onto the collet 62. At this time, the suction by the pickup-side collet 57 is released. As

a result, the chip 32 is sucked onto the suction surface, which is the lower surface of the bonding-side collet 62. In this case, the electrode formation surface 32a of the chip 32 is directed downward.

[0057] After that, the procedure proceeds to Step S7 of FIG. 7. In Step S7, determination is made on whether or not to perform the position recognition for the chip 32. When it is determined in Step S7 not to perform the position recognition, the procedure proceeds to Step S8. When it is determined in Step S7 to perform the position recognition, the procedure proceeds to Step S9 where the position recognition is performed. After that, the procedure proceeds to Step S8. When it is determined in Step 7 to perform the position recognition, an image of the chip 32 is captured by the second chip recognition part 73, and the position of the chip 32 is checked.

[0058] In Step S8, the substrate 31 and the chip 32 are aligned with each other. In this case, the substrate 31 is conveyed by the substrate conveyor 41 from the upstream side to the downstream side through the substrate conveyance path so that the chip joining portion 34 of the substrate 31, onto which the chip 32 is to be joined, is located above the bonding position.

[0059] In Step S8, the chip 32 and the chip joining portion 34 are aligned with each other based on: a relationship among the fiducial marks 40 on the pattern formation surface 31a and

the wire insertion hole 33 in the pattern formation surface 31a of the substrate 31; and the recognition of the position of the wire insertion hole 33 in the substrate 31, which has been checked by the insertion-hole recognition part 71. In this case, the wire insertion hole 33 in the chip joining portion onto which the chip 32 is to be bonded is recognized by the insertion-hole recognition part 71. Then, the positional relationship among the fiducial marks 40 and the wire insertion hole 33, which has been recorded, and the wire insertion hole 33 of the chip joining portion 34, which has been recognized by the insertion-hole recognition part 71, are compared with each other. In this case, the position of the wire insertion hole 33 differs for each chip joining portion 34 with respect to the fiducial marks 40 that are formed with high accuracy in accordance with intervals between islands (chip joining portions 34). Thus, a positional shift (positional shift between the wire insertion hole 33 that has been recognized by the recognition part 71 and the fiducial marks 40) may occur. Accordingly, the fiducial marks 40 on the substrate 31 and the positions of the electrodes of the chip 32 (or a position of an outline of the chip 32) are required to be aligned with each other through the wire insertion hole 33 checked by the recognition part 71 based on a positional shift amount recognized by the recognition part 71. There may be some cases in which no positional shift occurs. When no positional shift occurs, alignment is not required to be performed.

[0060] In this embodiment, the position recognition for the chip 32 can be performed in the first chip recognition step 87 and the second chip recognition step 88 before bonding. Thus, positional information of the chip 32 before bonding, which has been detected in the chip recognition steps 87 and 88, can be used for the alignment. In this manner, alignment with higher accuracy is enabled. Specifically, the positional information obtained in the first chip recognition step 87 and the second chip recognition step 88 is input to the computer. A positional shift is calculated in consideration of such information, and the alignment is performed.

[0061] The positional shift may occur in the longitudinal direction of the substrate 31, in the width direction of the substrate 31, and in both the longitudinal direction and the width direction. When the positional shift occurs in the longitudinal direction, the position of the bonding-side collet 62 is only required to be displaced in the directions indicated by the arrows X1 and X2. When the positional shift occurs in the width direction, the position of the bonding-side collet 62 is only required to be displaced in the directions indicated by the arrows A and B. When the positional shift occurs in the longitudinal direction and in the width direction, the position of the bonding-side collet 62 is only required to be displaced in the directions indicated by the arrows X1, X2, A, and B.

[0062] In Step S10, the chip 32 is bonded in an aligned

state. In this case, after the bonding-side collet 62, which has received the chip 32 from the pickup-side collet 57, is moved upward as indicated by the arrow C, the bonding-side collet 62 is moved so as to be located above the chip joining portion, as indicated by the arrow A. After that, the bonding-side collet 62 is moved downward to achieve joint. The alignment can be performed while the bonding-side collet 62 is operating. However, the alignment may be performed after the checking of the position of the chip 32 in a state of being sucked onto and reversed by the collet 57 is finished, or may be performed after the checking of the position of the chip 32 in a state of being sucked onto the collet 62 is finished.

[0063] Further, during the bonding step, the backup plate 43 is heated, and the adhesive has an increased temperature that allows joint. Thus, the collet 62 is moved downward, and the substrate 31 is sandwiched between the collet 62 and the backup plate 43. Thus, the chip 32 is joined via the adhesives S. As described above, when the chip 32 is bonded onto the chip joining portion 34, the alignment step enables the electrode formation surface 32a of the chip 32 to be precisely joined to the chip joining portion 34 of the chip joining surface 31b of the substrate 31.

[0064] After that, the procedure proceeds to Step S11 where determination is made on whether or not to terminate this process (work). When it is determined to terminate the process, the

process is terminated. When it is determined in Step S11 not to terminate the process, the procedure returns to Step S2. As described above, when the process from Step S2 to Step S10 is carried out, the chips can be joined to all the chip joining portions of one substrate 31.

[0065] In the substrate recognition step 81, the pattern formation surface 31a of the substrate 31, which is directed downward, can be observed from below the substrate 31. Thus, the pattern formation surface 31a can be observed not based on an indirect image. Hence, a field of view for observation is not restricted, and the pattern formation surface 31a can be stably observed with high accuracy. In addition, the image is observed on the upstream side in the substrate conveyance path, which is an unheated area. Thus, a heater (for example, the heater provided to the backup plate) can be arranged on the downstream side in the substrate conveyance path without being disturbed by, for example, the cameras that are used in the substrate recognition step. Specifically, a substrate recognition area and a substrate heating area can be arranged at separate positions. Thus, the positional relationship among the fiducial marks 40 for alignment and the wire insertion hole 33 can be recognized in the area where the substrate 31 is not heated. Thus, in the substrate recognition area, there is no influence of the heating of the substrate (for example, influence on the optical system, which is caused by a gas or the like

generated when the adhesive melts). In the substrate heating area, the wire insertion hole 33 of the substrate 31 is recognized (by the insertion-hole recognition part 71 of FIG. 1, which corresponds to the recognition part) from above. However, the substrate recognition is performed not at a position close to the substrate 31. Thus, the substrate 31 can be continuously heated. Further, the joining step 86 of joining the chip 32 can be implemented from above the substrate 31. This bonding method can be used for ordinary face-up bonding (a case in which the electrode surface of the chip is to be adhered).

[0066] Further, according to this bonding method, the adhesives S configured to join the chip 32 to the chip joining surface 31b of the substrate 31 are provided on the chip joining surface 31b in an upwardly directed state. Thus, even when the adhesive S has relatively high fluidity, there is no risk of dripping downward. Thus, application work for the adhesives S is easy. In addition, various adhesives can be used as the adhesives S, contributing to a reduction in cost.

[0067] In the present invention, the pattern formation surface 31a is observed not based on an indirect image. Thus, the field of view for observation is not restricted, the pattern formation surface 31a can be stably observed with high accuracy, and the chip 32 can be stably joined to the substrate 31 with high accuracy. Further, the chip 32 can be joined to the substrate 31 at low cost without complicating a device

configuration. Further, in the joining step 86 of joining the chip 32, the chip can be brought from above the substrate 31. This bonding method can be used for ordinary face-up bonding (a case in which the electrode surface of the chip is to be adhered). In addition, the substrate 31 can be continuously heated, resulting in excellent productivity.

[0068] The fiducial marks 40 for alignment are formed on the surface of the substrate 31, on which the pattern formation surface 31a is formed. Thus, the alignment step can be stably carried out. Specifically, the positional relationship among the positions of the fiducial marks 40 for alignment and the positions of the electrodes on the pattern formation surface 31a of the substrate 31 has high accuracy. Thus, the alignment step 85 can be stably carried out.

[0069] The method may comprise the chip recognition steps 87 and 88 for performing the position recognition for the chip 32 before bonding. When the method comprises the chip recognition steps 87 and 88 as described above, improvement in alignment accuracy can be achieved.

[0070] In the joining step 86, the substrate 31 is received by the backup plate 43 from below. Thus, when the chip 32 is joined to the chip joining surface 31b of the substrate 31, the chip 32 can be sandwiched between the collet 62 and the backup plate 43. Thus, stable joint can be obtained without, for example, curving the substrate 31.

[0071] An existing general-purpose bonding device can be used as each of components of the bonding device used for the bonding method according to the present invention. Thus, a reduction in cost can be achieved.

[0072] The present invention is not limited to the embodiment described above, and various modifications are possible. For example, when the adhesives S are to be heated, the bonding-side collet 62 may be heated. In this case, a heater may be provided only on the collet 62 side, only on the backup plate 43 side, or on each of the collet 62 side and the backup plate 43 side. Further, the backup plate 43 is not required to be provided. In such a case, a heater is additionally provided below the bonding position. As each of heaters in this case, various types of electric heating can be used.

[0073] Further, in the embodiment described above, the first chip recognition part 72 and the second chip recognition part 73 are used to check the position of the chip before bonding. However, any one of the chip recognition parts may be used. In the embodiment, as the observation part 53, the camera main body 66 is arranged so as to extend in a horizontal direction. However, the camera main body 66 may be arranged so as to be directed in a vertical direction.

[0074] In the embodiment, as illustrated in FIG. 6, after Step S1 corresponding to the step of performing substrate recognition is carried out, Step S2 corresponding to the step of

picking up the chip 32 is carried out. However, after Step S1, the substrate 31 may be conveyed, and the alignment of the substrate and the chip in Step S8 may be carried out. Specifically, the chip and the chip joining portion are aligned with each other based on the positional relationship among the fiducial marks for alignment and the wire insertion hole and the recognition of the position of the wire insertion hole, which is performed from above the bonding position. In this case, the alignment using the position recognition for the chip, which is performed in the first chip recognition step 87 and the second chip recognition step 88, cannot be performed, or after the chip and the chip joining portion are aligned with each other based on the positional relationship among the fiducial marks for alignment and the wire insertion hole and the recognition of the position of the wire insertion hole, which is performed from above the bonding position, alignment based on the position of the chip itself is performed.

Industrial Applicability

[0075] The bonding method and the method using a bonding device are used to manufacture a board-on-chip (BOC) type electronic component (semiconductor device).

Reference Signs List

[0076] 31 substrate

31a pattern formation surface
31b chip joining surface
32 chip
32a electrode formation surface
33 wire insertion hole
34 chip joining portion
40 fiducial mark
43 backup plate
57 pickup-side collet
58 reversing mechanism
62 bonding-side collet
81 substrate recognition step
82 pickup step
83 reversing step
84 receiving step
85 alignment step
86 joining step
S adhesive

Claims

[Claim 1] A bonding method which involves: conveying a substrate, which has a wire insertion hole passing therethrough in a thickness direction of the substrate and has fiducial marks for alignment formed on a pattern formation surface, conveyed from an upstream side to a downstream side along a substrate conveyance path; and joining, at a bonding position on a downstream side in a substrate conveyance path, an electrode formation surface of a chip onto a chip joining portion of a chip joining surface, which is located on a side opposite to a substrate-side electrode portion of a pattern formation surface of the substrate,

the bonding method comprising:

a substrate recognition step of recognizing a positional relationship among the fiducial marks for alignment and the wire insertion hole from below on the upstream side in the substrate conveyance path under a state in which the substrate is disposed with the pattern formation surface directed downward;

a pickup step of picking up the chip with use of a pickup-side collet;

a reversing step of reversing the chip picked up by the pickup-side collet so that the electrode formation surface of the chip is directed downward;

a receiving step of receiving the chip, which has been reversed in the reversing step, while the electrode formation

surface is kept directed downward, with use of a bonding-side collet;

an alignment step of aligning the chip and the chip joining portion based on the positional relationship among the fiducial marks for alignment and the wire insertion hole, which has been recognized in the recognition step, and recognition of a position of the wire through hole, which is performed from above the bonding position; and

a joining step of joining, at the bonding position on the downstream side in the substrate conveyance path, the chip, which has been received in the receiving step, to the chip joining portion of the substrate, which has been aligned in the alignment step.

[Claim 2] The bonding method according to claim 1, wherein the substrate recognition step is carried out in an area where the substrate is unheated.

[Claim 3] The bonding method according to claim 1 or 2, wherein, in the substrate recognition step, positional information for one substrate is acquired.

[Claim 4] The bonding method according to any one of claims 1 to 3, further comprising a chip recognition step of performing position recognition for the chip before bonding.

[Claim 5] The bonding method according to any one of claims 1 to 4, wherein, in the joining step, the substrate is received by a backup plate from below.

[Claim 6] The bonding method according to claim 5, wherein the backup plate is heated by a heater so as to heat an adhesive on the substrate.

[Claim 7] A method using a bonding device configured to pick up a chip at a pickup position with use of a pickup-side collet, reverse the chip picked up at the pickup position, and bond the reversed chip at a bonding position with use of a bonding-side collet,

the method enabling the bonding method of any one of claims 1 to 6.