

Description

BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to an output circuit for converting input charges into electrical voltage. More particularly, it relates to an output circuit, such as an initial stage output buffer of a charge transfer device, such as CCD imaging device or CCD delay device.

(2) Description of the Prior Art

In CCD imaging or CCD delay devices, an output circuit for outputting signal charges is formed on a chip for converting minute input electrical charges into electrical voltage.

Fig. 1 shows an example of a customary output circuit in which a transfer electrode 102 for transferring electrical charges and an output gate 103 are formed on a substrate 101. A floating diffusion region 104 for storage of signal charges is disposed between the output gate 103 and a precharging gate 105 and connected to a gate of an nMOS transistor 106 constituting an initial stage source follower of the output circuit. With this initial stage source follower, a ground voltage GND is applied via a constant current source 107 to the source of the nMOS transistor 106, the drain of which is supplied with a source voltage V_{DD} . The output of this initial stage source follower is provided from the source of nMOS transistor 106 and input to the gate of an nMOS transistor 108 constituting the next stage buffer. A constant current source 109 is similarly connected to the source of the nMOS transistor 108, from which an output signal V_{out} is provided.

There is also known a prior art device in which the floating diffusion region 104 is replaced by a floating gate from which electrical charges are supplied to a source follower so as to be converted into an electrical voltage.

Another output circuit (JP 60-22 31 61) is known for a charge coupled device having linearity by a method wherein the second semiconductor region is connected common to the source terminal of a MOS transistor having a drain terminal connected to a power source to reduce the input capacitance of a source follower output circuit and to eliminate a backgate effect.

In these output circuits, conversion from minute electrical charges into electrical voltage is carried out and, the larger the charge to voltage conversion gain, the higher is the S/N ratio of the circuit.

Meanwhile, from the well-known relation $Q = V \times C$, where V represents electrical voltage, Q

electrical charges and C electrical capacitance, an output circuit with a lesser electrical capacitance is preferred because lesser electrical charges suffice to produce desired electrical voltage.

Above all, as shown in Fig. 2, the following relation

$$C_{tot} = C_{FD} + C_s + C_{GD}$$

where C_{tot} represents total capacitance, C_{FD} the capacitance between the floating diffusion region and the substrate, C_s the wiring capacity and C_{GD} the gate-to-drain capacitance of the nMOS transistor, holds from the floating diffusion region 110 to the first stage source follower nMOS transistor 111. Above all, it is required from circuit characteristics to reduce the capacitance C_{GD} which depends upon the gate-to-drain overlap of the nMOS transistor which is supplied with a signal V_{sig} .

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an output circuit for converting input electrical charges into an electrical voltage, wherein the gate-to-drain capacitance of a first stage transistor of the output circuit is reduced to improve its electrical charge-to-voltage conversion gain.

The output circuit of the present invention includes a first MIS transistor having its gate supplied with input electrical charges and constituting a source follower for outputting a voltage signal converted from input electrical charges, which have been derived from a floating diffusion region or a floating gate. A constant current source may be connected to the source of the first MIS transistor and a load may be connected between the constant current source and an electrical source connected to the constant current source. To the drain side of the first MIS transistor is connected a depletion type or normally-on second MIS transistor, by means of which the electrical power is supplied from the electrical source to the source follower. This second MOS transistor has its gate connected to the output section of the source follower, that is to the source of the first MIS transistor. Thus the output signal of the second MIS transistor is changed in phase with the input signal, so that the drain level of the first MIS transistor follows level shifts of the gate of the first MIS transistor to reduce parasitic capacitance to improve its charge-to-voltage conversion gain.

It is also possible with the output circuit of the present invention to set the potential of the source of the first or second MIS transistor so as to be equal to the substrate potential inclusive of the well potential. Another object of the invention is a charge coupled device with such an output circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an example of an output circuit of a customary CCD.

Fig. 2 is a circuit diagram showing essential portions of an example of the output circuit shown in Fig. 1.

Fig. 3 is a circuit showing an embodiment of the output circuit according to the present invention.

Fig. 4 is a cross-sectional view showing the output circuit of Fig. 3 formed on a substrate.

Fig. 5 shows a potential energy distribution along the cross-section of Fig. 4 with the source voltage V_{DD} equal to 15V.

Fig. 6 is a circuit diagram showing a modified embodiment of the output circuit according to the present invention.

Fig. 7 is a cross-sectional view of the output circuit of Fig. 6 formed on a substrate.

Fig. 8 is a circuit diagram showing another modified embodiment of the output circuit of the present invention.

Fig. 9 is a circuit diagram showing a further modified embodiment of the output circuit of the present invention.

Fig. 10 is a circuit diagram showing a still further modified embodiment of the output circuit of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

By referring to the drawings, certain preferred embodiments of the present invention will be explained in detail.

First Embodiment

The present embodiment is directed to an output circuit formed on a CCD chip.

Fig. 3 shows a circuit organization of the present embodiment, wherein an nMOS transistor 1, which is a first MIS transistor constituting a source follower, has its gate connected to a floating diffusion region 10, which is provided at an end of a charge transfer section, not shown. The nMOS transistor 1 has its gate supplied with input electrical charges from the floating diffusion region 10. The source of the nMOS transistor 1 represents an output section 6 of the first stage source follower and is connected to the gate of an nMOS transistor 4 constituting the next stage source follower. An nMOS transistor 3 functioning as a constant current source is connected between the source of nMOS transistor 1 and the ground voltage GND. A constant voltage V_{GG} is supplied to the gate of the nMOS transistor 3.

The nMOS transistor 1 has its drain connected to the source of an nMOS transistor 2 which is a

depletion type second MIS transistor. A source voltage V_{DD} is supplied to the drain of this depletion type nMOS transistor 2, the gate of which is connected to the source of the nMOS transistor 1, that is the output section 6 of the source follower.

The next stage source follower is comprised of nMOS transistors 4, 5, and the nMOS transistor 4 having its gate connected to the output section 6 of the first stage source follower has its drain supplied with the source voltage V_{DD} , whereas the nMOS transistor 5 has its source supplied with the ground voltage GND while having its gate supplied with the constant voltage V_{GG} . An output signal is provided the source of nMOS transistor 4.

With the above described output circuit of the present illustrative embodiment, a voltage V_p at the source of the nMOS transistor 2 may be changed responsive to changes in the input voltage V_{sig} which is the gate voltage of the nMOS transistor 1. That is, the nMOS transistor 1 is caused to act as the source follower, at the same time that the nMOS transistor 2 substantially plays the role of the source follower. For example, with the gains G_1 and G_2 of the source followers about equal to 0.9, the following relation

$$V_{out} = G_1 \cdot V_{sig}$$

holds in the first stage source follower, so that

$$V_p \doteq G_2 \cdot G_1 \cdot V_{sig}$$

and hence it may be seen that the potential V_p at the drain of the nMOS transistor 1 is changed in phase with the input voltage V_{sig} . Thus the gate-to-drain capacitance C_{GD} of the nMOS transistor 1 is equivalently reduced and assumes a small value equal to 15 to 30 % of the previous values. In this manner, the charge-to-voltage conversion gain may be improved, whereas the short channel effect is alleviated and the source follower gain is also improved.

Fig. 4 shows in cross-sectional view a first stage source follower of the output circuit of the present embodiment formed on a chip. A p-type well region 22 is formed on an n-type silicon substrate, and a floating diffusion region 23 consisting of an n-type impurity diffusion region is formed on the p-type well region 22. In the p-type well region 22, there are formed n-type high concentration impurity diffusion regions 24a to 24d, in self-alignment with the gate electrode, with the n-type high concentration impurity diffusion regions 24a, 24b proving to be the drain and the source of the depletion type nMOS transistor 2, the n-type high concentration impurity diffusion regions 24b, 24c proving to be the drain and the source of the nMOS transistor 1 and the n-type high concentra-

tion impurity diffusion regions 24c, 24d proving to be the drain and the source of the nMOS transistor 3 functioning as the constant current source. The n-type high concentration impurity diffusion region 24c proves to be the output section 6, the source voltage V_{DD} is supplied to the n-type high concentration impurity diffusion region 24a and the ground voltage GND is supplied to the n-type high concentration impurity diffusion region 24d. With the present embodiment, the n-type high concentration impurity diffusion region 24c, functioning as the source of the nMOS transistor 1 constituting the source follower, is connected to the gate of the nMOS transistor 2, so that the gate-to-drain capacitance C_{GD} of the nMOS transistor 1 is reduced.

Fig. 5 shows an electrical potential energy distribution along the cross-section of Fig. 4, wherein the source voltage V_{DD} is about 15V, the ground voltage GND is 0V, the voltage V_{GG} is of the order of 2.5 to 3.0V and the center of the DC level of the input signal V_{sig} is about 8.0V.

In this figure, an output from the source follower is issued with changes in the potential ϕ_{OUT} in the high concentration impurity diffusion region 24c. Since the potential ϕ_2 of the high concentration impurity diffusion region 24b is changed with the change is the potential ϕ_{OUT} , and the changes in these potentials occur in phase with each other, a voltage difference ΔV_{gd1} shows only a minor change as compared with the case in which there lacks the nMOS transistor 2. Thus the gate-to-drain capacitance C_{GD} of the nMOS transistor 1 is reduced to improve the charge-to-voltage conversion gain.

As regards the manufacture method, the depletion type nMOS transistor 2 may be formed by ion implantation, such as, for example, implantation of phosphorus ions, for adjusting the threshold voltage V_{th} . Since it is only sufficient if the mask of ion implantation employed for forming the buried channel in the customary CCD process is modified on the output circuit, there is no necessity of increasing the number of process steps.

Second Embodiment

The present embodiment is directed to a CCD output circuit in which the p-type well region is biased to the source potential.

Fig. 6 shows the circuit organization of the output circuit wherein the floating diffusion region 30 is connected to the gate of the nMOS transistor 31 constituting a source follower. An nMOS transistor 33 functioning as the constant current source is connected between the source of the nMOS transistor 31 and the ground voltage GND. The gate of the nMOS transistor 33 is supplied with the constant potential V_{GG} . The depletion type nMOS tran-

sistor 32 has its gate connected to the source of the nMOS transistor 31 functioning as the output of the source follower. The source voltage V_{DD} is supplied to the drain of the nMOS transistor 32. This depletion type nMOS transistor 32 has its source connected to the drain of the nMOS transistor 31. Hence, by the operation of the nMOS transistor 32, the drain of the nMOS transistor 31 is controlled so as to be in phase with respect to the output voltage of the source follower, so that the gate-to-drain capacitance C_{GD} of the nMOS transistor 31 is prevented from increasing.

With the output circuit of the present embodiment, the potentials of the wells of the nMOS transistors 31, 32 are set so as to be equal to the potential at the respective sources of these nMOS transistors. For this reason, the well potential and the source potential are in phase with each other so that the channel-to-well capacitance is equivalently reduced to prevent the gain from being lowered.

Fig. 7 shows in cross-section the construction of the device according to the present embodiment. The nMOS transistor 31 to 33 are formed within p-type well regions 35 to 37, respectively, which are formed on the surface of an n-type silicon substrate 34 to which the substrate potential V_{sub} is supplied.

More specifically, the nMOS transistor 31, from the source of which an output voltage V_{out} is provided, has an n-type high concentration impurity diffusion region 38 within the p-type well region 35 as the drain and an n-type high concentration impurity diffusion region 39 as the source. The gate 40 of the nMOS transistor 31 is formed at an upper portion of a region between the n-type high concentration impurity diffusion regions 38, 39 and is supplied with input voltage V_{sig} . In the p-type well region 35, there is formed a plug-in region 41, which is a p-type high concentration impurity diffusion region 41 for affording a well potential and the same potential as that of the n-type high concentration diffusion region 39 is applied to this plug-in region 41.

The depletion type nMOS transistor 32, which is formed on the side source voltage V_{DD} of the nMOS transistor 31, has an n-type high concentration impurity diffusion region 42 in the p-type well region 36 as the drain and an n-type high concentration diffusion region 43 in the p-type well region 36 as the source. The gate 44 of the transistor 32 is formed in an upper portion of a region between the n-type high concentration impurity diffusion regions 42, 43, and is connected to the n-type high concentration impurity diffusion region 39, which is the source of the nMOS transistor 31. The n-type high concentration impurity diffusion region 43 functioning as the source is connected to

the n-type high concentration impurity diffusion region 38, functioning as the drain of the nMOS transistor 31, and is connected to a plug-in region 45 consisting of a p-type high concentration impurity diffusion region for affording the well region 36.

The nMOS transistor 33 as the constant current source has its drain formed by an n-type high concentration impurity diffusion region 46 formed in turn in a p-type well region 37, and its source connected to the ground potential GND formed by an n-type high concentration impurity diffusion region 47 formed in turn in the well region 37. The drain of the nMOS transistor 33 is connected to the source of the nMOS transistor 31. The gate 48 of the nMOS transistor 33, supplied with the constant voltage V_{GG} , is formed on top of an between these n-type high concentration impurity diffusion regions 46, 47. A plug-in region 49 consisting of an n-type high concentration impurity diffusion region is formed in the well region and supplied with the ground voltage GND.

With the above described output circuit, the potential of the n-type high concentration impurity diffusion region 38, functioning as the drain of the nMOS transistor 31, is changed in phase with input voltage V_{sig} , owing to the function of the nMOS transistor 32, to the gate 44 of which the output voltage V_{out} is input. As a result, the gate-to-drain capacitance C_{GD} of the nMOS transistor 31 is reduced. With the output circuit of the present illustrative embodiment, the plug-in regions 41, 45, 49 of the well regions 35, 36, 37 are connected to the source of the nMOS transistors 31, 32, 33, respectively. Thus the substrate potential or well potential may be changed in phase with the source potential to reduce the channel-to-well parasitic capacitance to prevent the gain from being lowered.

Third Embodiment

The present third embodiment is a modification from the first embodiment and has a circuit organization in which a resistor is provided at the ground side terminal of the constant current source.

Fig. 8 shows the circuit organization, wherein an nMOS transistor 51, which is a first MIS transistor, has its gate connected to a floating diffusion region 55, with the source of the transistor 51 functioning as an output section for outputting to the next stage source follower. The source of this nMOS transistor 51 is also connected to the gate of an nMOS transistor 52, a depletion type second MIS transistor, and to the drain of an nMOS transistor 53, functioning as the constant current source. The depletion type nMOS transistor 52 has its drain supplied with the source voltage V_{DD} , and has its source connected to the drain of the nMOS

transistor 51. Thus the gate-to-drain capacitance C_{GD} of the nMOS transistor 51 may be lowered. The nMOS transistor 53 functioning as the constant current source has its gate supplied with the constant voltage V_{GG} and has its source supplied with the ground potential GND via resistor 54. The next stage source follower is constituted by an nMOS transistor 56 and an nMOS transistor 57 functioning as a constant current source.

With the output circuit of the present embodiment, since the resistor 54 is connected between the nMOS transistor 53 and the ground voltage GND, changes in the constant current caused by noises occasionally contained in the constant voltage V_{GG} may be absorbed to maintain the constant current value. The gate-to-drain capacitance C_{GD} of the nMOS transistor 51 may naturally be lowered, similarly to the above embodiment.

In the present embodiment, the source potential may be rendered equal to the substrate or well potential, similarly to the second embodiment.

Fourth Embodiment

With the output circuit of the fourth embodiment, input charges of the output circuit of the first embodiment are taken out via the floating gate.

Fig. 9 shows a circuit organization wherein an nMOS transistor 61, which is a first MIS transistor, has its gate connected to a floating gate 64, from which input charges are transferred to the gate of nMOS transistor 61. This nMOS transistor 61 constitutes a source follower, the output of which is provided from its source. This source is supplied with the ground voltage GND via nMOS transistor 63 as the constant current source, and is connected to the gate of a depletion type nMOS transistor 62. This depletion type nMOS transistor 62 has its drain supplied with the source voltage V_{DD} and has its source connected to the drain of the nMOS transistor 61 constituting the source follower. The next stage source follower is constituted by an nMOS transistor 65 and an nMOS transistor 66.

With the above described arrangement of taking out input charges at the floating gate 64, the drain potential of the nMOS transistor 61 is changed by the depletion type nMOS transistor 62 in phase with the input charges, as a result of which the gate-to-drain capacitance C_{GD} of the nMOS transistor 61 may be reduced. With the above arrangement, the substrate or well potential may be made equal to the source potential of each of the nMOS transistors.

Fifth Embodiment

With the present fifth embodiment, input charges are provided from a floating gate and a

resistor is connected in series with the constant current source.

Fig. 10 shows the circuit arrangement, wherein an nMOS transistor 71, which is a first MIS transistor, has its gate connected to a floating gate 74, from which input charges are transferred to the gate of the nMOS transistor 71. This nMOS transistor 71 constitutes a source follower, the output of which is taken out at its source. An nMOS transistor 73 as a constant current source and a resistor 75 are connected in series between the source and a transistor 71 and the ground voltage GND to suppress any adverse affects due to noises occasionally contained in the constant voltage V_{GG} . The nMOS transistor 71 has its source connected to the gate of a depletion type nMOS transistor 72. This depletion type nMOS transistor 72 has its drain supplied with the source voltage V_{DD} and has its source connected to the drain of the nMOS transistor 71 constituting a source follower. Thus the gate-to-drain capacitance C_{GD} of the nMOS transistor 71 may be lowered. The next stage source follower is constituted by an nMOS transistor 76 and an nMOS transistor 77 as the constant current source.

With the above described arrangement of taking out input charges and providing the resistor in series with the constant current source, the gate-to-drain capacitance C_{GD} may be reduced.

Claims

1. An output circuit of a source follower for converting input charges into an electrical voltage signal with an output section for outputting the converted voltage signal, this circuit comprising
 - a first MIS transistor (1) constituting said source follower and having its gate supplied with input electrical charges,
 - said output section (6) of said source follower which is the source of said first MIS transistor (1) and from which said converted voltage signal (V_{OUT}) is output and being characterised by
 - a depletion type second MIS transistor (2) connected between the drain side of said first MIS transistor (1) and an electrical source (V_{DD}) and having its gate connected to said output section (6).
2. A charge coupled device with said output circuit according to claim 1, comprising
 - a semiconductor substrate (21),
 - a charge transfer section formed on said semiconductor substrate,
 - charge extracting means (10, 23, 55, 64, 74) formed on said semiconductor substrate (21) and at an end of said charge

transfer section, and

- said output circuit formed on said semiconductor substrate (21) and adapted for amplifying electrical charges from said charge extracting means.
3. The charge coupled device according to claim 2 wherein said charge extracting means is a floating diffusion (23, 10, 55).
 4. The charge coupled device according to claim 2, wherein said charge extracting means is a floating gate (64, 74).
 5. The charge coupled device according to claim 2, wherein a source voltage (V_{DD}) is applied to the drain of a second MIS transistor (2), a ground voltage is supplied to the source of said first MIS transistor (1) via a constant current source (3) and wherein said first (1) and second (2) MIS transistors each have a structure of an n-channel MOS transistor.
 6. The output circuit according to claim 1, comprising
 - a constant current source (3) connected to the source of said first MIS transistor (1), and
 - a load connected between said constant current source (3) and a reference voltage line.
 7. The output circuit according to claim 1, whereby the substrate potential of said first MIS transistor (1) and/or said second MIS transistor (2) is equal to the source potential of each of said MIS transistors.
 8. The output circuit according to claim 1 including a first stage buffer, comprising
 - said first MIS transistor (1) having a channel of a first conductivity type, said first MIS transistor (1) being formed in a first well region (22) of a second conductivity type and having its gate supplied with input electrical charges, said first well region (22) being set to an electrical potential equal to that of its source,
 - said output section (6) of said source follower which is the source of said first MIS transistor (1) and from which an output converted into an electrical voltage is provided, and
 - said depletion type second MIS transistor (2) having a channel of a first conductivity type, said MIS transistor being formed in a second well region (22) of a second



resistor is connected in series with the constant current source.

Fig. 10 shows the circuit arrangement, wherein an nMOS transistor 71, which is a first MIS transistor, has its gate connected to a floating gate 74, from which input charges are transferred to the gate of the nMOS transistor 71. This nMOS transistor 71 constitutes a source follower, the output of which is taken out at its source. An nMOS transistor 73 as a constant current source and a resistor 75 are connected in series between the source and a transistor 71 and the ground voltage GND to suppress any adverse affects due to noises occasionally contained in the constant voltage V_{GG} . The nMOS transistor 71 has its source connected to the gate of a depletion type nMOS transistor 72. This depletion type nMOS transistor 72 has its drain supplied with the source voltage V_{DD} and has its source connected to the drain of the nMOS transistor 71 constituting a source follower. Thus the gate-to-drain capacitance C_{GD} of the nMOS transistor 71 may be lowered. The next stage source follower is constituted by an nMOS transistor 76 and an nMOS transistor 77 as the constant current source.

With the above described arrangement of taking out input charges and providing the resistor in series with the constant current source, the gate-to-drain capacitance C_{GD} may be reduced.

Claims

1. An output circuit of a source follower for converting input charges into an electrical voltage signal with an output section for outputting the converted voltage signal, this circuit comprising
 - a first MIS transistor (1) constituting said source follower and having its gate supplied with input electrical charges,
 - said output section (6) of said source follower which is the source of said first MIS transistor (1) and from which said converted voltage signal (V_{OUT}) is output and being characterised by
 - a depletion type second MIS transistor (2) connected between the drain side of said first MIS transistor (1) and an electrical source (V_{DD}) and having its gate connected to said output section (6).
2. A charge coupled device with said output circuit according to claim 1, comprising
 - a semiconductor substrate (21),
 - a charge transfer section formed on said semiconductor substrate,
 - charge extracting means (10, 23, 55, 64, 74) formed on said semi-conductor substrate (21) and at an end of said charge

transfer section, and

- said output circuit formed on said semiconductor substrate (21) and adapted for amplifying electrical charges from said charge extracting means.
3. The charge coupled device according to claim 2 wherein said charge extracting means is a floating diffusion (23, 10, 55).
 4. The charge coupled device according to claim 2, wherein said charge extracting means is a floating gate (64, 74).
 5. The charge coupled device according to claim 2, wherein a source voltage (V_{DD}) is applied to the drain of a second MIS transistor (2), a ground voltage is supplied to the source of said first MIS transistor (1) via a constant current source (3) and wherein said first (1) and second (2) MIS transistors each have a structure of an n-channel MOS transistor.
 6. The output circuit according to claim 1, comprising
 - a constant current source (3) connected to the source of said first MIS transistor (1), and
 - a load connected between said constant current source (3) and a reference voltage line.
 7. The output circuit according to claim 1, whereby the substrate potential of said first MIS transistor (1) and/or said second MIS transistor (2) is equal to the source potential of each of said MIS transistors.
 8. The output circuit according to claim 1 including a first stage buffer, comprising
 - said first MIS transistor (1) having a channel of a first conductivity type, said first MIS transistor (1) being formed in a first well region (22) of a second conductivity type and having its gate supplied with input electrical charges, said first well region (22) being set to an electrical potential equal to that of its source,
 - said output section (6) of said source follower which is the source of said first MIS transistor (1) and from which an output converted into an electrical voltage is provided, and
 - said depletion type second MIS transistor (2) having a channel of a first conductivity type, said MIS transistor being formed in a second well region (22) of a second



conductivity type between the drain side (24b) of said first MIS transistor (1) and an electrical source (24a) and having its gate connected to said output section (6), said second well region being set to an electrical potential equal to that of its source.

9. The charge coupled device according to claim 2 comprising the output circuit according to claim 8, wherein

- said semiconductor substrate (21) is of a first conductivity type,
- said charge transfer section is formed in a well region of a second conductivity type in said semiconductor substrate (21),
- said charge extracting means (10, 23, 55, 64, 74) are formed on said semiconductor substrate and at the end of said charge transfer section.

10. The charge coupled device according to claim 9, wherein a constant current source (3; 33; 53; 63; 73) constituting the source follower is constituted by a nMOS transistor having a channel of a first conductivity type, said nMOS transistor being formed in a well region of the second conductivity type distinct from said well regions of the second conductivity type having said first and second MIS transistors.

Patentansprüche

1. Ausgangsschaltung eines Source-Folgers zum Wandeln von Eingangsladungen in ein elektrisches Spannungssignal, mit einem Ausgabebereich zum Ausgeben des gewandelten Spannungssignals, bei welcher Schaltung

- ein erster MIS-Transistor (1) den Source-Folger bildet, dessen Gate-Anschluß mit den elektrischen Eingangsladungen beaufschlagt ist,
- die Source des ersten MIS-Transistors (1) den Ausgabebereich (6) des Source-Folgers bildet, über die das gewandelte Spannungssignal (V_{OUT}) ausgegeben wird,

gekennzeichnet durch

- einen zwischen die Drain des ersten MIS-Transistors (1) und eine elektrische Quelle (V_{DD}) geschalteten zweiten MIS-Transistor (2) vom Verarmungstyp, dessen Gate mit dem Ausgabebereich (6) verbunden ist.

2. Ladungsgekoppelter Baustein mit einer Ausgangsschaltung nach Anspruch 1, gekenn-

zeichnet durch

- ein Halbleitersubstrat (21),
- einen auf dem Halbleitersubstrat ausgebildeten Ladungsübertragungsbereich,
- eine auf dem Halbleitersubstrat (21) an einem Ende des Ladungsübertragungsbereichs ausgebildete Einrichtung (10, 23, 55, 64, 74) zum Auslesen von Ladungen,
- wobei die Ausgangsschaltung auf dem Halbleitersubstrat (21) ausgebildet ist, zum Verstärken der von der Ladungsausleseeinrichtung bereitgestellten elektrischen Ladungen.

3. Ladungsgekoppelter Baustein nach Anspruch 2, dadurch gekennzeichnet, daß die Einrichtung zum Auslesen von Ladungen ein potentialfrei gehaltener Diffusionsbereich (23, 10, 55) ist.

4. Ladungsgekoppelter Baustein nach Anspruch 2, dadurch gekennzeichnet, daß die Einrichtung zum Auslesen von Ladungen ein schwimmendes Gate (64, 74) ist.

5. Ladungsgekoppelter Baustein nach Anspruch 2, dadurch gekennzeichnet, daß eine Source-Spannung (V_{DD}) den Drain-Anschluß eines zweiten MIS-Transistors (2) beaufschlagt, eine Grundspannung über eine Konstantstromquelle (3) den Source-Anschluß des ersten MIS-Transistors (1) beaufschlagt, und daß der erste (1) und der zweite (2) MIS-Transistor jeweils den Aufbau eines N-Kanal-MOS-Transistors aufweisen.

6. Ausgangsschaltung nach Anspruch 1, gekennzeichnet durch

- eine mit dem Source-Anschluß des ersten MIS-Transistors (1) verbundene Konstantstromquelle (3), und durch
- eine Last zwischen der Konstantstromquelle (3) und einer Bezugsspannung.

7. Ausgangsschaltung nach Anspruch 1, dadurch gekennzeichnet, daß das Substratpotential des ersten MIS-Transistors (1) und/oder des zweiten MIS-Transistors (2) gleich dem Source-Potential der jeweiligen MIS-Transistoren ist.

8. Ausgangsschaltung nach Anspruch 1 mit einem ersten Stufenpuffer, dadurch gekennzeichnet, daß

- der erste MIS-Transistor (1) einen Kanal mit einer ersten Leitfähigkeit aufweist, in einem ersten leitfähigen Bereich (22) ei-



ner zweiten Leitfähigkeit ausgebildet ist und sein Gate-Anschluß mit elektrischen Eingangsladungen beaufschlagt wird, wobei der erste leitfähige Bereich (22) auf ein elektrisches Potential gleich dem seines Source-Anschluß gesetzt ist,

- der den Source-Anschluß des ersten MIS-Transistors (1) darstellende Ausgabebereich (6) des Source-Folgers vorhanden ist, von dem ein in eine elektrische Spannung gewandeltes Ausgangssignal ausgeht, und daß
- der zweite MIS-Transistor (2) vom Verarmungstyp einen Kanal einer ersten Leitfähigkeit aufweist, wobei der MIS-Transistor in einem zweiten leitfähigen Bereich (22) einer zweiten Leitfähigkeit zwischen dem Drain-Anschluß (24b) des ersten MIS-Transistors (1) und einer elektrischen Quelle (24a) ausgebildet und sein Gate-Anschluß mit dem Ausgabebereich (6) verbunden ist, wobei der zweite leitfähige Bereich auf das gleiche elektrische Potential gesetzt ist, wie sein Source-Anschluß.

9. Ladungsgekoppelter Baustein nach Anspruch 2 mit der Ausgangsschaltung nach Anspruch 8, dadurch gekennzeichnet, daß

- das Halbleitersubstrat (21) eine erste Leitfähigkeit aufweist,
- der Ladungsübertragungsbereich in einem Leitfähigkeitsbereich einer zweiten Leitfähigkeit in dem Halbleitersubstrat (21) ausgebildet ist,
- die Einrichtung (10, 23, 55, 64, 74) zum Abgreifen von Ladung auf dem Halbleitersubstrat am Ende des Ladungsübertragungsbereichs ausgebildet ist.

10. Ladungsgekoppelter Baustein nach Anspruch 9, dadurch gekennzeichnet, daß eine den Source-Folger darstellende Konstantstromquelle (3; 33; 53; 63; 73) durch einen nMOS-Transistor mit einem Kanal einer ersten Leitfähigkeit gebildet wird, wobei der nMOS-Transistor in einem Leitfähigkeitsbereich einer zweiten Leitfähigkeit getrennt von den den ersten und den zweiten MIS-Transistor aufweisenden Leitfähigkeitsbereichen der zweiten Leitfähigkeit ausgebildet ist.

Revendications

- 1. Circuit de sortie d'un suiveur de source pour convertir des charges d'entrée en un signal de tension électrique, muni d'une section de sortie pour émettre en sortie le signal de tension**

converti, ce circuit comprenant :

un premier transistor métal-isolant-semi-conducteur (MIS) (1) constituant ledit suiveur de source et se voyant appliquer sur sa grille des charges électriques d'entrée ;

ladite section de sortie (6) dudit suiveur de source qui est la source dudit premier transistor MIS (1) et depuis laquelle ledit signal de tension converti (V_{OUT}) est émis en sortie étant caractérisée par :

un second transistor MIS du type à appauvrissement (2) connecté entre le côté de drain dudit premier transistor MIS (1) et une source électrique (V_{DD}) et ayant sa grille connectée à ladite section de sortie (6).

2. Dispositif à couplage de charge muni dudit circuit de sortie selon la revendication 1, comprenant :

un substrat semiconducteur (21) ;

une section de transfert de charges formée sur ledit substrat semiconducteur ;

un moyen d'extraction de charges (10, 23, 55, 64, 74) formé sur ledit substrat semiconducteur (21) et au niveau d'une extrémité de ladite section de transfert de charges ; et

ledit circuit de sortie formé sur ledit substrat semiconducteur (21) et conçu pour amplifier des charges électriques provenant dudit moyen d'extraction de charges.

3. Dispositif à couplage de charge selon la revendication 2, dans lequel ledit moyen d'extraction de charges est une diffusion flottante (23, 10, 55).

4. Dispositif à couplage de charge selon la revendication 2, dans lequel ledit moyen d'extraction de charges est une grille flottante (64, 74).

5. Dispositif à couplage de charge selon la revendication 2, dans lequel une tension de source (V_{DD}) est appliquée au drain d'un second transistor MIS (2), une tension de masse est appliquée à la source dudit premier transistor MIS (1) via une source de courant constant (3) et dans lequel lesdits premier (1) et second (2) transistors MIS comportent chacun une structure constituée par un transistor métal-oxyde-semiconducteur (MOS) à canal N.

6. Circuit de sortie selon la revendication 1, comprenant :

une source de courant constant (3) connectée à la source dudit premier transistor MIS (1) ; et

une charge connectée entre ladite source de courant constant (3) et une ligne de tension



de référence.

7. Circuit de sortie selon la revendication 1 et ainsi, le potentiel de substrat dudit premier transistor MIS (1) et/ou dudit second transistor MIS (2) est égal au potentiel de source de chacun desdits transistors MIS. 5
8. Circuit de sortie selon la revendication 1, incluant un premier tampon d'étage, comprenant : 10
 - ledit premier transistor MIS (1) comportant un canal d'un premier type de conductivité, ledit premier transistor MIS (1) étant formé dans une première région de puits (22) d'un second type de conductivité et se voyant appliquer sur sa grille des charges électriques d'entrée, ladite première région de puits (22) étant établie à un potentiel électrique égal à celui de sa source ; 15 20
 - ladite section de sortie (6) du suiveur de source qui est la source dudit premier transistor MIS (1) et depuis laquelle une sortie convertie en tension électrique est produite ; et
 - ledit second transistor MIS du type à appauvrissement (2) comportant un canal d'un premier type de conductivité, ledit transistor MIS étant formé dans une seconde région de puits (22) d'un second type de conductivité entre le côté de drain (24b) dudit premier transistor MIS (1) et une source électrique (24a) et sa grille étant connectée à ladite section de sortie (6), ladite seconde région de puits étant établie à un potentiel électrique égal à celui de sa source. 25 30 35
9. Dispositif à couplage de charge selon la revendication 2, comprenant le circuit de sortie selon la revendication 8, dans lequel : 40
 - ledit substrat semiconducteur (21) est d'un premier type de conductivité ; 45
 - ladite section de transfert de charges est formée dans une région de puits d'un second type de conductivité dans ledit substrat semiconducteur (21) ; 50
 - ledit moyen d'extraction de charges (10, 23, 55, 64, 74) est formé sur ledit substrat semiconducteur et au niveau de l'extrémité de ladite section de transfert de charges. 55
10. Dispositif à couplage de charge selon la revendication 9, dans lequel une source de courant constant (3 ; 33 ; 53 ; 63 ; 73) constituant le suiveur de source est constituée par un transistor NMOS comportant un canal d'un premier type de conductivité, ledit transistor NMOS étant formé dans une région de puits du second type de conductivité distincte desdites 59

régions de puits du second type de conductivité comportant lesdits premier et second transistors MIS.