

SEMICONDUCTOR STRUCTURE

FIELD OF THE INVENTION

The present invention is generally related to a semiconductor structure,
5 which particularly relates to the semiconductor structure with an anti-stress
zone.

BACKGROUND OF THE INVENTION

A conventional semiconductor structure 200 illustrated in Fig. 6
comprises a carrier 210, a first protective layer 220, a second protective
10 layer 230 and a third protective layer 240. The shape of the first protective
layer 220, the second protective layer 230 and the third protective layer 240
is quadrangle. Besides, the first protective layer 220, the second protective
layer 230 and the third protective layer 240 are disposed at the carrier 210
and arranged in a layer-by-layer stack. For mentioned features of those
15 protective layers, the stress of the semiconductor structure 200 likely
concentrates at a corner that is overlapped between the first protective layer
220 and the second protective layer 230 such that the corner might be
cracked or separated therefore lowering the production yield of the
semiconductor structure 200.

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SUMMARY

The primary object of the present invention is to provide a
semiconductor structure. A first anti-stress zone of a first surface of a first
protective layer prevents the stress from concentrating at a corner to avoid
cracks or separations occurred in the semiconductor structure.

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A semiconductor structure having at least one corner includes a carrier,
a first protective layer, a second protective layer and a third protective layer.

The carrier comprises a carrier surface having a protection-layered disposing zone and a protection-layered exposing zone located outside the protection-layered disposing zone. The first protective layer is disposed on the protection-layered disposing zone and comprises a first surface having a first disposing zone, at least one first anti-stress zone and a first exposing zone located outside the first disposing zone and the at least one first anti-stress zone. The at least one first anti-stress is located at the at least one corner. The second protective layer is disposed at the first disposing area and reveals the at least one first anti-stress zone and the first exposing zone. The second protective layer comprises a second surface, a first lateral surface and a second lateral surface, wherein the second surface comprises a second disposing zone and a second exposing zone located outside the second disposing zone. The first lateral surface comprises a first bottom edge, wherein the second lateral surface comprises a second bottom edge, and a first extension line extendedly formed from the first bottom edge intersects with a second extension line extendedly formed from the second bottom edge to form a first base point. The third protective layer is disposed at the second disposing zone and comprises a third lateral surface and a fourth lateral surface, the third lateral surface comprises a third bottom edge, and the fourth lateral surface comprises a fourth bottom edge. The third bottom edge is projected on the first surface of the first protective layer to form a first projection line situated on the first surface, and an extension line of the first projection line intersects with the second bottom edge of the second lateral surface to form a first intersection point. The fourth bottom edge is projected on the first surface of the first protective layer to form a second projection line situated on the first surface, and an

extension line of the second projection line intersects with the first bottom edge of the first lateral surface to form a second intersection point. A zone formed by connecting the first base point, the first intersection point and the second intersection point is the at least one first anti-stress zone. Via the at least one first anti-stress zone formed by connecting the first base point, the first intersection point and the second intersection point, the stress of the semiconductor structure does not concentrate at the at least one corner to prevent the at least one corner from cracks or separations.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective exploded view illustrating a semiconductor structure in accordance with a first embodiment of the present invention.

FIG. 2 is a perspective view illustrating the semiconductor structure in accordance with the first embodiment of the present invention.

FIG. 3 is a top view illustrating the semiconductor structure in accordance with the first embodiment of the present invention.

FIG. 4 is a perspective view illustrating a semiconductor structure in accordance with a second embodiment of the present invention.

FIG. 5 is a top view illustrating the semiconductor structure in accordance with the second embodiment of the present invention.

FIG. 6 is a perspective view illustrating a conventional semiconductor structure.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Figs. 1 and 2, a semiconductor structure 100 having at least one corner 100a in accordance with a first embodiment of the present invention includes a carrier 110, a first protective layer 120, a second protective layer 130, and a third protective layer 140. The carrier 110

comprises a carrier surface 111 having a protection-layered disposing zone 111a and a protection-layered exposing zone 111b located outside the protection-layered disposing zone 111a. The first protective layer 120 is disposed at the protection-layered disposing zone 111a and comprises a first surface 121 having a first disposing zone 121a, at least one first anti-stress zone 121b and a first exposing zone 121c located outside the first disposing zone 121a and the at least one first anti-stress zone 121b. The at least one first anti-stress zone 121b is located at the at least one corner 100a of the semiconductor structure 100. The second protective layer 130 is disposed at the first disposing zone 121a and reveals the at least one first anti-stress zone 121b and the first exposing zone 121c, and the second protective layer 130 comprises a second surface 131, a first lateral surface 132, a second lateral surface 133 and a connection surface 134 connected to the first lateral surface 132 and the second lateral surface 133. The second surface 131 comprises a second disposing zone 131a, at least one second anti-stress zone 131b and a second exposing zone 131c located outside the second disposing zone 131a and the at least one second anti-stress zone 131b. The at least one second anti-stress area 131b is located at a corner of the second disposing area 131a. The at least one second anti-stress zone 131b and the at least one first anti-stress zone 121b are both located at the at least one corner 100a of the semiconductor structure 100. In this embodiment, the area of the at least one first anti-stress zone 121b is not smaller than that of the at least one second anti-stress zone 131b.

With reference to Figs. 2 and 3, the first lateral surface 132 comprises a first bottom edge 132a, the second lateral surface 133 comprises a second bottom edge 133a, wherein a first extension line L1 extendedly formed from

the first bottom edge 132a intersects with a second extension line L2 extendedly formed from the second bottom edge 133a to form a first base point A1. In this embodiment, the first extension line L1 is perpendicular to the second extension line L2, and the first connection surface 134 is a flat surface.

With reference to Figs. 1, 2 and 3, the third protective layer 140 is disposed at the second disposing zone 131a and reveals the at least one second anti-stress zone 131b. Besides, the third protective layer 140 comprises a third lateral surface 141, a fourth lateral surface 142 and a second connection surface 143 connected to the third lateral surface 141 and the fourth lateral surface 142, wherein the third lateral surface 141 comprises a third bottom edge 141a, and the fourth lateral surface 142 comprises a fourth bottom edge 142a. The third bottom edge 141a is projected on the first surface 121 of the first protective layer 120 to form a first projection line P1 situated on the first surface 121, wherein an extension line extended from the first projection line P1 intersects with the second bottom edge 133a of the second lateral surface 133 to form a first intersection point I1. The fourth bottom edge 142a is projected on the first surface 121 of the first protective layer 120 to form a second projection line P2 situated on the first surface 121, wherein an extension line extended from the second projection line P2 intersects with the first bottom edge 132a of the first lateral surface 132 to form a second intersection point I2. A zone formed by connecting the first base point A1, the first intersection point I1 and the second intersection point I2 is the at least one first anti-stress zone 121b. In this embodiment, the second connection surface 143 is a flat surface.

With reference to Fig. 2, the third bottom edge 141a of the third lateral

surface 141 comprises a first point T1, and the fourth bottom edge 142a of the fourth lateral surface 142 comprises a second point T2. A third extension line L3 extendedly formed from the third bottom edge 141a intersects with a fourth extension line L4 extendedly formed from the fourth bottom edge 142a to form a second base point A2, and a zone formed by connecting the second base point A2, the first point T1 and the second point T2 is the at least one second anti-stress zone 131b. In this embodiment, a first distance D1 is spaced apart between the second base point A2 and the first point T1, a second distance D2 is spaced apart between the second base point A2 and the second point T2, and the first distance D1 is equal to the second distance D2.

In this invention, via the at least one first anti-stress zone 121b formed by connecting the first base point A1, the first intersection point I1 and the second intersection point I2, particularly, the first base point A1 formed by intersection between the first extension line L1 and the second extension line L2, the first intersection point I1 formed by intersection between the extension line of the first projection line P1 and the second bottom edge 133a, and the second intersection point I2 formed by intersection between the extension line of the second projection line P2 and the first bottom edge 132a, while the first protective layer 120, the second protective layer 130 and the third protective layer 140 are stackable to the carrier 110, the stress does not concentrate at the at least one corner 100a therefore preventing the at least one corner 100a of the semiconductor structure 100 from cracks or separations.

A semiconductor structure 100 is illustrated in Figs. 4 and 5 according to a second embodiment of the present invention. The primary difference

between the second embodiment and the first embodiment is that the first connection surface 134 and the second connection surface 143 are arc surfaces. The arc surfaces of the first connection surface 134 and the second connection surface 143 themselves also possess the function for preventing the stress of the semiconductor structure 100 from concentrating at the corner that is overlapped between the second protective layer 130 and the second protective layer 120 (adjacent to the at least one corner 100a). Therefore, cracks or separations likely occurred from the at least one corner 100a can be avoidable.

While this invention has been particularly illustrated and described in detail with respect to the preferred embodiments thereof, it will be clearly understood by those skilled in the art that it is not limited to the specific features and describes and various modifications and changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is:

1. A semiconductor structure having at least one corner includes:

- 5 a carrier having a carrier surface, the carrier surface comprises a protection-layered disposing zone and a protection-layered exposing zone located outside the protection-layered disposing zone;
- a first protective layer disposed at the protection-layered disposing zone and having a first surface, the first surface comprises a first disposing zone, at least one first anti-stress zone and a first exposing zone located outside the first disposing zone and the at least one first anti-stress zone,
- 10 the at least one first anti-stress zone is located at the at least one corner;
- a second protective layer disposed at the first disposing zone and revealing the at least one first anti-stress zone and the first exposing zone, the second protective layer comprises a second surface, a first lateral surface and a second lateral surface, the second surface comprises a
- 15 second disposing zone and a second exposing zone located outside the second disposing zone, the first lateral surface comprises a first bottom edge, the second lateral surface comprises a second bottom edge, wherein a first extension line extended from the first bottom edge intersects with a second extension line extended from the second bottom
- 20 edge to form a first base point; and
- a third protective layer disposed at the second disposing zone and having a third lateral surface and a fourth lateral surface, the third lateral surface comprises a third bottom edge, the fourth lateral surface comprises a fourth bottom edge, wherein the third bottom edge is projected on the
- 25 first surface of the first protective layer to form a first projection line situated on the first surface, an extension line of the first projection line

- intersects with the second bottom edge of the second lateral surface to form a first intersection point, wherein the fourth bottom edge is projected on the first surface of the first protective layer to form a second projection line situated on the first surface, an extension line of the second projection line intersects with the first bottom edge of the first lateral surface to form a second intersection point, and a zone formed by connecting the first base point, the first intersection point and the second intersection point is the at least one first anti-stress zone.
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2. The semiconductor structure in accordance with claim 1, wherein the first extension line is perpendicular to the second extension line.
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3. The semiconductor structure in accordance with claim 1, wherein the second surface of the second protective layer further comprises at least one second anti-stress zone located at a corner of the second disposing zone, the second exposing zone is located outside the at least one second anti-stress zone, the third protective layer reveals the at least one second anti-stress zone, the at least one second anti-stress zone and the at least one first anti-stress zone are located at the at least one corner, and the area of the at least one first anti-stress zone is not smaller than that of the at least one second anti-stress zone.
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4. The semiconductor structure in accordance with claim 3, wherein the third bottom edge of the third lateral surface comprises a first point, the fourth bottom edge of the fourth lateral surface comprises a second point, wherein a third extension line extended from the third bottom edge and a fourth extension line extended from the fourth bottom edge intersect to form a second base point, wherein a zone formed by connecting the second base point, the first point and the second point is
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the at least one second anti-stress zone.

5. The semiconductor structure in accordance with claim 4, wherein a first distance is spaced apart between the second base point and the first point, a second distance is spaced apart between the second base point and the second point, and the first distance is equal to the second distance.
6. The semiconductor structure in accordance with claim 1, wherein the second protective layer further comprises a first connection surface connected to the first lateral surface and the second lateral surface, and the first connection surface is a flat surface or an arc surface.
7. The semiconductor structure in accordance with claim 1, wherein the third protective layer further comprises a second connection surface connected to the third lateral surface and the fourth lateral surface, and the second connection surface is a flat surface or an arc surface.