

Description

The invention relates to a transconductance amplifier for converting an input voltage to an output current comprising a first (T_{01}) and a second (T_{02}) input transistor, each input transistor having an emitter area e_0 , the bases of the first and second input transistors constituting inputs for receiving the input voltage and the emitters of the first and second input transistors being connected to a current source, and further comprising at least a first output for the output current.

Such transconductance amplifiers, briefly referred to as transconductors, are suitable for general uses and in particular for use in filter circuits, multipliers and oscillators.

A transconductor is a voltage-controlled current source in which the proportionality factor between the output current and the input voltage is given by the transconductance. The simplest transconductor is a differential amplifier, by means of which a voltage applied between the bases is converted into two collector signal currents of opposite phase. In a differential amplifier these signal currents increase as a linear function of the input voltage over a small range only, so that the transconductance is only constant over a very small range of input voltage. The article "Bipolar Integration of analog gyrator and laguerre type filters (transconductor-capacitor filters)" in Proceedings ECCTD'83, September 1983, pages 107-110 describes a linearised transconductor which comprises two parallel-connected differential amplifiers, the transistors of each amplifier having different emitter areas and the bases and the collectors of two transistors having different emitter areas being interconnected. In the case of a suitable choice of the ratio between the emitter areas of the transistors, the linear range of this transconductor is approximately five times as large as that of a single differential amplifier. In addition, this known transconductor may be arranged to form a square-law transconductor, in which the output current increases as a square-law function of the input voltage over a specific range. In this case the collectors of the transistors whose bases are interconnected are not coupled to each other but are cross-coupled to the collector of the corresponding transistor of the other differential amplifier.

It is the object of the invention to provide a transconductor which enables both a linear and a square-law transconductor with a larger useful output-voltage range to be obtained.

The manner in which the components of a transconductor in accordance with the invention are arranged depends on whether the circuit is to be used as a linear transconductor, in which the output current increases, as far as possible, as a linear function of the input voltage, or as a square-law transconductor, in which the output current increases, as far as possible, as a square-law function of the input voltage. In the case of a linear transconductor a distinction should be made between class AB and class A operation of the transconductor. A class AB transconductor is to be understood to mean a transconductor whose bias current increases as the input voltage V_i increases, and a class A transconductor is to be understood to mean a transconductor whose bias current is independent of the input voltage V_i . In the transconductors in accordance with the invention it is possible to obtain an output-voltage range which is at least twice as large as that of the known transducers for any value of N by a suitable choice of the ratio between the emitter areas of the transistors and the ratio between the resistance values.

A class AB linear transconductor in accordance with the invention may be characterized in that

- a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided in a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_N$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
- the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistors $T_1, T_2, \dots, T_{N-1}, T_N$ having respective emitter areas $e_1, e_2, \dots, e_{N-1}, e_N$; the group transistors having their emitters directly connected to the current source, their collectors connected to a power-supply terminal;
- the collectors of the first and second input transistors constitute the first and a second output of the amplifier.

The difference between the collector currents of the input transistors then increases as a linear function of the input voltage over a specific range. As a result of the class AB operation of the circuit the bias current is comparatively small for low input voltages. As a result of this the noise level and the d.c. offset at low input voltages are small.

It is to be noted that apparently the construction of such a class AB transconductor for which $N=1$, and the resistance value $W_1=0$ bears some resemblance to the differential amplifier shown in Fig. 1 of European Patent Application 0157447. In said differential amplifier the bias current also increases as the input voltage increases. However, this is not a step aimed at increasing the linear range but at increasing the slow rate, i.e. the maximum rate at which the output signal of the amplifier can vary in the case of capacitive loading. Moreover, the amplifier is a negative-feedback differential amplifier in which the emitters, in contradistinction to the transconductor in accordance with the invention, are not connected directly to the bias-current source but via a resistor. A transconductor in accordance with the invention maintains its linearity over a wide range of bias current, whilst the circuit for increasing the slow rate only operates in a small current range around the value for which the circuit has been designed.

A class A linear transconductor in accordance with the invention may be characterized in that

- a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided in a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
- the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistor pairs $T_1, T_2, \dots, T_{N-1}, T_N$; the group transistor pairs having their emitters directly connected to the current source, each of the group transistor pairs comprising two parallel-connected transistors each having respective emitter areas $\theta_1, \theta_2, \dots, \theta_{N-1}, \theta_N$, the collectors of the first transistors of the pairs being connected to the collector of the first input transistor and the collectors of the second transistors of the pairs being connected to the collector of the second input transistor, and in that the collector of the first input transistor constitutes the first output of the transconductance amplifier.

The output current in each of the collectors of the input transistor then varies as a linear function of the input voltage over a specific range, so that each of these collectors may constitute an output of the transconductor.

A square-law transconductor in accordance with the invention may be characterized in that

- a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided in a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
- the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistors $T_1, T_2, \dots, T_{N-1}, T_N$ having respective emitter areas $\theta_1, \theta_2, \dots, \theta_{N-1}, \theta_N$; the group transistors having their emitters directly connected to the current source, their collectors connected to the first output of the transconductance amplifier.

The output current in the first output then decreases as a square-law function of the input voltage over a specific range. If, in accordance with the further embodiment, the collectors of the input transistors are interconnected these collectors may constitute a second output of the transconductor because the current in this output then increases as a square-law function of the input voltage.

Embodiments of the invention will now be described in more detail, by way of example, with reference to the accompanying drawings in which:

Fig. 1 is the circuit diagram of a class AB linear transconductor in accordance with the invention,

Fig. 2 shows the circuit diagram of a class A transconductor in accordance with the invention,

Fig. 3 is the circuit diagram of a square-law transconductor in accordance with the invention,

Fig. 4 shows a class AB linear transconductor in accordance with a first embodiment,

Fig. 5 shows a class AB linear transconductor in accordance with a second embodiment,

Fig. 6 shows a class AB linear transconductor in accordance with a third embodiment,

Fig. 7 shows a class AB linear transconductor in accordance with a fourth embodiment,

Fig. 8 shows a class AB linear transconductor in accordance with a fifth embodiment,
 Fig. 9 shows a class A linear transconductor in accordance with a first embodiment,
 Fig. 10 shows a class A linear transconductor in accordance with a second embodiment,
 Fig. 11 shows a square-law transconductor,

Fig. 12 shows a base-current compensation circuit for a transconductor in accordance with the invention, and

Fig. 13 shows a series arrangement of two transconductors in accordance with the invention.

Fig. 1 is the circuit diagram of a class-AB linear transconductor in accordance with the invention. Between a first power-supply terminal 1 and a second power-supply terminal 2 the transconductor comprises two input transistors T_{01} and T_{02} whose bases 3 and 4 constitute the inputs for receiving an input voltage V_i and whose emitters are connected to the output 5 of a current source 6 which can supply a current I . A voltage divider is arranged between the bases 3 and 4 and comprises $2N+1$ resistors $R_0, R_1, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_1, R_0$ having resistance values W_k , where $k = 0, 1, \dots, N$. The $2N$ junction points $a_1, \dots, a_N, a_N, \dots, a_1$ are connected to bases of the transistors $T_1, \dots, T_N, T_N, \dots, T_1$ having emitter areas e_k , where $k = 1, \dots, N$. The emitters of these $2N$ transistors are connected to the output 5 of the current source 6. The collectors of the transistors T_{01} and T_{02} constitute the outputs 7 and 8 of the transconductor, whilst the collectors of the transistors $T_1, \dots, T_N, T_N, \dots, T_1$ are connected to the positive power-supply terminal 1. In the quiescent state the transistors $T_1, \dots, T_N, T_N, \dots, T_1$ drain a part of the current I from the current source 6, so that the bias current through the transistors T_{01} and T_{02} is only a fraction of the current I . As the input voltage V_i increases the transistors $T_1, \dots, T_N, T_N, \dots, T_1$ draw an increasingly smaller part of the current I , so that the bias current through one of the transistors T_{01} and T_{02} increases. The advantage of such a bias current which increases with the input voltage is that for small input voltages V_i there will be less noise and less offset than in the case of a constant bias current. For each value N the ratio between the emitter areas e_k , where $k = 0, \dots, N$, of the transistors $T_{01}, T_1, \dots, T_N, T_N, \dots, T_1, T_{02}$ and the ratio between the resistance values W_k ($k = 0, \dots, N$) of the resistors $R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$ can be selected in such a way that the difference between the collector currents of the transistors T_{01} and T_{02} has a linear relationship with the input voltage V_i over an as large as possible range. This will be explained hereinafter by means of some examples of class AB linear transconductors. The difference between the collector currents of the transistors T_{01} and T_{02} can be obtained by means of a differential-to-single-ended converter 9 of arbitrary construction. This converter 9 may comprise, for example, a current mirror, of which the simplest version is shown in the Figure and which comprises a diode-connected PNP transistor T_{01} and a PNP transistor T_{02} connected in parallel therewith. The difference between the collector currents of the transistors T_{01} and T_{02} can then be taken from the output 8.

Fig. 2 shows the circuit diagram of a class A linear transconductor in accordance with the invention. Identical parts bear the same reference numerals as in Fig. 1. The transistors $T_1, \dots, T_N, T_N, \dots, T_1$ are now each constructed as two parallel-connected identical transistors T_{KA} and T_{KB} with $K = 1, \dots, N$, the collectors of all the transistors T_{KA} being connected to the collector of the transistor T_{01} and the collectors of all the transistors T_{KB} being connected to the collector of transistor T_{02} . As a result of these collector connections the d.c. component of the currents on the output 7 and 8 is independent of the input voltage V_i , which means that the circuit operates in class A. The ratio between the emitter areas e_k , where $K = 0, \dots, N$, of the transistors $T_{01}, T_1, \dots, T_N, T_N, \dots, T_1, T_{02}$ and the ratio between the resistance values W_K , where $K = 0, \dots, N$, of the resistors $R_0, \dots, R_N$ may be selected in the same way as in the circuit of Fig. 1. In that case the current at the output 7 increases as a linear function of the input voltage V_i and the current on the output 8 decreases as a linear function of the input voltage V_i . This will be explained in more detail by means of example. It has the advantage that both the output 7 and the output 8 may be used directly as the output of the circuit. This makes the circuit very suitable for operation at high frequencies, because it is not necessary to use a differential-to-single-ended converter comprising PNP transistors, which generally has less satisfactory high-frequency properties. In the Figure the output current appears on the output 7. The output 8 is connected to the first power-supply terminal 1. However, it is alternatively possible to employ the difference between the currents on the outputs 7 and 8 as the output current of the circuit, which difference can again be obtained by means of a differential-to-single-ended converter.

Fig. 3 shows the circuit diagram of a square-law transconductor in accordance with the invention. Identical parts bear the same reference numerals as in Fig. 1. The collectors of the transistors T_{01} and T_{02} are now connected to an output 7 and the collectors of the transistors $T_1, \dots, T_N, T_N, \dots, T_1$ are connected to an output 8. For any value of N the ratio between the emitter areas e_k , where $K = 0, \dots, N$, of the transistors $T_{01}, T_1, \dots, T_N, T_N, \dots, T_1, T_{02}$ and the ratio between the resistance values W_K ($K = 0, \dots, N$) of the resistors $R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$ can be selected in such a way that the current on each of the outputs 7 and 8 has a square-law relationship with the input voltage V_i over an as large as possible range. Both the output 7

and the output 8 may serve as the output of the circuit, the output which is not used being connected to, for example, the positive power-supply terminal 1. However, it is alternatively possible to employ the difference between the currents on the outputs 7 and 8 as the output current of the circuit, which difference can again be obtained by means of a differential-to-single-ended converter.

Fig. 4a shows a class AB linear transconductor in accordance with a first embodiment, which is the simplest embodiment. This embodiment corresponds to the circuit shown in Fig. 1 if $N = 1$, the resistor R_1 has a resistance value $W_1 = 0$ and the two junction points a_1 are commoned to form one junction point. Between the bases 3 and 4 of the transistors T_{o1} and T_{o2} voltage divider comprising two resistors R_o is arranged, the junction point of these resistors being connected to two transistors T_1 each having an emitter area e_1 . In the present embodiment these transistors T_1 are suitably commoned to form a single transistor having an emitter area $2e_1$, as is shown in Fig. 4b. If the collector currents of the transistors T_{o1} , T_1 and T_{o2} are I_1 , I_2 and I_3 respectively the following relationship applies to the circuit shown in Fig. 4b:

$$I_1 + I_2 + I_3 = I \quad (1)$$

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When the input voltage is V_i a voltage V_{i2} appears between the bases of the transistors T_{o1} and T_1 and between the bases of the transistors T_1 and T_{o2} as a result of the voltage division by the resistors R_o . If the ratio between the emitter areas of the transistors T_1 and T_{o1} or T_{o2} is $2e_1:e_o=n:1$, it follows from the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor that:

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$$\frac{I_1}{I_2/n} = \frac{I_2/n}{I_3} = \exp \left(\frac{V_{i2}}{2KT} \right) \quad (2)$$

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If

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$$\frac{V_{i2}}{2KT} = x$$

It follows from equations (1) and (2) that:

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$$\frac{I_1}{I} = \frac{\exp(x)}{(n + \exp(x) + \exp(-x))} \quad (3)$$

and

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$$\frac{I_3}{I} = \frac{\exp(-x)}{(n + \exp(x) + \exp(-x))} \quad (4)$$

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It follows from equations (3) and (4) that the difference between the collector currents of the transistors T_{o1} and T_{o2} is:

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$$\frac{I_1 - I_3}{I} = \frac{\exp(x) - \exp(-x)}{(n + \exp(x) + \exp(-x))} \quad (5)$$

Series expansion of the exponential functions yields:

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$$\frac{I_1 - I_3}{I} = \frac{d x (1 + \frac{x^2}{3!} + \frac{x^4}{5!} + \dots)}{(1 + \frac{dx^2}{2!} + \frac{dx^4}{4!} + \dots)} \quad (6)$$

where

$$d = \frac{2}{n+2}$$

which may be reduced to

$$\frac{I_1 - I_3}{I} = d(x + (\frac{1}{6} - \frac{d}{2})x^3 + (\frac{1}{120} - \frac{d}{8} + \frac{d^2}{4})x^5 + \dots) \quad (7)$$

If $d = \frac{1}{3}$, i.e. for $n = 4$, this equation provides maximum linearity. Thus, for an emitter area of the transistor T_1 which is $4x$ as large as that of the transistors T_{o1} and T_{o2} the difference between the collector currents of the transistors T_{o1} and T_{o2} increases as a linear function of the input voltage V_i over an as large as possible range. In the linear range the following approximation is valid:

$$I_1 - I_3 = I \cdot \frac{V_i \cdot q}{6KT} \quad (8)$$

from which it follows that the transconductance $G = (I_1 - I_3)/V_i$ is directly proportional to the current I from the current source 6, so that the transconductance can be varied by varying the current I . This renders the circuit particularly suitable for use as a variable resistance ($R = 1/G$) in filter arrangements, enabling the magnitude of the RC time constants to be varied.

For a ratio between the emitter areas $2e_1:e_o = 4:1$ the transistor T_1 draws $2/3$ of the current I from the current source 6 for small input voltages V_i , so that the effective bias current is then equal to $I/3$. At increasing input voltages this bias current increases, which has the advantage that for low input voltages the arrangement exhibits a lower noise level and a lower d.c. offset than the known transducers.

Fig. 5 shows a class AB linear transconductor in accordance with a second embodiment, identical parts bearing the same reference numerals as in Fig. 4a. This embodiment corresponds to the circuit of Fig. 1 in the case that $N=1$ and the resistor R_1 has a resistance $W_1 \neq 0$. In comparison with the circuit shown in Fig. 4a a resistor R_1 is arranged between the bases of the transistors T_1 . In a similar way as for the circuit of Fig. 4 it can be found for the circuit shown in Fig. 5 that the difference between the collector currents of the transistors T_{o1} and T_{o2} and the input voltages V_i are in a linear relationship over an as large as possible range, if the ratio between the emitter areas of the transistors T_1 and T_o is substantially equal to $e_1:e_o = 5:1$ and the ratio between the resistance values of the resistors R_1 and R_o is substantially equal to $W_1:W_o = 8.5$. It is to be noted that in order to obtain a ratio containing only integers the resistance ratio may be selected to be $W_1:W_o = 2:1$, which results in overcompensation.

Fig. 6 shows a class AB linear transconductor in accordance with a third embodiment. This embodiment corresponds to the arrangement shown in Fig. 1 in the case that $N = 2$, the resistor R_2 has a resistance value $W_2 = 0$ and the two junction points a_2 are commoned to form a single junction point. For this circuit it is possible to demonstrate that an optimum linear relationship between the output current $I_1 - I_3$ and the input voltage V_i is obtained for a ratio between the emitter areas of the transistors T_2 , T_1 and T_o which is substantially equal to $e_2:e_1:e_o = 32:49:9$ and for a ratio between the resistance values of the resistors R_1 and R_o which is substantially equal to $W_1:W_o = 1.9:1$. In the present embodiment the emitter-area ratio and the resistance ratio may be selected to equal $e_2:e_1:e_o = 1.6:4$ and $W_1:W_o = 2:1$ respectively in order to obtain easy-to-realise ratios. In this embodiment the transistors T_2 may be combined to form a single transistor having an emitter area equal to $2e_2$.

Fig. 7 shows a class AB linear transconductor in accordance with a fourth embodiment, which corresponds to the arrangement shown in Fig. 1 in the case that $N = 2$ and the resistor R_2 has a resistance

value W_2 unequal to zero. In order to obtain an as large as possible range within which the output current $I_1 - I_3$ increases as a linear function of the input voltage V_i , the emitter areas of the transistors T_2 , T_1 and T_0 should be proportioned in such a way that $e_2:e_1:e_0=25:17:3$ and the resistance values of the resistors R_2 , R_1 and R_0 should have a ratio which is substantially equal to $W_2:W_1:W_0=2.4:2:1$.

Fig. 8 shows a class AB linear transconductor in accordance with a fifth embodiment which is identical to the arrangement of Fig. 1 for $N = 3$ and a resistance value of the resistor R_3 which is $W_3 = 0$. In the present embodiment the linear range is as large as possible if the ratio between the emitter areas of the transistor, T_3 , T_2 , T_1 and T_0 is substantially equal to $e_3:e_2:e_1:e_0=5:9:6:1$ and the ratio between the resistance values of the resistors R_2 , R_1 and R_0 is substantially equal to $W_2:W_1:W_0=47:36:17$. In the present embodiment the transistors T_3 are preferably also combined to form a single transistor.

The properties of the class AB linear transconductor in accordance with the embodiment shown in Figs. 4 to 8 are given in the following Table. The Table also gives the properties of a normal differential amplifier and the transconductor in accordance with the aforementioned article in the Proceedings ECCTD'83.

Type of transconductor	$\Delta = 1\%$ (mV)	C.E. (%)	S
Differential amplifier (prior art)	6	6	1
Proc. ECCTD'83 (prior art)	30	40	1
Figure 4	60	40	1/3
Figure 5	142	47	1/6
Figure 6	255	51	1/10
Figure 7	400	53	1/15
Figure 8	575	55	1/21

For each transconductor the above Table consecutively gives : the voltage for which the departure from the linear characteristic has increased to 1 %; the current efficiency (C.E.) which indicates the fraction of the current I to which the signal current is equal when the 1 % linearity deviation is reached, and the effective bias current (S) for low input voltages.

It follows from the Table that the simplest embodiment of the class AB transconductor (Fig. 4) already has a linear voltage range which is 2 x as large as that of the known transconductor and a linear voltage range which is even 10 x as large as that of a normal differential amplifier. Thin linear range becomes increasingly larger for the consecutive embodiments. The effective bias current S then decreases, which means that the noise level and the d.c. offset are also further reduced.

Fig. 9 shows a class A linear amplifier in accordance with a first embodiment, in which Figure identical parts bear the same reference numerals as in Fig. 2. This embodiment corresponds to the arrangement shown in Fig. 2 in the case that $N = 1$, the resistor R_1 has a resistance value $W_1 = 0$ and the junction points a_1 are commoned to form a single junction point. One transistor T_1 then constitutes the transistor T_{1A} whose collector is connected to the collector of the transistor T_{01} and the other transistor T_1 constitutes the transistor T_{1B} whose collector is connected to the collector of the transistor T_{02} . The ratio between the emitter areas of the transistors T_{1A} and T_{01} and those of T_{1B} and T_{02} is then $e_1:e_0=2:1$ and is consequently equal to that used in Fig. 4. The fact that the currents on the outputs 7 and 8 then each increase as a linear function of the input voltage can be demonstrated as follows. The difference between the output currents as linear because, as compared with the circuit shown in Fig. 4a, a similar current is added to the currents I_1 and I_3 . Further, the sum of the output currents on the outputs 7 and 8 is equal to the current I from the current source 6, which means that the output currents each should then also increase as a linear function of the input voltage. As a result of this, both the current in output 7 and the current in output 8 can be used directly as the output current of the transconductor. If one of the outputs is employed, the other output may be connected to, for example, the first power-supply terminal. However, it is alternatively possible to employ the difference between the currents on said outputs as the output current of the circuit. The linear range of the arrangement is the same as that of the arrangement shown in Fig. 4. The d.c. component in each of the output currents is constant and is $I/2$. For small input voltages the noise and the d.c. offset are therefore higher than in the corresponding class AB transconductor shown in Fig. 4.

Fig. 10 shows a class A linear transconductor in accordance with a second embodiment. This arrangement corresponds to the arrangement shown in Fig. 2 in the case that $N = 1$ and the resistor R_1 has a resistance W_1 unequal to zero. Each of the transistors T_{1A} and T_{1B} then has an emitter area equal to half the emitter area of the transistor T_1 used in the arrangement shown in Fig. 5.

In the same way as in the class AB transconductors the arrangement shown in Fig. 2 may be constructed as a higher-order class A linear transconductor. The linear range then increases in the same

way as specified in the above Table for the class AB transconductors.

Fig. 11 shows a square-law transconductor in accordance with a first embodiment, identical parts bearing the same reference numerals as in Fig. 3. This arrangement corresponds to the arrangement shown in Fig. 3 in the case that $N = 1$ and the resistor R_1 has a resistance $W_1 = 0$. Suitably, the transistors T_1 are combined to form a single transistor having an emitter area $2e_1$. If the collector currents of the transistors T_{o1} , T_1 and T_{o2} are again I_1 , I_2 and I_3 respectively the circuit complies with:

$$I_1 + I_2 + I_3 = I \quad (9)$$

For an input voltage V_i a voltage V_{i2} will appear between the bases of the transistors T_{o1} and T_1 and between the bases of the transistors T_1 and T_{o2} as a result of the voltage division by the resistors R_o . If the ratio between the emitter areas of the transistors T_1 and those of the transistors T_{o1} and T_{o2} is $2e_1:e_o = n:1$, the following is valid:

$$\frac{I_1}{I_2/n} = \frac{I_2/n}{I_3} = \exp\left(\frac{V_i}{2} \cdot \frac{q}{kT}\right) \quad (10)$$

For

$$x = \frac{V_i \cdot q}{2kT}$$

It follows from equations (9) and (10) that:

$$\frac{I_2}{I} = \frac{n}{n + \exp(x) + \exp(-x)} \quad (11)$$

By means of a series expansion of the exponential functions it can be demonstrated, in a similar way as for the arrangement shown in Fig. 4b, that the relationship between the output current I_2 on output 8 decreases as a square-law function of the input voltage over an as large as possible range if the emitter-area ratio is substantially equal to $2e_1:e_o = 10:1$. In that case the current $I_1 + I_3$ on the output 7 increases as a square-law function of the input voltage V_i . Therefore, not only the current on output 7 but also the current on output 8 may be utilized as the output current of the arrangement. However, it is alternatively possible to take the difference of these currents as the output current. The purely quadratic range of the transconductor is substantially twice as large as that of the known transconductor.

For the embodiments of a square-law transconductor with values of $N > 1$ it is possible, in the same way as for the arrangement shown in Fig. 11, to find a ratio between the emitter areas of the transistors and a resistance ratio for which the square-law range is as large as possible.

The invention is not limited to the embodiments described above. Within the scope of the present invention many modifications are obvious to those skilled in the art. For example, the impedances of the voltage dividers in the above embodiments are not limited to pure resistors. In parallel with the resistors it is possible to arrange, for example, capacitors in order to improve the high-frequency behaviour of the arrangements. In addition the transistors shown in the above embodiments may be driven by buffer transistors. These transistors may be employed in a suitable manner in order to reduce the influence of the base currents of the transistors and hence the voltage drop across the voltage-divider resistors on the operation of the arrangement. Another method of reducing this influence will be described with reference to Fig. 12, which illustrates this possibility for the embodiment shown in Fig. 4b. Identical parts bear the same reference numerals as in Fig. 4b. The base currents for the transistors T_{o1} , T_1 and T_{o2} are supplied by a current source 15 which can supply a current I/β , where β is the current-gain factor of the transistors T_{o1} , T_1 and T_{o2} . The current I/β is applied to a dividing circuit comprising three PNP transistors T_{20} , T_{21} and T_{22} having the same emitter-area ratio as the transistors T_{o1} , T_1 and T_{o2} . Consequently, the collector currents of the transistors T_{20} , T_{21} and T_{22} are equal to the base currents of the transistors T_{o1} , T_1 and T_{o2} . Further, the input voltage range of the transconductor can be extended by not applying the total input voltage but by applying, via a voltage divider, a fraction of the total input voltage to the inputs of the transconductor. This

results in a reduction of the effective transconductance. The effective transconductance can also be reduced by utilising only a part of the output current by means of a current divider. In order to increase the output voltage range it is further possible to arrange two or more transconductors "in series". Fig. 13 illustrates this for the transconductor shown in Fig. 9. Corresponding parts of the second transconductor are primed in this Figure. As a result of the voltage division by the resistors R_0 half the input voltage appears between the bases of the transistors T_{01} and T_{02} and the bases of the transistors T_{01}' and T_{02}' , which voltages are converted into output currents of opposite phase by each of the transconductors. The corresponding outputs of the two transconductors are interconnected, so that the corresponding output currents are added to each other.

Claims

1. A transconductance amplifier for converting an input voltage to an output current comprising a first (T_{01}) and a second (T_{02}) input transistor, each input transistor having an emitter area e_0 , the bases of the first and second input transistors constituting inputs for receiving the input voltage and the emitters of the first and second input transistors being connected to a current source, and further comprising at least a first output for the output current, characterized in that:
 - a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided into a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
 - the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistors $T_1, T_2, \dots, T_{N-1}, T_N$ having respective emitter areas $e_1, e_2, \dots, e_{N-1}, e_N$; the group transistors having their emitters directly connected to the current source, their collectors connected to a power-supply terminal;
 - the collectors of the first and second input transistors constitute the first and a second output of the amplifier.
2. A transconductance amplifier as claimed in Claim 1, characterized in that for a resistance value W_N of the central impedance R_N equal to zero the two junction points a_N are commoned to form a single junction point a_N .
3. A transconductance amplifier for converting an input voltage to an output current comprising a first (T_{01}) and a second (T_{02}) input transistor, each input transistor having an emitter area e_0 , the bases of the first and second input transistors constituting inputs for receiving the input voltage and the emitters of the first and second input transistors being connected to a current source, and further comprising at least a first output for the output current, characterized in that:
 - a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided into a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
 - the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistor pairs $T_1, T_2, \dots, T_{N-1}, T_N$; the group transistor pairs having their emitters directly connected to the current source, each of the group transistor pairs comprising two parallel-connected transistors each having respective emitter areas $e_1, e_2, \dots, e_{N-1}, e_N$, the collectors of the first transistors of the pairs being connected to the collector of the first input



results in a reduction of the effective transconductance. The effective transconductance can also be reduced by utilising only a part of the output current by means of a current divider. In order to increase the output voltage range it is further possible to arrange two or more transconductors "in series". Fig. 13 illustrates this for the transconductor shown in Fig. 9. Corresponding parts of the second transconductor are primed in this Figure. As a result of the voltage division by the resistors R_0 , half the input voltage appears between the bases of the transistors T_{01} and T_{02} and the bases of the transistors T_{01}' and T_{02}' , which voltages are converted into output currents of opposite phase by each of the transconductors. The corresponding outputs of the two transconductors are interconnected, so that the corresponding output currents are added to each other.

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Claims

1. A transconductance amplifier for converting an input voltage to an output current comprising a first (T_{01}) and a second (T_{02}) input transistor, each input transistor having an emitter area e_0 , the bases of the first and second input transistors constituting inputs for receiving the input voltage and the emitters of the first and second input transistors being connected to a current source, and further comprising at least a first output for the output current, characterized in that:
 - a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided into a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
 - the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistors $T_1, T_2, \dots, T_{N-1}, T_N$ having respective emitter areas $e_1, e_2, \dots, e_{N-1}, e_N$; the group transistors having their emitters directly connected to the current source, their collectors connected to a power-supply terminal;
 - the collectors of the first and second input transistors constitute the first and a second output of the amplifier.
2. A transconductance amplifier as claimed in Claim 1, characterized in that for a resistance value W_N of the central impedance R_N equal to zero the two junction points a_N are commoned to form a single junction point a_N .
3. A transconductance amplifier for converting an input voltage to an output current comprising a first (T_{01}) and a second (T_{02}) input transistor, each input transistor having an emitter area e_0 , the bases of the first and second input transistors constituting inputs for receiving the input voltage and the emitters of the first and second input transistors being connected to a current source, and further comprising at least a first output for the output current, characterized in that:
 - a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided into a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
 - the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistor pairs $T_1, T_2, \dots, T_{N-1}, T_N$; the group transistor pairs having their emitters directly connected to the current source, each of the group transistor pairs comprising two parallel-connected transistors each having respective emitter areas $e_1, e_2, \dots, e_{N-1}, e_N$, the collectors of the first transistors of the pairs being connected to the collector of the first input



transistor and the collectors of the second transistors of the pairs being connected to the collector of the second input transistor, and in that the collector of the first input transistor constitutes the first output of the transconductance amplifier.

- 5 4. A transconductance amplifier as claimed in Claim 3, characterized in that the collector of the second input transistor constitutes a second output of the transconductance amplifier.
5. A transconductance amplifier as claimed in Claim 3 or 4, characterized in that for a resistance value W_N of the central impedance R_N equal to zero the two junction points a_N are commoned to form a single a
10 compound transistor.
6. A transconductance amplifier for converting an input voltage to an output current comprising a first (T_{01}) and a second (T_{02}) input transistor, each input transistor having an emitter area e_o , the bases of the first and second input transistors constituting inputs for receiving the input voltage and the emitters of the first and second input transistors being connected to a current source, and further comprising at least a first output for the output current, characterized in that:
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 - a series arrangement of $2N+1$ impedances ($R_0, \dots, R_{N-1}, R_N, R_{N+1}, \dots, R_0$) is coupled between the bases of the first (T_{01}) and second (T_{02}) input transistor, N being an integer number greater than or equal to 1; the series arrangement being subdivided into a first and a second group of N group impedances $R_0, R_1, \dots, R_{N-1}$ having respective resistance values $W_0, W_1, \dots, W_{N-1}$ and a central impedance R_N having a resistance value W_N ; the group impedances of each group being interconnected in $N-1$ junction points $a_1, a_2, \dots, a_k, \dots, a_{N-1}$, a_k being the junction point of group impedance R_k and R_{k+1} , where k is an integer running from $k=1$ to $k=N-1$; the impedance R_{N-1} of each group being connected to the central impedance R_N in a junction point a_N ; the group impedance R_0 of the first and second group being connected to the base of the first and second input transistor respectively;
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 - the $N-1$ junction points $a_1, \dots, a_{N-1}$ and the junction point a_N of each group are connected to bases of N respective group transistors $T_1, T_2, \dots, T_{N-1}, T_N$ having respective emitter areas $e_1, e_2, \dots, e_{N-1}, e_N$; the group transistors having their emitters directly connected to the current source, their collectors connected to the first output of the transconductance amplifier.
7. A transconductance amplifier as claimed in Claim 6, characterized in that the collectors of the first and second input transistors are connected to a second output of the transconductance amplifier.
8. A transconductance amplifier as claimed in Claim 6 or 7, characterized in that for a resistance value W_N of the central impedance R_N equal to zero the two junction points a_N are commoned to form a single junction point a_N .
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9. A transconductance amplifier as claimed in Claim 2 or 5, characterized in that for $N=1$ the ratio between the emitter areas is substantially equal to $e_1:e_o=2:1$.
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10. A transconductance amplifier as claimed in Claim 2 or 5, characterized in that for $N=2$ the ratio between the emitter areas is substantially equal to $e_2:e_1:e_o=32:49:9$ and the ratio between the resistance values is substantially equal to $W_1:W_o=1.9:1$.
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11. A transconductance amplifier as claimed in Claim 2 or 5, characterized in that for $N=3$ the ratio between the emitter areas is substantially equal to $e_3:e_2:e_1:e_o=5:9:8:1$ and the ratio between the resistance values is substantially equal to $W_2:W_1:W_o=47:36:17$.
12. A transconductance amplifier as claimed in Claim 1, characterized in that for $N=1$ the ratio between the emitter areas is substantially equal to $e_1:e_o=5:1$ and the ratio between the resistance values is substantially equal to $W_1:W_o=8:5$.
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13. A transconductance amplifier as claimed in Claim 1, characterized in that for $N=2$ the ratio between the emitter areas is substantially equal to $e_2:e_1:e_o=25:17:3$ and the ratio between the resistance values is substantially equal to $W_2:W_1:W_o=2.4:2:1$.
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14. A transconductance amplifier as claimed in Claim 8, characterized in that for $N=1$ the ratio between the



emitter areas is substantially equal to $e_1:e_0 = 5:1$.

Revendications

1. Amplificateur de conductance de transfert pour convertir une tension d'entrée en un courant de sortie comportant un premier transistor d'entrée (T_{01}) et un deuxième transistor d'entrée (T_{02}), chaque transistor d'entrée présentant une surface d'émetteur e_0 , les bases des premier et deuxième transistors d'entrée constituant les entrées pour la réception de la tension d'entrée et les émetteurs des premier et deuxième transistors d'entrée étant connectés à une source de courant, et comportant en outre au moins une entrée de sortie pour le courant de sortie, caractérisé en ce que
 - un montage en série de deux $2N+1$ impédances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) est couplé entre les bases des premier (T_{01}) et deuxième (T_{02}) transistors d'entrée, N étant un nombre entier supérieur ou égal à 1, le montage en série étant divisé en un premier groupe et un deuxième groupe de N impédances de groupe $R_0, R_1, \dots, R_{N-1}$ présentant des valeurs de résistance respectives $W_0, W_1, \dots, W_{N-1}$ et une impédance centrale R_N présentant une valeur de résistance W_N ; les impédances de groupe de chaque groupe étant interconnectées à $N-1$ points de jonction $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k, a_{N-1}, a_k$ étant le point de jonction des impédances de groupe R_k et R_{k+1} , k étant un nombre entier allant de $k=1$ à $k=N-1$; l'impédance R_{N-1} de chaque groupe étant connectée à une impédance centrale R_N à un point de jonction a_N ; l'impédance de groupe R_0 des premier et deuxième groupes étant connectée à la base respectivement des premier et deuxième transistors d'entrée;
 - les $N-1$ points de jonction $a_1, \dots, a_{N-1}$ et le point de jonction a_N de chaque groupe sont connectés aux bases de N transistors de groupe respectifs $T_1, T_2, \dots, T_{N-1}, T_N$ présentant des surfaces d'émetteur respectives $e_1, e_2, \dots, e_{N-1}, e_N$, les émetteurs des transistors de groupe étant connectés de façon directe à la source de courant, leurs collecteurs étant connectés à une borne d'alimentation;
 - les collecteurs des premier et deuxième transistors d'entrée constituant les première et deuxième sorties de l'amplificateur.
2. Amplificateur de conductance de transfert selon la revendication 1, caractérisé en ce que pour une valeur ohmique W_N de l'impédance centrale R_N égale à zéro, les deux points de jonction a_N sont combinés de façon à former un seul point de jonction a_N .
3. Amplificateur de conductance de transfert pour convertir une tension d'entrée en un courant de sortie comportant un premier transistor d'entrée (T_{01}) et un deuxième transistor d'entrée (T_{02}), chaque transistor d'entrée présentant une surface d'émetteur e_0 , les bases des premier et deuxième transistors d'entrée constituant les entrées pour la réception de la tension d'entrée et les émetteurs des premier et deuxième transistors d'entrée étant connectés à une source de courant et comportant en outre au moins une entrée de sortie pour le courant de sortie, caractérisé en ce que
 - un montage en série de $2N+1$ impédances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) est couplé entre les bases d'un premier (T_{01}) et deuxième (T_{02}) transistor d'entrée, N étant un nombre entier supérieur ou égal à 1; le montage en série étant subdivisé en un premier groupe et un deuxième groupe de N impédances de groupe $R_0, R_1, \dots, R_{N-1}$ présentant des valeurs de résistance respectives $W_0, W_1, \dots, W_{N-1}$ et une impédance centrale R_N présentant une valeur de résistance W_N ; les impédances de groupe de chaque groupe étant interconnectées à $N-1$ points de jonction $a_1, 2, \dots, a_k, \dots, a_{N-1}, a_k$ étant le point de jonction de l'impédance de groupe R_k et r_{k+1} , k étant un nombre entier allant de $k = 1$ à $K=N-1$; l'impédance R_{N-1} de chaque groupe étant connectée à l'impédance centrale R_N à un point de jonction a_N ; l'impédance de groupe R_0 des premier et deuxième groupes étant connectée à la base respectivement des premier et deuxième transistors d'entrée,
 - les $N-1$ points de jonction $a_1, \dots, a_{N-1}$ et le point de jonction a_N de chaque groupe sont connectés aux bases de N paires de transistor de groupe respectifs $T_1, T_2, \dots, T_{N-1}$, les émetteurs des paires de transistors de groupe étant connectés de façon directe à la source de courant, chaque paire de transistors de groupe comportant deux transistors montés en parallèle, chacun présentant une surface d'émetteur respective $e_1, e_2, \dots, e_{N-1}, e_N$, les collecteurs des premiers transistors de la paire étant connectés au collecteur du premier transistor d'entrée et les collecteurs des deuxièmes transistors des paires étant connectés au collecteur du deuxième transistor d'entrée, et en ce que le collecteur du premier transistor d'entrée constitue la première sortie de l'amplificateur



de conductance de transfert.

4. Amplificateur de conductance de transfert selon la revendication 3, caractérisé en ce que le collecteur du deuxième transistor d'entrée constitue une deuxième sortie de l'amplificateur de conductance de transfert.
5. Amplificateur de conductance de transfert selon la revendication 3 ou 4, caractérisé en ce que pour une valeur ohmique W_N de l'impédance centrale R_N égale à zéro, les deux points de jonction a_N sont combinés de façon à former un seul transistor composé.
6. Amplificateur de conductance de transfert pour convertir une tension d'entrée en un courant de sortie comportant un premier transistor d'entrée (T_{01}) et un deuxième transistor d'entrée (T_{02}), chaque transistor d'entrée présentant une surface d'émetteur e_0 , les bases des premier et deuxième transistors d'entrée constituant les entrées pour la réception de la tension d'entrée et les émetteurs des premier et deuxième transistors d'entrée étant connectés à une source de courant et comportant en outre au moins une entrée de sortie pour le courant de sortie, caractérisé en ce que
 - un montage en série de $2N+1$ impédances ($R_0, \dots, R_{N-1}, R_N, R_{N-1}, \dots, R_0$) est couplé entre les bases des premier (T_{01}) et deuxième (T_{02}) transistors d'entrée, N étant un nombre entier supérieur ou égal à 1; le montage en série étant subdivisé en un premier et un deuxième groupe de N impédances de groupe $R_0, R_1, \dots, R_{N-1}$ présentant des valeurs de résistance respectives $W_0, W_1, \dots, W_{N-1}$ et une impédance centrale R_N présentant une valeur de résistance W_N ; les impédances de groupe de chaque groupe étant interconnectées à $N-1$ points de jonction $a_1, a_2, \dots, a_k, \dots, a_{N-1}, a_k$ étant le point de jonction de l'impédance de groupe R_k et R_{k+1} , k étant un nombre entier allant de $K=1$ à $k=N-1$; l'impédance R_{N-1} de chaque groupe étant connectée à l'impédance centrale R_N à un point de jonction a_N , l'impédance de groupe R_0 des premier et deuxième groupes étant connectée à la base respectivement des premier et deuxième transistors d'entrée,
 - les $N-1$ points de jonction $a_1, \dots, a_{N-1}$ et le point de jonction a_N de chaque groupe sont connectés aux bases de N transistors de groupe respectifs $T_1, T_2, \dots, T_{N-1}, T_N$ présentant des surfaces d'émetteur respectives $e_1, e_2, \dots, e_{N-1}, e_N$; les émetteurs des transistors de groupe étant connectés de façon directe à la source de courant, leurs collecteurs étant connectés à la première sortie de l'amplificateur de conductance de transfert.
7. Amplificateur de conductance de transfert selon la revendication 6, caractérisé en ce que les collecteurs des premier et deuxième transistors d'entrée sont connectés à une deuxième sortie de l'amplificateur de conductance de transfert.
8. Amplificateur de conductance de transfert selon la revendication 6 ou 7, caractérisé en ce que pour une valeur ohmique W_N de l'impédance centrale R_N égale à zéro, les deux points de jonction a_N sont combinés de façon à former un seul point de jonction a_N .
9. Amplificateur de conductance de transfert selon la revendication 2 ou 5, caractérisé en ce que pour $N = 1$, le rapport entre les surfaces d'émetteur est pratiquement égal à $e_1:e_0 = 2:1$.
10. Amplificateur de conductance de transfert selon la revendication 2 ou 5, caractérisé en ce que pour $N=2$, le rapport entre les surfaces d'émetteur est pratiquement égal à $e_2:e_1:e_0 = 32:49:9$ et le rapport entre les valeurs ohmiques est pratiquement égal à $W_1:W_0 = 1.9:1$.
11. Amplificateur de conductance de transfert selon la revendication 2 ou 5, caractérisé en ce que pour $N=3$, le rapport entre les surfaces d'émetteur est pratiquement égal à $e_3:e_2:e_1:e_0 = 5:9:6:1$ et le rapport entre les valeurs ohmiques est pratiquement égal à $W_2:W_1:W_0 = 47:36:17$.
12. Amplificateur de conductance de transfert selon la revendication 1, caractérisé pour $N=1$, le rapport entre les surfaces d'émetteur est pratiquement égal à $e_1:e_0 = 5:1$ et le rapport entre les valeurs ohmiques est pratiquement égal à $W_1:W_0 = 8:5$.
13. Amplificateur de conductance de transfert selon la revendication 1, caractérisé pour $N=2$, le rapport entre les surfaces d'émetteur est pratiquement égal à $e_2:e_1:e_0 = 25:17:3$ et le rapport entre les valeurs



ohmiques est pratiquement égal à $W_2:W_1:W_0=2,4:2:1$.

14. Amplificateur de conductance de transfert selon la revendication 8, caractérisé en ce que pour $N=1$, le rapport entre les surfaces d'émetteur est pratiquement égal à $e_1:e_0=5:1$.

Patentansprüche

1. Steilheitsverstärker zum Umsetzen einer Eingangsspannung in einen Ausgangsstrom, mit einem ersten (T_{01}) und einem zweiten Eingangstransistor (T_{02}), wobei jeder Eingangstransistor eine Emittierfläche e_0 besitzt, die Basen der ersten und zweiten Eingangstransistoren zum Empfangen der Eingangsspannung Eingänge bilden und die Emittier der ersten und zweiten Eingangstransistoren an eine Stromquelle angeschlossen sind, und außerdem mit einem ersten Ausgang für den Ausgangsstrom, dadurch gekennzeichnet, daß
 - eine Reihenschaltung von $2N+1$ Impedanzen ($R_0...R_{N-1}$, R_N , $R_{N-1}...R_0$) zwischen den Basen des ersten (T_{01}) und des zweiten (T_{02}) Eingangstransistors gekoppelt ist, worin N eine ganze Zahl größer als oder gleich 1 ist, wobei die Reihenschaltung in eine erste und in eine zweite Gruppe von N Gruppenimpedanzen R_0 , $R_1...R_{N-1}$ mit jeweils den Widerstandswerten W_0 , $W_1...W_{N-1}$ und eine zentrale Impedanz R_N mit einem Widerstandswert W_N aufgeteilt ist, die Gruppenimpedanzen jeder Gruppe an $N-1$ Verbindungspunkten a_1 , $a_2...a_k...a_{N-1}$ miteinander verbunden sind, worin a_k der Verbindungspunkt der Gruppenimpedanz R_k und R_{k+1} ist, worin k eine ganze Zahl ist, die von $k=1$ bis $k=N-1$ läuft, die Impedanz R_{N-1} jeder Gruppe an einem Verbindungspunkt a_N mit der zentralen Impedanz verbunden ist, die Gruppenimpedanz R_0 der ersten und der zweiten Gruppe mit der Basis des ersten bzw. des zweiten Eingangstransistors verbunden ist,
 - die $N-1$ Verbindungspunkte $a_1...a_{N-1}$ und der Verbindungspunkt a_N jeder Gruppe mit Basen von N jeweiligen Gruppentransistoren T_1 , $T_2...T_{N-1}$, T_N mit jeweiligen Emittierflächen e_1 , $e_2...e_{N-1}$, e_N verbunden sind, wobei die Gruppentransistoren mit ihren Emittiern direkt mit der Stromquelle verbunden sind, und ihre Kollektoren mit einer Energieversorgungsquelle verbunden sind,
 - die Kollektoren der ersten und zweiten Eingangstransistoren den ersten und den zweiten Ausgang des Verstärkers darstellen.
2. Steilheitsverstärker nach Anspruch 1, dadurch gekennzeichnet, daß für einen Widerstandswert W_N der zentralen Impedanz R_N gleich Null die zwei Verbindungspunkte a_N zur Bildung eines einzigen Verbindungspunkts a_N zusammengeschaltet sind.
3. Steilheitsverstärker zum Umsetzen einer Eingangsspannung in einen Ausgangsstrom, mit einem ersten (T_{01}) und einem zweiten Eingangstransistor (T_{02}), wobei jeder Eingangstransistor eine Emittierfläche e_0 besitzt, die Basen der ersten und zweiten Eingangstransistoren zum Empfangen der Eingangsspannung Eingänge bilden und die Emittier der ersten und zweiten Eingangstransistoren an eine Stromquelle angeschlossen sind, und außerdem mit einem ersten Ausgang für den Ausgangsstrom, dadurch gekennzeichnet, daß
 - eine Reihenschaltung von $2N+1$ Impedanzen $R_0...R_{N-1}$, R_N , $R_{N-1}...R_0$) zwischen den Basen des ersten (T_{01}) und des zweiten (T_{02}) Eingangstransistors gekoppelt ist, worin N eine ganze Zahl größer als oder gleich 1 ist, wobei die Reihenschaltung in eine erste und in eine zweite Gruppe von N Gruppenimpedanzen R_0 , $R_1...R_{N-1}$ mit jeweils den Widerstandswerten W_0 , $W_1...W_{N-1}$ und eine zentrale Impedanz R_N mit einem Widerstandswert W_N aufgeteilt ist, die Gruppenimpedanzen jeder Gruppe an $N-1$ Verbindungspunkten a_1 , $a_2...a_k...a_{N-1}$ miteinander verbunden sind, worin a_k der Verbindungspunkt der Gruppenimpedanz R_k und R_{k+1} ist, worin k eine ganze Zahl ist, die von $k=1$ bis $k=N-1$ läuft, die Impedanz R_{N-1} jeder Gruppe an einem Verbindungspunkt a_N mit der zentralen Impedanz verbunden ist, und die Gruppenimpedanz R_0 der ersten und der zweiten Gruppe mit der Basis des ersten bzw. des zweiten Eingangstransistors verbunden ist,
 - die $N-1$ Verbindungspunkte $a_1...a_{N-1}$ und der Verbindungspunkt a_N jeder Gruppe mit Basen von N jeweiligen Gruppentransistorpaaren T_1 , $T_2...T_{N-1}$, T_N verbunden sind, wobei die Gruppentransistorpaare mit ihren Emittiern direkt mit der Stromquelle verbunden sind, jedes der Gruppentransistorpaare zwei parallelgeschaltete Transistoren mit jeweiligen Emittierflächen e_1 , $e_2...e_{N-1}$, e_N enthalten, und die Kollektoren der ersten Transistoren der Paare mit dem Kollektor des ersten Eingangstransistors und die Kollektoren der zweiten Transistoren der Paare mit dem Kollektor des zweiten Eingangstransistors verbunden sind, und daß der Kollektor des ersten Eingangstransistors den



ersten Ausgang des Steilheitsverstärkers bildet.

4. Steilheitsverstärker nach Anspruch 3,
dadurch gekennzeichnet, daß der Kollektor des zweiten Eingangstransistors einen zweiten Ausgang des Steilheitsverstärkers darstellt.
5. Steilheitsverstärker nach Anspruch 3 oder 4,
dadurch gekennzeichnet, daß für einen Widerstandswert W_N der zentralen Impedanz R_N gleich Null die zwei Verbindungspunkte a_N zur Bildung eines Verbundtransistors zusammengeschaltet sind.
6. Steilheitsverstärker zum Umsetzen einer Eingangsspannung in einen Ausgangsstrom, mit einem ersten (T_{01}) und einem zweiten Eingangstransistor (T_{02}), wobei jeder Eingangstransistor eine Emitterfläche e_0 besitzt, die Basen der ersten und zweiten Eingangstransistoren zum Empfangen der Eingangsspannung Eingänge bilden und die Emittoren der ersten und zweiten Eingangstransistoren an eine Stromquelle angeschlossen sind, und außerdem mit einem ersten Ausgang für den Ausgangsstrom, dadurch gekennzeichnet, daß
 - eine Reihenschaltung von $2N+1$ Impedanzen ($R_0 \dots R_{N-1}$, R_N , $R_{N+1} \dots R_0$) zwischen den Basen des ersten (T_{01}) und des zweiten (T_{02}) Eingangstransistors gekoppelt ist, worin N eine ganze Zahl größer als oder gleich 1 ist, wobei die Reihenschaltung in eine erste und in eine zweite Gruppe von N Gruppenimpedanzen $R_0, R_1 \dots R_{N-1}$ mit jeweils den Widerstandswerten $W_0, W_1 \dots W_{N-1}$ und eine zentrale Impedanz R_N mit einem Widerstandswert W_N aufgeteilt ist, die Gruppenimpedanzen jeder Gruppe an $N-1$ Verbindungspunkten $a_1, a_2 \dots a_{N-1}$ miteinander verbunden sind, worin a_k der Verbindungspunkt der Gruppenimpedanz R_k und R_{k+1} ist, worin k eine ganze Zahl ist, die von $k=1$ bis $k=N-1$ läuft, die Impedanz R_{N-1} jeder Gruppe an einem Verbindungspunkt a_N mit der zentralen Impedanz R_N verbunden ist, die Gruppenimpedanz R_0 der ersten und der zweiten Gruppe mit der Basis des ersten bzw. des zweiten Eingangstransistors verbunden ist,
 - die $N-1$ Verbindungspunkte $a_1 \dots a_{N-1}$ und der Verbindungspunkt a_N jeder Gruppe mit Basen von N jeweiligen Gruppentransistoren $T_1, T_2 \dots T_{N-1}, T_N$ mit jeweiligen Emitterflächen $e_1, e_2 \dots e_{N-1}, e_N$ verbunden sind, wobei die Gruppentransistoren mit ihren Emittoren direkt mit der Stromquelle verbunden sind, und ihre Kollektoren mit dem ersten Ausgang des Steilheitsverstärkers verbunden sind.
7. Steilheitsverstärker nach Anspruch 6,
dadurch gekennzeichnet, daß die Kollektoren der ersten und zweiten Eingangstransistoren mit einem zweiten Ausgang des Steilheitsverstärkers verbunden sind.
8. Steilheitsverstärker nach Anspruch 6 oder 7,
dadurch gekennzeichnet, daß für einen Widerstandswert W_N der zentralen Impedanz R_N gleich Null die zwei Verbindungspunkte a_N zur Bildung eines einzigen Verbindungspunkts a_N zusammengeschaltet sind.
9. Steilheitsverstärker nach Anspruch 2 oder 5,
dadurch gekennzeichnet, daß für $N=1$ das Verhältnis zwischen den Emitterflächen im wesentlichen gleich $e_1:e_0 = 2:1$ beträgt.
10. Steilheitsverstärker nach Anspruch 2 oder 5,
dadurch gekennzeichnet, daß für $N=2$ das Verhältnis zwischen den Emitterflächen im wesentlichen gleich $e_2:e_1:e_0 = 32:49:91$ und das Verhältnis zwischen den Widerstandswerten im wesentlichen gleich $W_1:W_0 = 8:5$ beträgt.
11. Steilheitsverstärker nach Anspruch 2 oder 5,
dadurch gekennzeichnet, daß für $N=3$ das Verhältnis zwischen den Emitterflächen im wesentlichen gleich $e_3:e_2:e_1:e_0 = 5:9:6:1$ und das Verhältnis zwischen den Widerstandswerten im wesentlichen gleich $W_2:W_1:W_0 = 47:36:17$ beträgt.
12. Steilheitsverstärker nach Anspruch 1,
dadurch gekennzeichnet, daß für $N=1$ das Verhältnis zwischen den Emitterflächen im wesentlichen gleich $e_1:e_0 = 5:1$ und das Verhältnis zwischen den Widerstandswerten im wesentlichen gleich $W_1:W_0$



= 8:5 beträgt.

13. Steilheitsverstärker nach Anspruch 1,

dadurch gekennzeichnet, daß für $N=2$ das Verhältnis zwischen den Emitterflächen im wesentlichen
gleich $a_2:a_1:a_0 = 25:17:3$ und das Verhältnis zwischen den Widerstandswerten im wesentlichen gleich
 $W_2:W_1:W_0 = 2.4:2:1$ beträgt.

14. Steilheitsverstärker nach Anspruch 8,

dadurch gekennzeichnet, daß für $N=1$ das Verhältnis zwischen den Emitterflächen im wesentlichen
gleich $a_1:a_0 = 5:1$ beträgt.