ABSTRACT

A semiconductor device, including a fin active region; a device isolation layer covering two sidewalls of the fin active region on the substrate; a gate structure; a nano-sheet structure including a plurality of nano-sheets; and source/drain regions disposed on the fin active region and adjacent to the gate structure, wherein each source/drain region of the source/drain regions includes a buffer layer, an inner impurity layer, and a central impurity layer which are sequentially stacked, wherein the buffer layer fills a first indentation between two vertically-adjacent nano-sheets and a second indentation between the top surface of the fin active region and a nano-sheet, and wherein the plurality of nano-sheets contact side surfaces of the inner impurity layer.

FIG. 2A