

CLAIMS

We claim:

1. A gated nanosheet diode comprising:

a substrate;

a first source/drain (S/D) disposed on the substrate, the first S/D having a first S/D doping concentration with a first S/D doping type;

a second source/drain (S/D) disposed on the substrate, the second S/D having a second S/D doping concentration with a second S/D doping type;

a p-n junction forming a diode;

a first side of the p-n junction, the first side having a first side junction doping concentration with a first side junction doping type, the first side junction doping type being the same as the first S/D doping type and the first side of the p-n junction electrically and physically connected to the first S/D;

a second side of the p-n junction, the second side having a second side junction doping concentration with a second side junction doping type, the second side junction doping type being the same as the second S/D doping type and the second side of the p-n junction electrically and physically connected to the second S/D;

a gate dielectric layer interfacing and surrounding the p-n junction; and

a gate metal surrounding the gate dielectric layer, the gate metal and the gate dielectric layer forming a gate stack surrounding the p-n junction.

2. A gated nanosheet diode, as in Claim 1, where the first side junction doping type and the first S/D doping type are n-type doped.

3. A gated nanosheet diode, as in Claim 2, where the n-type dopants are one of the following: phosphorus (P), arsenic (As), and antimony (Sb).
4. A gated nanosheet diode, as in Claim 2, where a first side junction doping concentration is between $1 \times 10^{19} \text{ cm}^{-3}$ and $4 \times 10^{20} \text{ cm}^{-3}$ and the first S/D doping concentration is between $8 \times 10^{20} \text{ cm}^{-3}$ and $2 \times 10^{21} \text{ cm}^{-3}$.
5. A gated nanosheet diode, as in Claim 1, where the second side junction doping type and the second S/D doping type are p-type dopants.
6. A gated nanosheet diode, as in Claim 5, where the p-type dopants are one of the following: boron (B), gallium (Ga), indium (In), and thallium (Tl).
7. A gated nanosheet diode, as in Claim 2, where a second side junction doping concentration is between $1 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ and the second S/D doping concentration is between $8 \times 10^{20} \text{ cm}^{-3}$ and $2 \times 10^{21} \text{ cm}^{-3}$.
8. A gated nanosheet diode, as in Claim 1, where the first side junction doping type and the first S/D doping type are p-type doped.
9. A gated nanosheet diode, as in Claim 8, where a first side junction doping concentration is between $1 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ and the first S/D doping concentration is between $8 \times 10^{20} \text{ cm}^{-3}$ and $2 \times 10^{21} \text{ cm}^{-3}$.

10. A gated nanosheet diode, as in Claim 1, where the second side junction doping type and the second S/D doping type are n-type dopants.

11. A gated nanosheet diode, as in Claim 10, where a second side junction doping concentration is between $1 \times 10^{19} \text{ cm}^{-3}$ and $4 \times 10^{20} \text{ cm}^{-3}$ and the second S/D doping concentration is between $8 \times 10^{20} \text{ cm}^{-3}$ and $2 \times 10^{21} \text{ cm}^{-3}$.

12. A gated nanosheet diode comprising:

a substrate;

a first source/drain (S/D) disposed on the substrate, the first S/D having a first S/D doping concentration with a first S/D doping type;

two or more second source/drain (S/Ds) disposed on the substrate, the second S/Ds having a second S/D doping concentration with a second S/D doping type, one of the second S/Ds being a right second S/D and one of the second S/Ds being a left second S/D;

one or more p-n junctions, each p-n junction forming a diode in a separate channel, each of the diodes and the channels being surrounded by a gate stack, the gate stack having a gate dielectric layer interfacing and surrounding each of the p-n junctions and a gate metal surrounding the gate dielectric layer;

two or more device stacks formed by one or more of the diodes stacked upon one another, a left device stack being between the left second S/D and the first S/D and the right second right device stack being between the right second S/D and the first S/D;

a first side of each of the p-n junctions, the first side having a first side junction doping concentration with a first side junction doping type, the first side junction doping type being the

same as the first S/D doping type and the first sides of the p-n junctions electrically and physically connected to the first S/D;

a second side of the p-n junction, the second side having a second side junction doping concentration with a second side junction doping type, the second side junction doping type being the same as the second S/D doping type and the second side of the p-n junctions in the left stack electrically and physically connected to the left second S/D and the p-n junctions in the right stack electrically and physically connected to the right second S/D,

where the first sides of the p-n junctions in the left and right stack being electrically connected to the first S/D forms a plurality of the diodes electrically connected in parallel.

13. A gated nanosheet diode, as in Claim 12, where the gate metal surrounding the gate dielectric layer and each of the diodes is electrically connected in common.

14. A gated nanosheet diode, as in Claim 12, where a current capacity of the gated diode increases with the number of diodes.

15. A method of making a gated nanosheet diode comprising the steps of:

forming an interim layered structure from a plurality of nanolayers, the nanolayers being one or more channel layers and one or more dummy gate layers, the channel layers and dummy gate layers disposed, alternating, one on the other, to form the interim layered structure, the channel layers being a semiconductor material with a second side junction doping concentration and a second side junction doping type;

depositing two dummy gates each covered by a gate spacer layer on the interim layered structure;

using the gate spacer layers as a mask, creating a pair of stacks from the interim layered structure by removing the nanolayers between and beside the stacks;

forming an inner spacer on each of one or more exposed ends of the dummy gate layers;

removing part of each of the channel layers to expose a channel layer end of each channel layer within a channel, the channel layer now being a second side junction;

epitaxially growing a channel epitaxy as a first part of a first S/D epitaxial growth, the channel epitaxy growing a first side junction within the channel and creating a p-n junction/diode at the exposed channel layer where the first side junction contacts the second side junction, the first side junction having a first side junction doping concentration and a first side junction doping type opposite of the second side junction doping type;

continuing the first S/D epitaxial growth to grow a first S/D with a first S/D doping concentration and a first S/D doping type, the first side junction doping type and the first S/D doping type being the same and the first S/D doping concentration being higher than the first side junction doping concentration;

epitaxially growing a second source/drain (S/D) with a second S/D doping concentration and a second S/D doping type, the second S/D in electrical contact with the second side junctions, the second S/D doping type being the same as the second side junction doping type and the second S/D doping concentration being higher than the second side junction doping concentration; and

forming a gate stack around one or more of the p-n junction/diodes.

16. A method, as in Claim 15, where the first side junction doping concentration is increased to the first S/D doping concentration after the p-n junction/diodes are formed.

17. A method, as in Claim 16, where the channel epitaxy is a timed epitaxial growth.

18. A method, as in Claim 15, where the part of each of the channel layers removed exposes the channel layer end at about one half a width of the channel layer.

19. A method, as in Claim 15, where the first S/D doping concentration and the second S/D doping concentration are between $8 \times 10^{20} \text{ cm}^{-3}$ and $2 \times 10^{21} \text{ cm}^{-3}$.

20. A method, as in Claim 15, where the gate stack has a gate dielectric layer interfacing and surrounding each of the p-n junctions and a gate metal surrounding the gate dielectric layer and the gate metal is one or more of the following: titanium nitride (TiN), tantalum nitride (Ta₂N₅) or ruthenium (Ru), titanium aluminum nitride (TiAlN), titanium aluminum carbon nitride (TiAlCN), titanium carbide (TiC), titanium aluminum carbide (TiAlC), tantalum aluminum carbide (TaAlC), tantalum aluminum carbon nitride (TaAlCN) or lanthanum (La) doped TiN, TaN.