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ABSTRACT

A NOVEL METHOD OF FABRICATING METALLIC LOCAL INTERCONNECTIONS THAT ALSO IMPROVES TRANSISTOR PERFORMANCE

A method for making low sheet resistance local metal interconnections and improved transistor performance is described. The method involves patterning a polysilicon layer and a silicon nitride (Si_3N_4) cap layer over device areas to form FET gate electrodes, and the patterned polysilicon extends over the field oxide regions to form portions of the local interconnections. After forming source/drain areas and sidewall spacers on the FET gate electrodes, a silicon oxide (SiO_2) insulating layer is deposited and polished back to the Si_3N_4 cap. The Si_3N_4 is then selectively removed over the patterned polysilicon layer, leaving recesses in the SiO_2 layer. After etching contact openings in the SiO_2 layer to the substrate, a high electrically conducting metal layer, having a barrier layer, is deposited and patterned to complete the local interconnections. Portions of the metal are retained in the recesses over the pattered polysilicon layer to improve transistor performance, while portions of the metal in the contact openings provide low-contact resistance to the substrate.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)



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