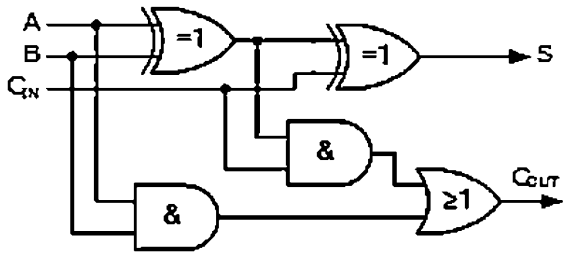


Truth Table			
B	A	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(PRIOR ART)

Figure 1



Truth Table				
C-in	B	A	Sum	C-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(PRIOR ART)

Figure 2

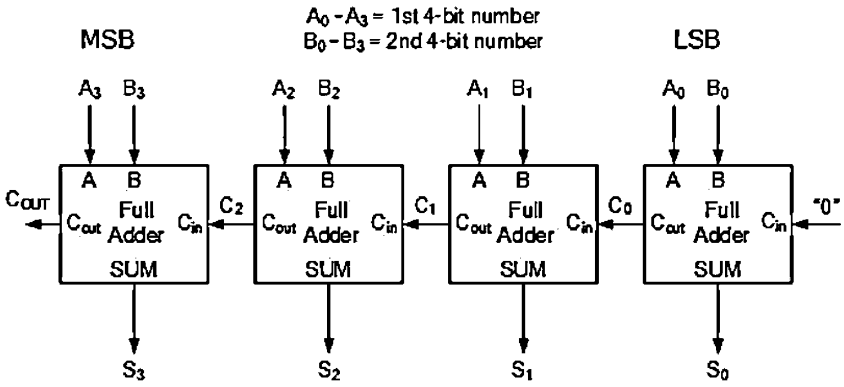


Figure 3 (PRIOR ART)

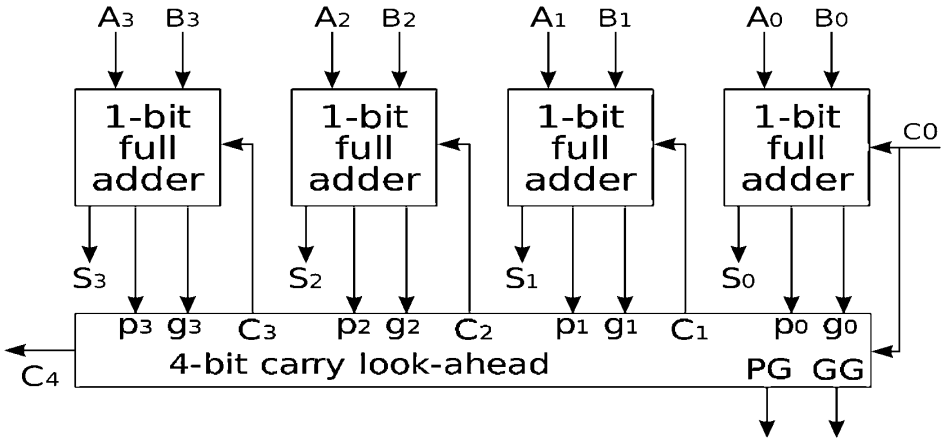


Figure 4 (PRIOR ART)

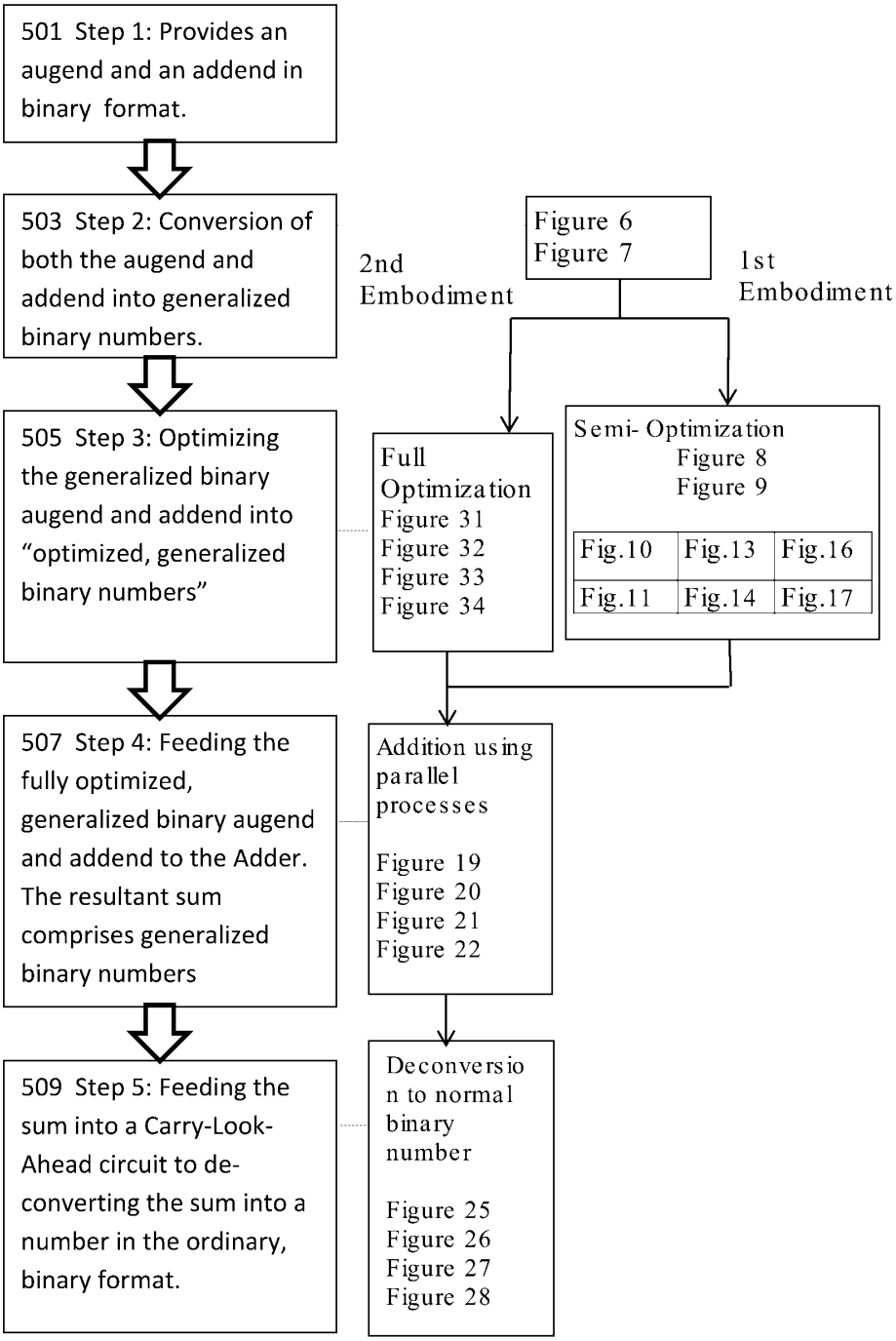

501 Step 1: Provides an augend and an addend in binary format.
503 Step 2: Conversion of both the augend and addend into generalized binary numbers.
505 Step 3: Optimizing the generalized binary augend and addend into "optimized, generalized binary numbers"
507 Step 4: Feeding the fully optimized, generalized binary augend and addend to the Adder. The resultant sum comprises generalized binary numbers
509 Step 5: Feeding the sum into a Carry-Look-Ahead circuit to de-converting the sum into a number in the ordinary, binary format.
Figure 6
Figure 7
2nd Embodiment
1st Embodiment
Full Optimization
Figure 31
Figure 32
Figure 33
Figure 34
Semi- Optimization
Figure 8
Figure 9
Fig.10
Fig.13
Fig.16
Fig.11
Fig.14
Fig.17
Addition using parallel processes
Figure 19
Figure 20
Figure 21
Figure 22
Deconversio n to normal binary number
Figure 25
Figure 26
Figure 27
Figure 28

Figure 5

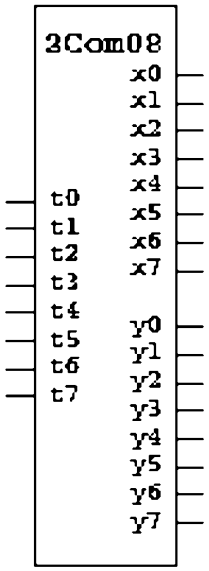

2Com08
x0
x1
x2
x3
x4
x5
x6
x7
t0
t1
t2
t3
t4
t5
t6
t7
y0
y1
y2
y3
y4
y5
y6
y7

Figure 6

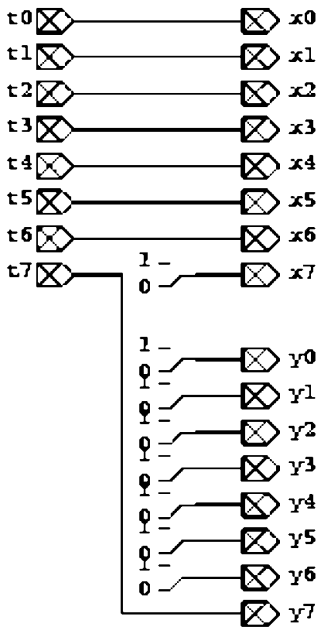


Figure 7a

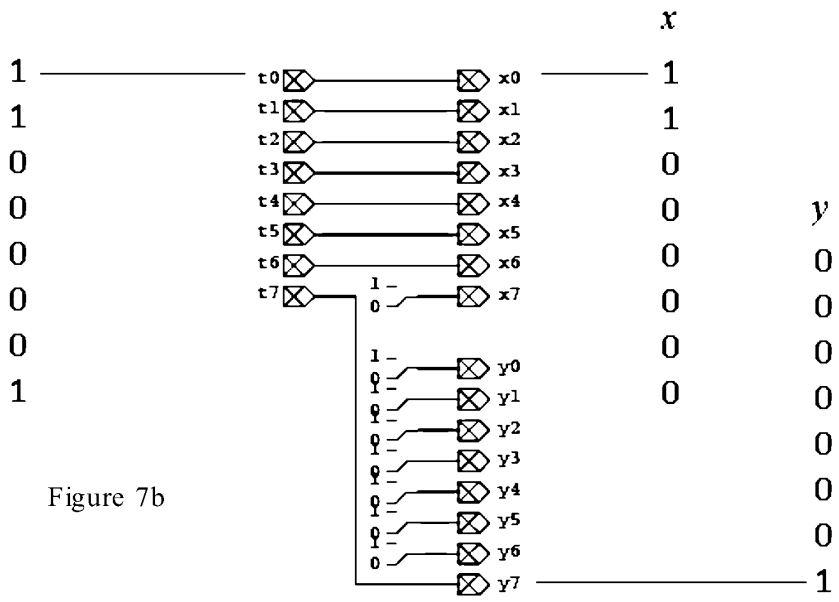


Figure 7b

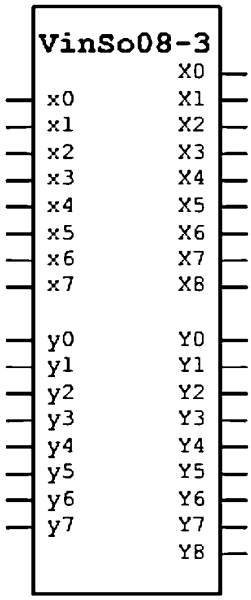


Figure 8

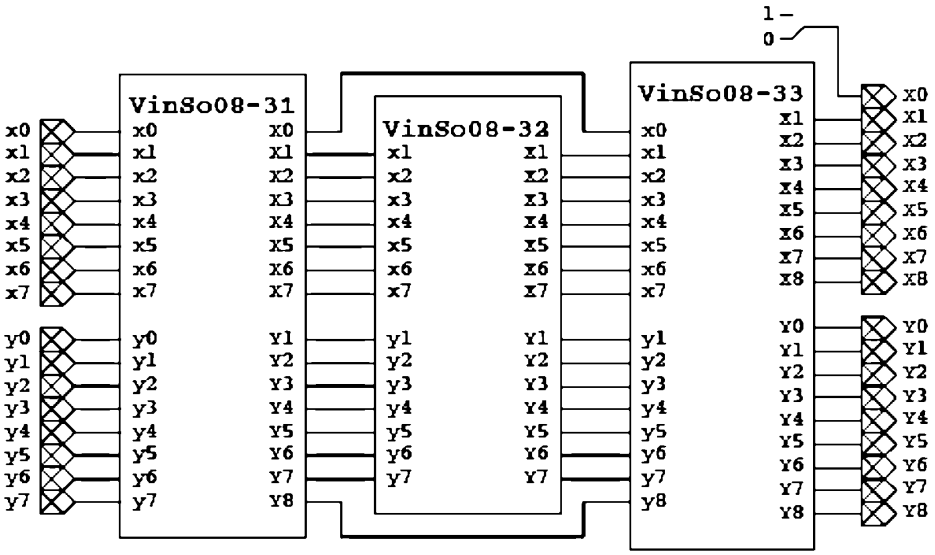


Figure 9

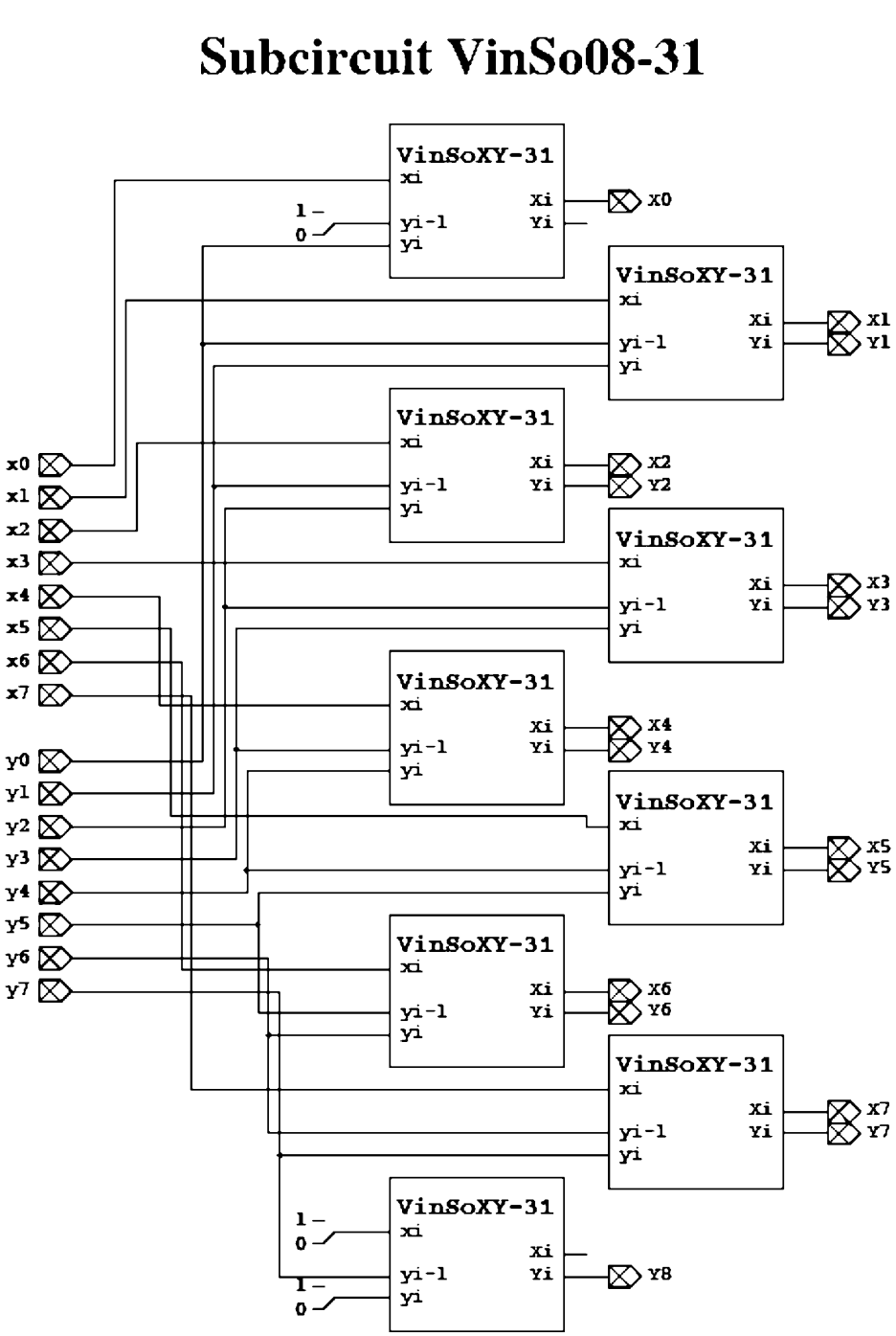

Subcircuit VinSo08-31
VinSoXY-31
xi
yi-1
yi
Xi
Yi
1
0
x0
x1
x2
x3
x4
x5
x6
x7
y0
y1
y2
y3
y4
y5
y6
y7
X0
X1
Y1
X2
Y2
X3
Y3
X4
Y4
X5
Y5
X6
Y6
X7
Y7
Y8

Figure 10

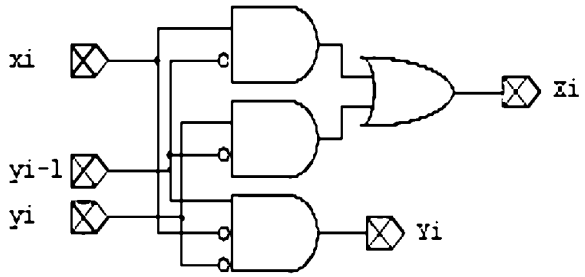
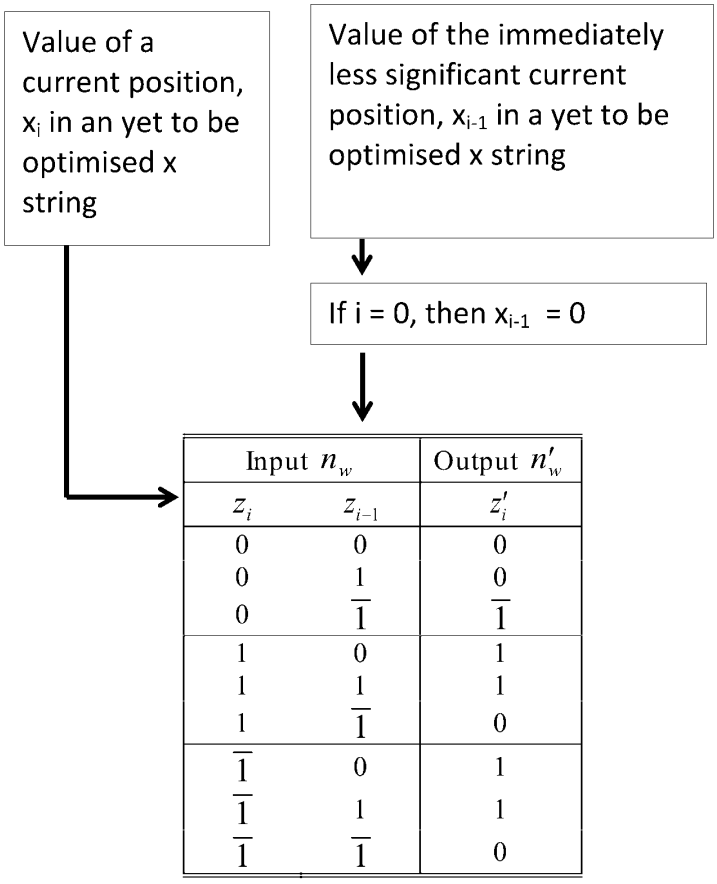


Figure 11



Input n_w		Output n'_w
z_i	z_{i-1}	z'_i
0	0	0
0	1	0
0	$\overline{1}$	$\overline{1}$
1	0	1
1	1	1
1	$\overline{1}$	0
$\overline{1}$	0	1
$\overline{1}$	1	1
$\overline{1}$	$\overline{1}$	0

Table 1: Eliminating strings of $\overline{1}$.

Figure 12

Subcircuit VinSo08-32

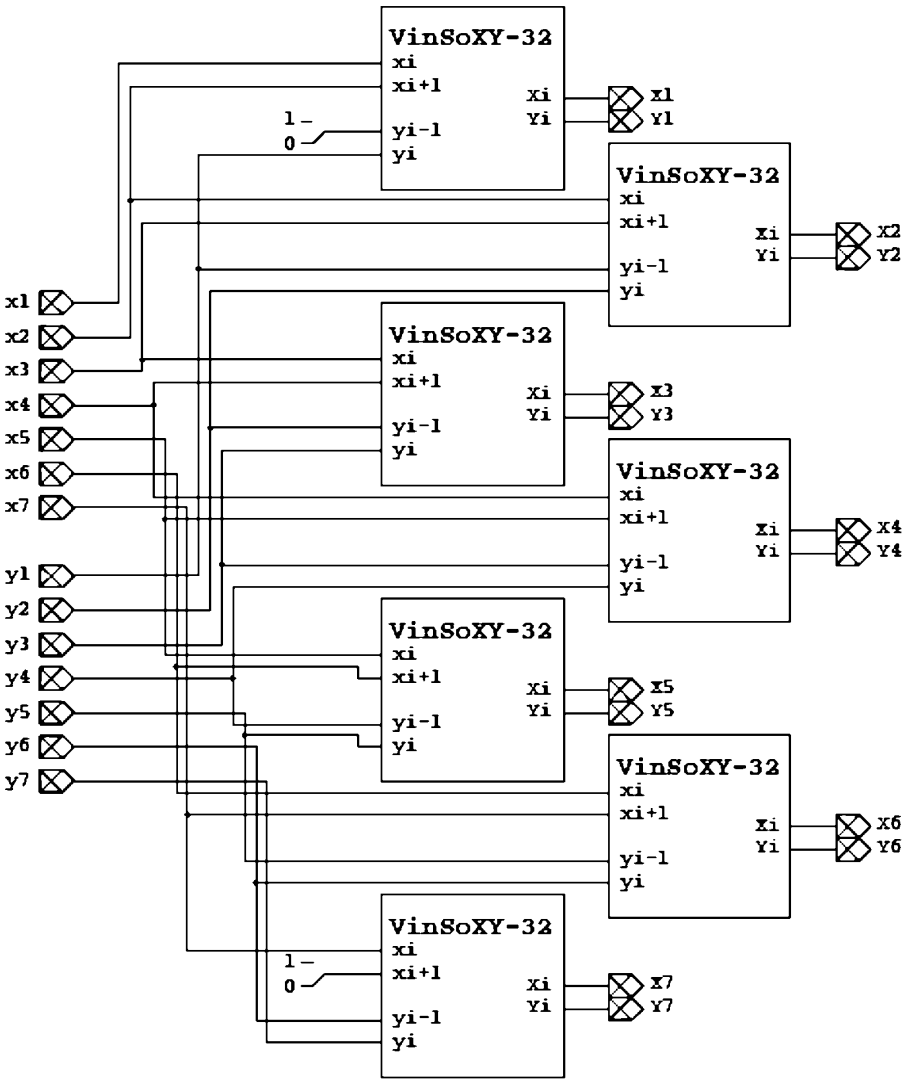


Figure 13

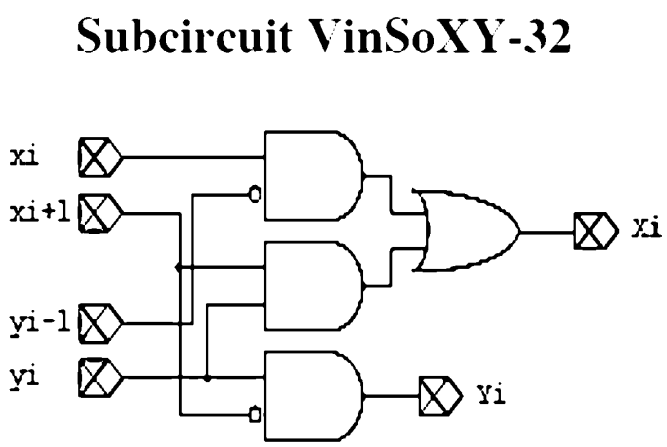


Figure 14

n'_w			n''_w	n'_w			n''_w	n'_w			n''_w
z'_{i+1}	z'_i	z'_{i-1}	z''_i	z'_{i+1}	z'_i	z'_{i-1}	z''_i	z'_{i+1}	z'_i	z'_{i-1}	z''_i
0	0	0	0	1	0	0	0	$\overline{1}$	0	0	0
0	0	1	0	1	0	1	0	$\overline{1}$	0	1	0
0	0	$\overline{1}$	0	1	0	$\overline{1}$	0	$\overline{1}$	0	$\overline{1}$	0
0	1	0	1	1	1	0	1	$\overline{1}$	1	0	1
0	1	1	1	1	1	1	1	$\overline{1}$	1	1	1
0	1	$\overline{1}$	0	1	1	$\overline{1}$	0	$\overline{1}$	1	$\overline{1}$	0
0	$\overline{1}$	0	$\overline{1}$	1	$\overline{1}$	0	1	$\overline{1}$	$\overline{1}$	0	*
0	$\overline{1}$	1	$\overline{1}$	1	$\overline{1}$	1	1	$\overline{1}$	$\overline{1}$	1	*
0	$\overline{1}$	$\overline{1}$	*	1	$\overline{1}$	$\overline{1}$	*	$\overline{1}$	$\overline{1}$	$\overline{1}$	*

Note: * indicates impossible inputs as strings of $\overline{1}$ have been eliminated

Table 2

Figure 15

Subcircuit VinSo08-33

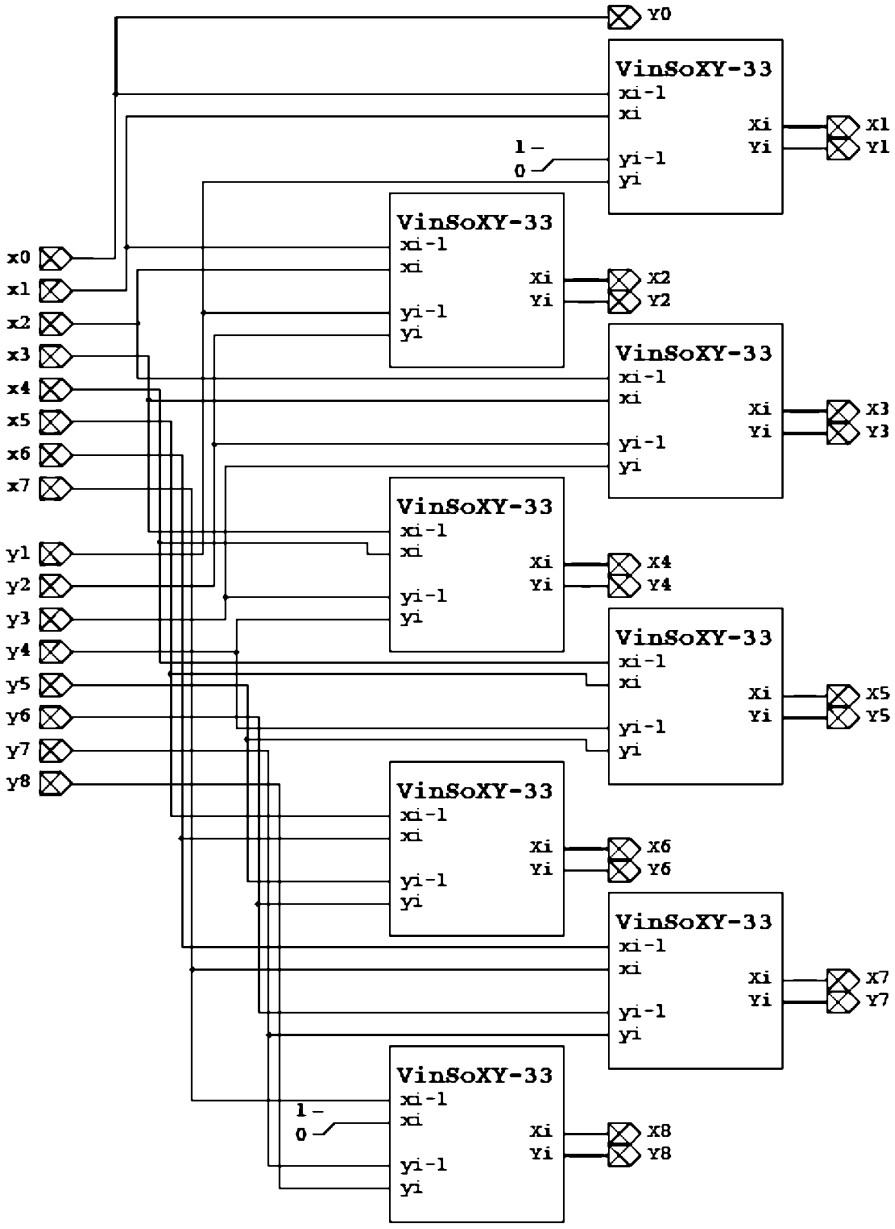


Figure 16

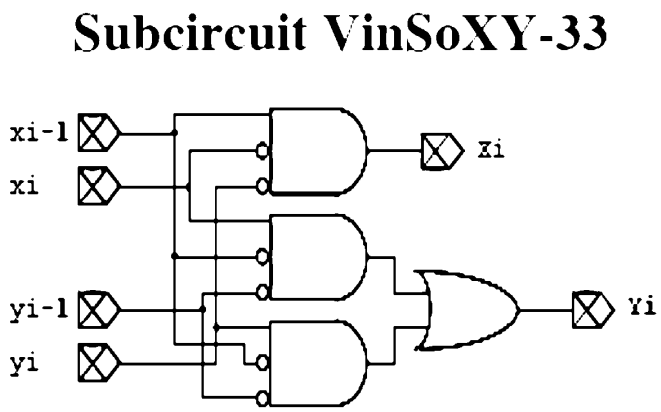


Figure 17

Input n''_w		Output $\widetilde{N}_w$
z''_i	z''_{i-1}	$\widetilde{Z}_i$
0	0	0
0	1	1
0	$\overline{1}$	0
1	0	$\overline{1}$
1	1	0
1	$\overline{1}$	*
$\overline{1}$	0	$\overline{1}$
$\overline{1}$	1	0
$\overline{1}$	$\overline{1}$	*

Note: * indicates impossible inputs as strings of $1\overline{1}$ and $\overline{1}1$ have been eliminated.

Table 3

Figure 18

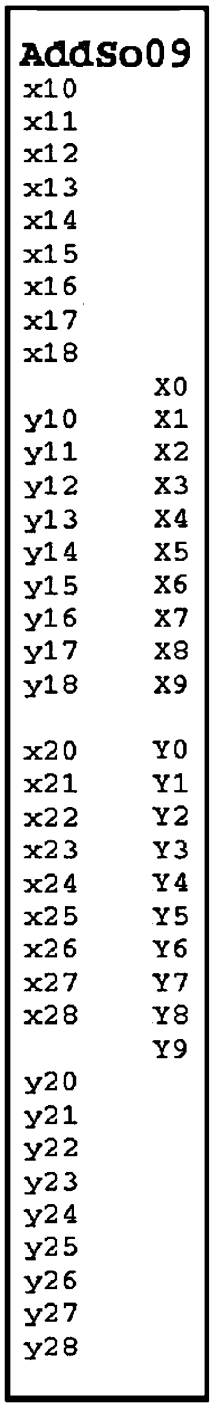

AddSo09
x10
x11
x12
x13
x14
x15
x16
x17
x18
X0
y10 X1
y11 X2
y12 X3
y13 X4
y14 X5
y15 X6
y16 X7
y17 X8
y18 X9
x20 Y0
x21 Y1
x22 Y2
x23 Y3
x24 Y4
x25 Y5
x26 Y6
x27 Y7
x28 Y8
Y9
y20
y21
y22
y23
y24
y25
y26
y27
y28

Figure 19

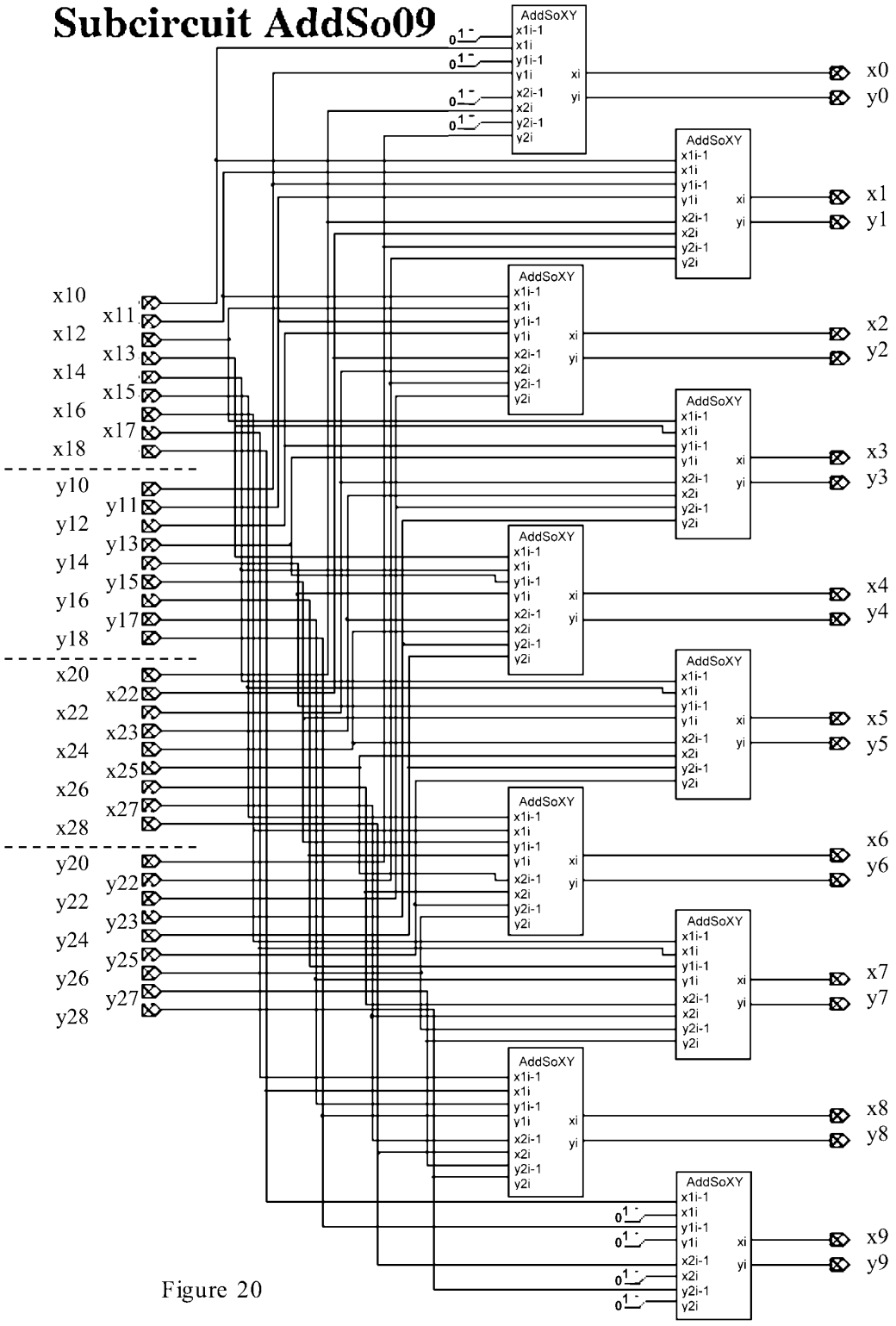

Subcircuit AddSo09
AddSoXY
x1i-1
x1i
y1i-1
y1i
x2i-1
x2i
y2i-1
y2i
xi
yi
x10
x11
x12
x13
x14
x15
x16
x17
x18
y10
y11
y12
y13
y14
y15
y16
y17
y18
x20
x22
x22
x23
x24
x25
x26
x27
x28
y20
y22
y22
y23
y24
y25
y26
y27
y28
x0
y0
x1
y1
x2
y2
x3
y3
x4
y4
x5
y5
x6
y6
x7
y7
x8
y8
x9
y9

Figure 20

Subcircuit AddSoXY

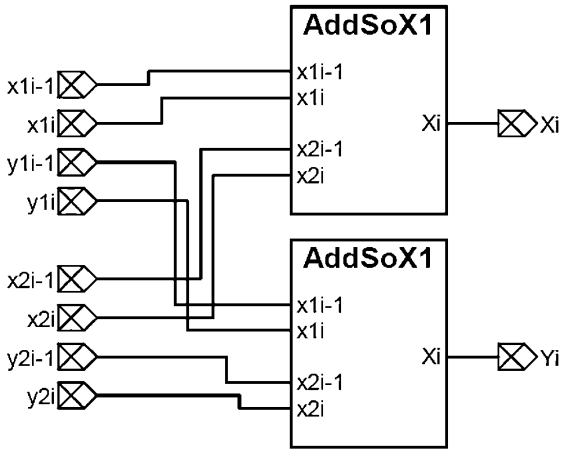


Figure 21

Subcircuit AddSoX1

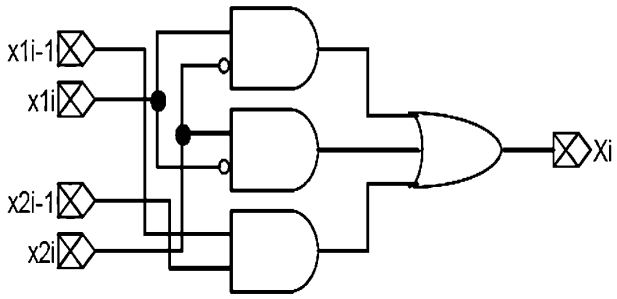


Figure 22

Table 12: Separate addition of positive and negative components.

Input*				Output	Input*				Output
$(x_i)_1$	$(x_{i-1})_1$	$(x_i)_2$	$(x_{i-1})_2$	x_i'	$(y_i)_1$	$(y_{i-1})_1$	$(y_i)_2$	$(y_{i-1})_2$	y_i'
0	0	0	0	0	0	0	0	0	0
		0	1	0			0	$\overline{1}$	0
		1	0	1			$\overline{1}$	0	$\overline{1}$
0	1	0	0	0	0	$\overline{1}$	0	0	0
		0	1	1			0	$\overline{1}$	$\overline{1}$
		1	0	1			$\overline{1}$	0	$\overline{1}$
1	0	0	0	1	$\overline{1}$	0	0	0	$\overline{1}$
		0	1	1			0	$\overline{1}$	$\overline{1}$
		1	0	0			$\overline{1}$	0	0

*Inputs for 11 and $\overline{1}\overline{1}$ are impossible because these are semi-optimized binary numbers.

Figure 23

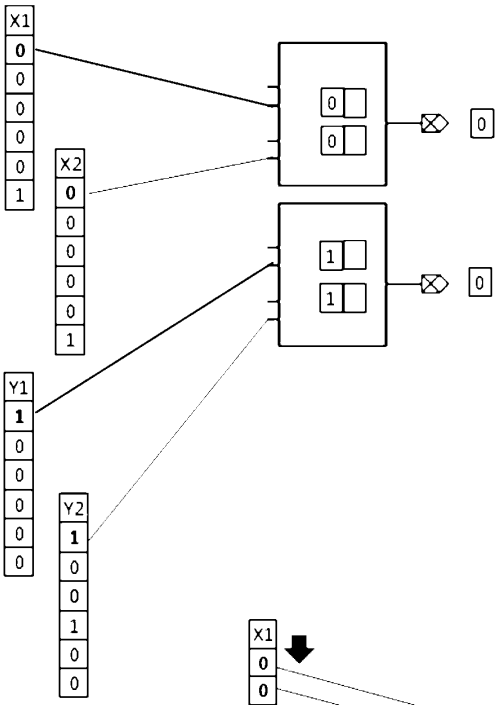


Figure 24a

Figure 24b

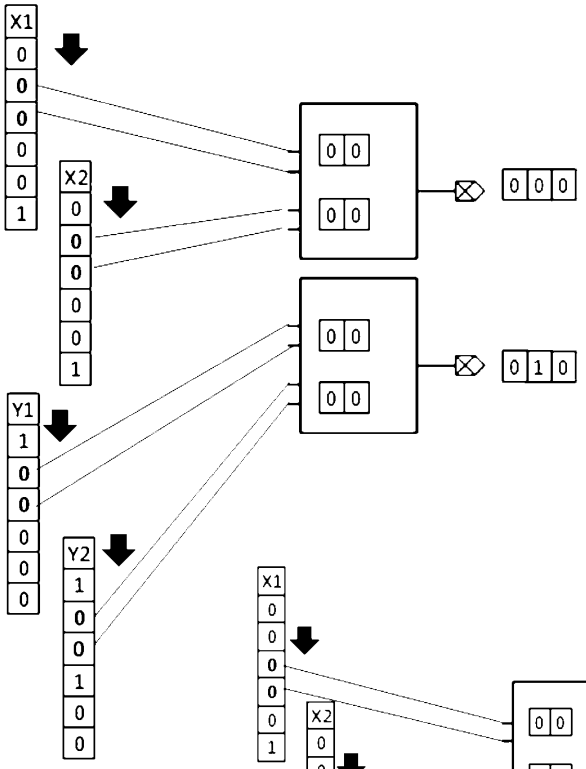


Figure 24c

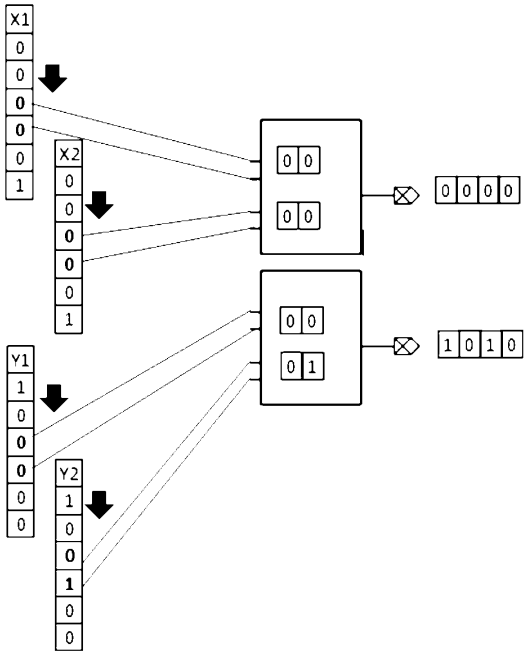


Figure 24d

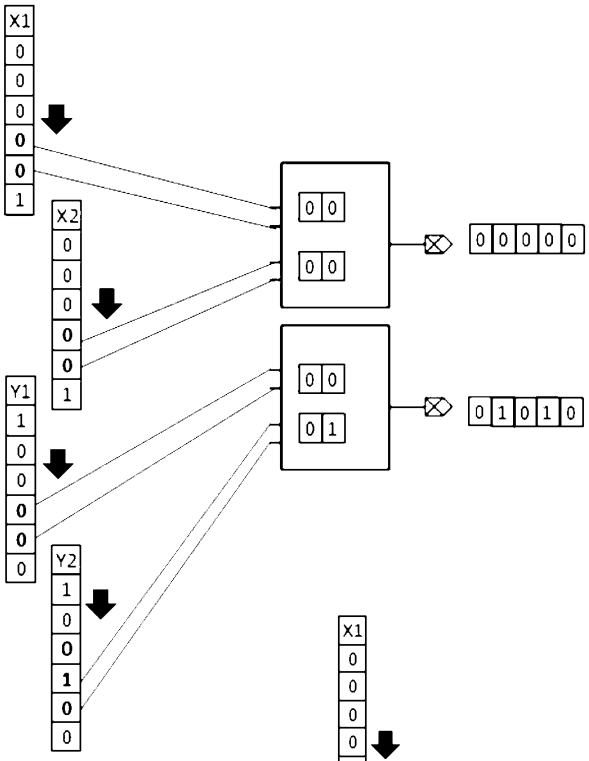
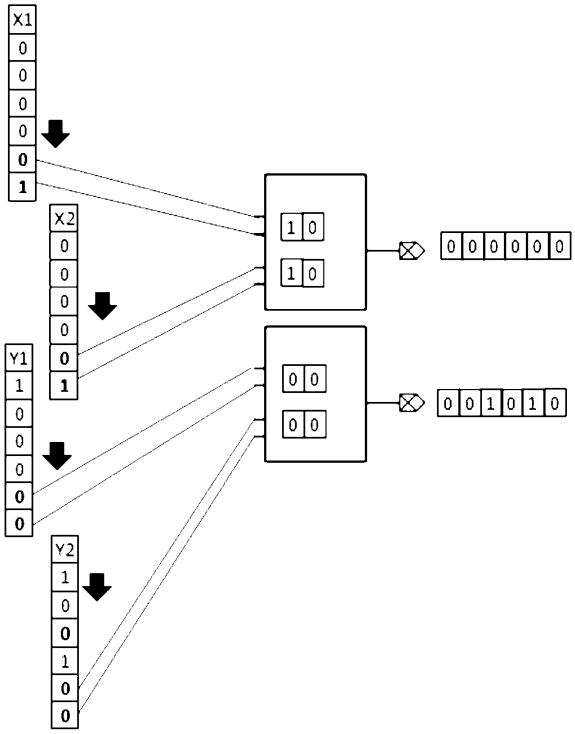


Figure 24e

Figure 24f



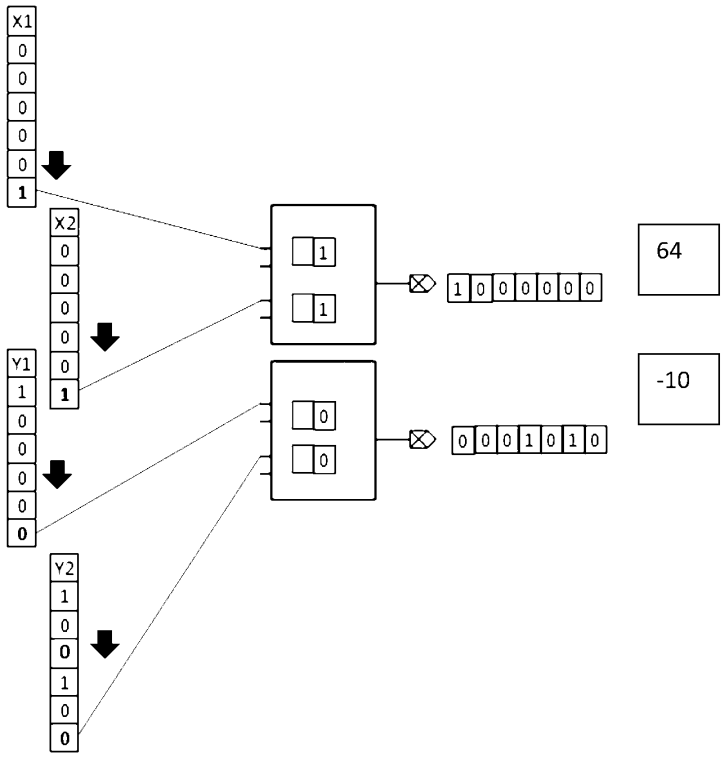

X1
0
0
0
0
0
1
X2
0
0
0
0
0
1
Y1
1
0
0
0
0
0
Y2
1
0
0
0
1
0
0
1
1
0
0
1
0
0
0
0
0
0
1
0
0
0
1
0
1
0
64
-10

Figure 24g

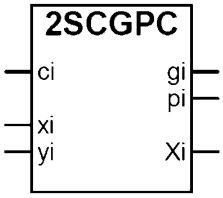


Figure 25

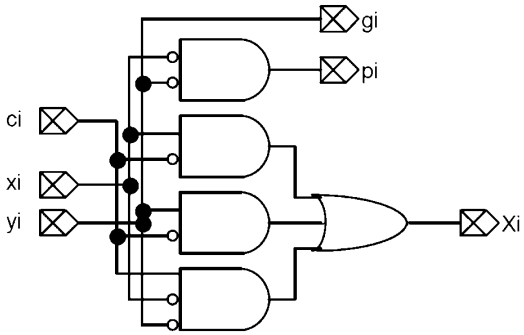


Figure 26

Input z_i	Generate g_i	Propagate p_i
0 ($x_i = y_i = 0$ only)	0	1
1	0	0
$\overline{1}$	1	0

Table 4

Figure 27

"carry" c_i	General binary number z_i	2's complement number X_i
0	0	0
0	1	1
0	$\overline{1}$	1
1	0	1
1	1	0
1	$\overline{1}$	0

Table 5a: "Final stage summation" logic $i = 0,1,2,\cdots,(n-1)$.

Figure 28

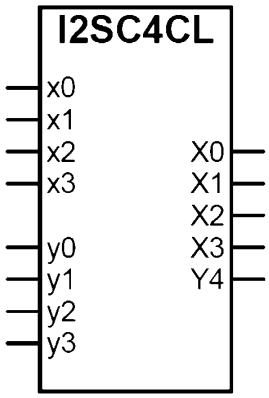


Figure 29a

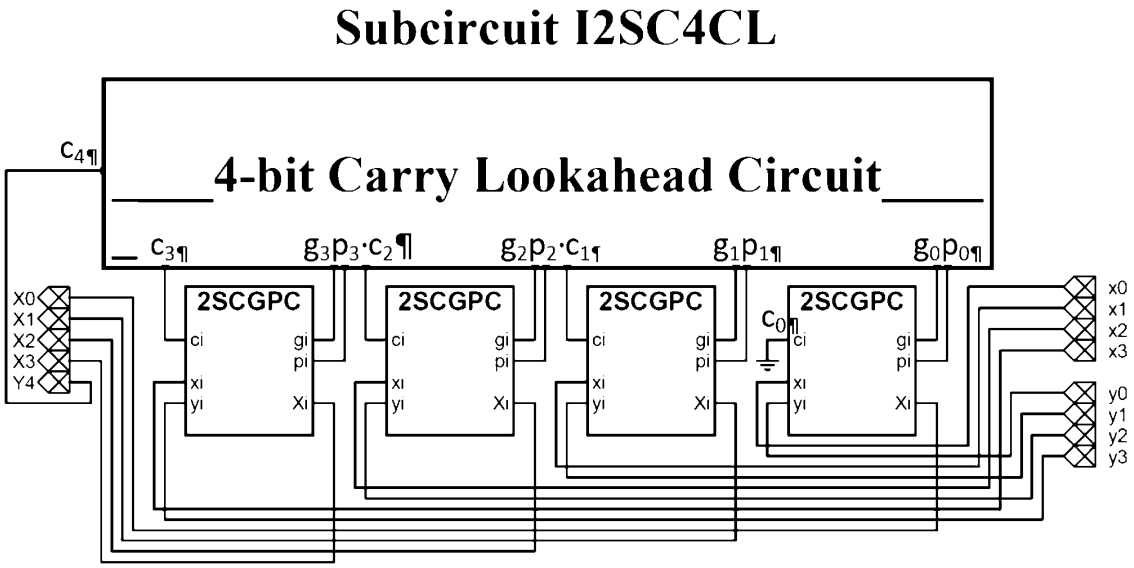


Figure 29b

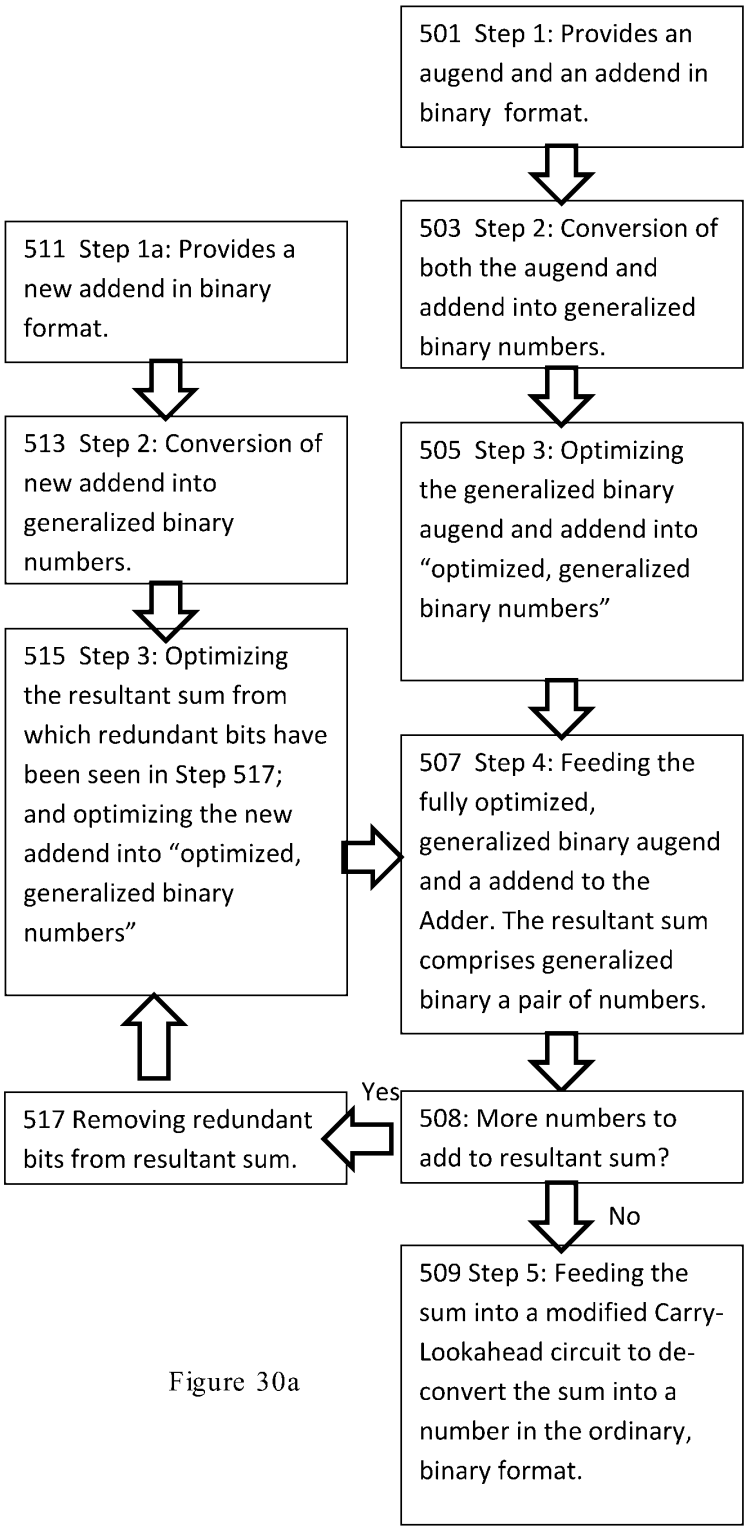

501 Step 1: Provides an augend and an addend in binary format.
503 Step 2: Conversion of both the augend and addend into generalized binary numbers.
505 Step 3: Optimizing the generalized binary augend and addend into "optimized, generalized binary numbers"
507 Step 4: Feeding the fully optimized, generalized binary augend and a addend to the Adder. The resultant sum comprises generalized binary a pair of numbers.
508: More numbers to add to resultant sum?
Yes
No
509 Step 5: Feeding the sum into a modified Carry-Lookahead circuit to de-convert the sum into a number in the ordinary, binary format.
517 Removing redundant bits from resultant sum.
515 Step 3: Optimizing the resultant sum from which redundant bits have been seen in Step 517; and optimizing the new addend into "optimized, generalized binary numbers"
513 Step 2: Conversion of new addend into generalized binary numbers.
511 Step 1a: Provides a new addend in binary format.

Figure 30a

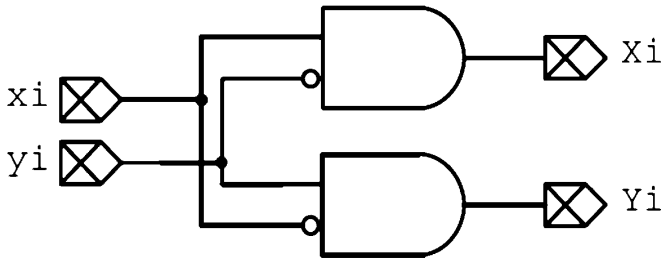


Figure 30b

Input $\hat{z}_j$	Output z'_j
0^*	0
1	1
$\overline{1}$	$\overline{1}$

0^* implies $\hat{x}_j = \hat{y}_j = 0$ or $\hat{x}_j = \hat{y}_j = 1$

Table 5b

Figure 30c

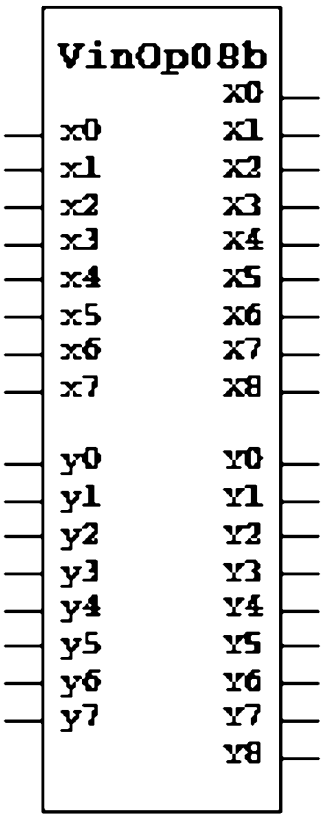

VinOp08b
x0
x1
x2
x3
x4
x5
x6
x7
y0
y1
y2
y3
y4
y5
y6
y7
X0
X1
X2
X3
X4
X5
X6
X7
X8
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8

Figure 31

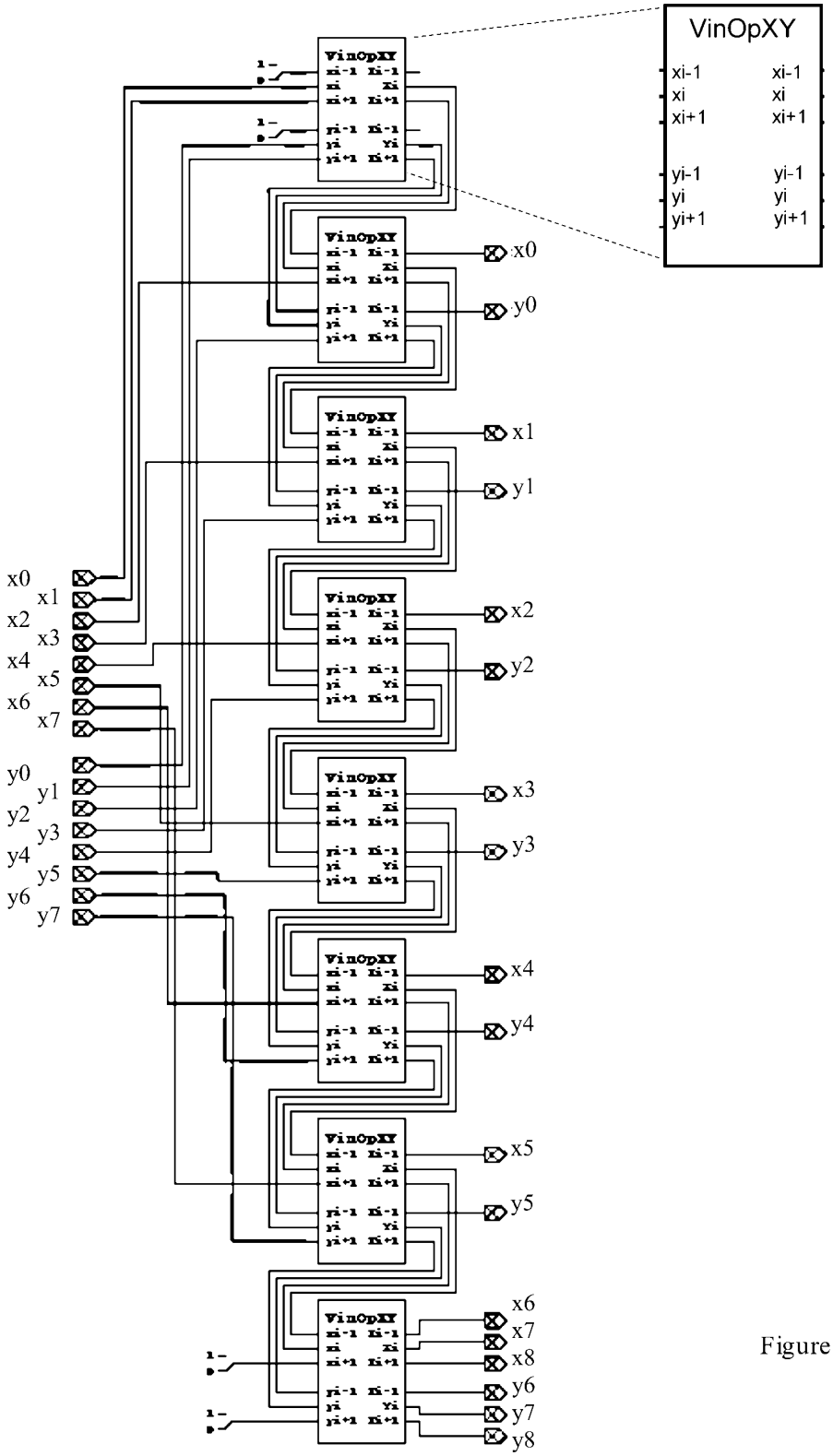

VinOpXY
xi-1 xi-1
xi xi
xi+1 xi+1
yi-1 yi-1
yi yi
yi+1 yi+1
x0
x1
x2
x3
x4
x5
x6
x7
y0
y1
y2
y3
y4
y5
y6
y7
x8
y8

Figure 32

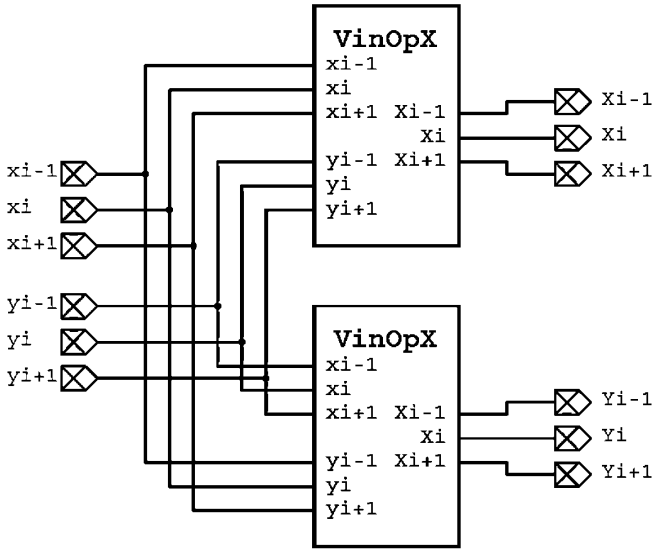


Figure 33

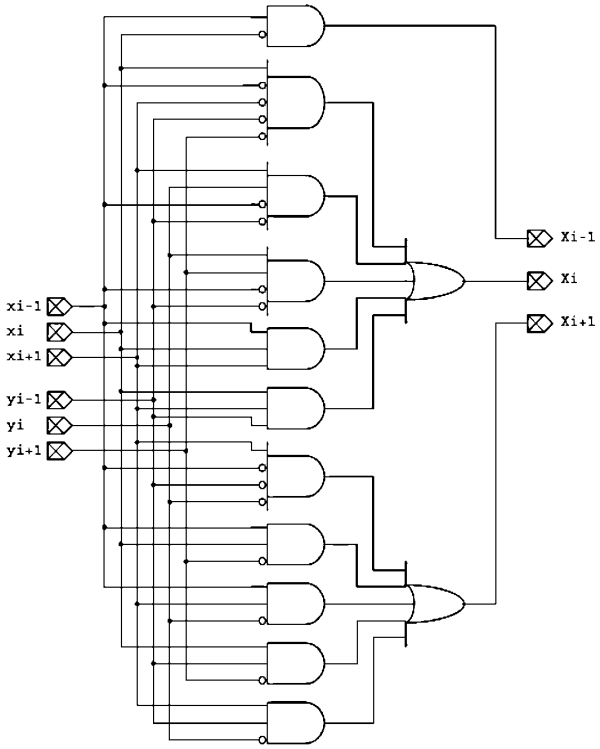


Figure 34

Input n_w			Output N_w			Input n_w			Output N_w			Input n_w			Output N_w		
z_{i+1}	z_i	z_{i-1}	$\hat{Z}_{i+1}$	$\hat{Z}_i$	$\hat{Z}_{i-1}$	z_{i+1}	z_i	z_{i-1}	$\hat{Z}_{i+1}$	$\hat{Z}_i$	$\hat{Z}_{i-1}$	z_{i+1}	z_i	z_{i-1}	$\hat{Z}_{i+1}$	$\hat{Z}_i$	$\hat{Z}_{i-1}$
0	0	0	0	0	0	0	0	1	0	0	1	0	0	$\overline{1}$	0	0	$\overline{1}$
1	0	0	1	0	0	1	0	1	1	0	1	1	0	$\overline{1}$	1	0	$\overline{1}$
$\overline{1}$	0	0	$\overline{1}$	0	0	$\overline{1}$	0	1	$\overline{1}$	0	1	$\overline{1}$	0	$\overline{1}$	$\overline{1}$	0	$\overline{1}$
0	1	0	0	1	0	0	1	1	1	0	0	0	1	$\overline{1}$	1	0	$\overline{1}$
1	1	0	1	$\overline{1}$	0	1	1	1	1	1	0	1	1	$\overline{1}$	1	1	$\overline{1}$
$\overline{1}$	1	0	0	$\overline{1}$	0	$\overline{1}$	1	1	0	0	0	$\overline{1}$	1	$\overline{1}$	0	0	$\overline{1}$
0	$\overline{1}$	0	0	$\overline{1}$	0	0	$\overline{1}$	1	$\overline{1}$	0	1	0	$\overline{1}$	$\overline{1}$	$\overline{1}$	0	0
1	$\overline{1}$	0	0	1	0	1	$\overline{1}$	1	0	0	1	1	$\overline{1}$	$\overline{1}$	0	0	0
$\overline{1}$	$\overline{1}$	0	$\overline{1}$	1	0	$\overline{1}$	$\overline{1}$	1	$\overline{1}$	$\overline{1}$	1	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	0

Note: where Z is shorthand notation of an x substring and an y substring,

Table 6a

Figure 35

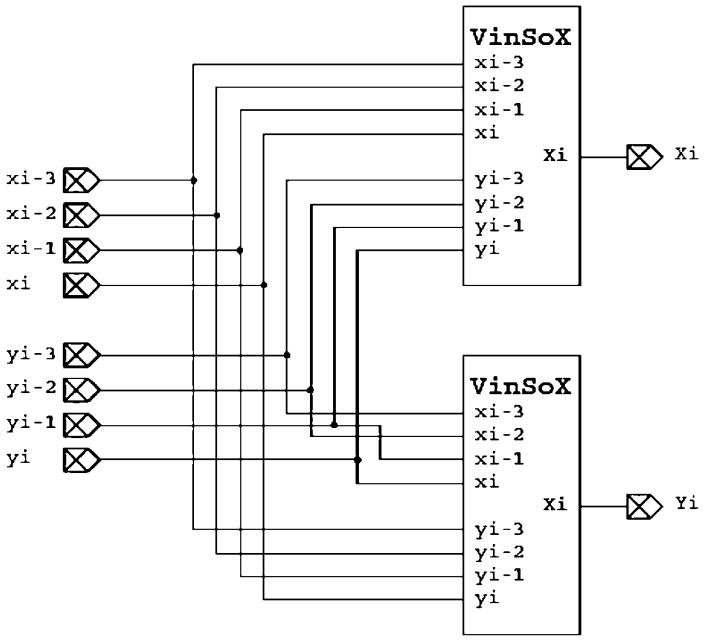


Figure 36

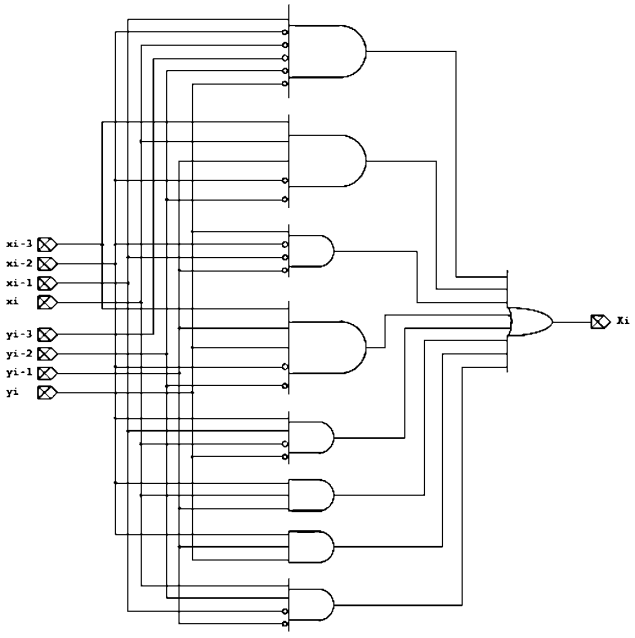


Figure 37a

n_w			$\widetilde{N}_w^1$	n_w			$\widetilde{N}_w^1$	n_w			$\widetilde{N}_w^1$
z_i	z_{i-1}	z_{i-2}	$\widetilde{Z}_i^1$	z_i	z_{i-1}	z_{i-2}	$\widetilde{Z}_i^1$	z_i	z_{i-1}	z_{i-2}	$\widetilde{Z}_i^1$
0	0	0	0	0	0	1	0	0	0	$\overline{1}$	0
0	1	0	1	0	1	1	1	0	1	$\overline{1}$	0
0	$\overline{1}$	0	$\overline{1}$	0	$\overline{1}$	1	0	0	$\overline{1}$	$\overline{1}$	$\overline{1}$
1	0	0	$\overline{1}$	1	0	1	$\overline{1}$	1	0	$\overline{1}$	$\overline{1}$
1	1	0	0	1	1	1	0	1	1	$\overline{1}$	$\overline{1}$
1	$\overline{1}$	0	0	1	$\overline{1}$	1	1	1	$\overline{1}$	$\overline{1}$	0
$\overline{1}$	0	0	1	$\overline{1}$	0	1	1	$\overline{1}$	0	$\overline{1}$	1
$\overline{1}$	1	0	0	$\overline{1}$	1	1	0	$\overline{1}$	1	$\overline{1}$	$\overline{1}$
$\overline{1}$	$\overline{1}$	0	0	$\overline{1}$	$\overline{1}$	1	1	$\overline{1}$	$\overline{1}$	$\overline{1}$	0

Table 6b

Figure 37b

n_w			$\tilde{N}_w^2$	n_w			$\tilde{N}_w^2$	n_w			$\tilde{N}_w^2$
z_i	z_{i-1}	z_{i-2}	$\tilde{Z}_i^2$	z_i	z_{i-1}	z_{i-2}	$\tilde{Z}_i^2$	z_i	z_{i-1}	z_{i-2}	$\tilde{Z}_i^2$
0	0	0	0	0	0	1	0	0	0	$\overline{1}$	0
0	1	0	0	0	1	1	1	0	1	$\overline{1}$	0
0	$\overline{1}$	0	0	0	$\overline{1}$	1	0	0	$\overline{1}$	$\overline{1}$	$\overline{1}$
1	0	0	1	1	0	1	1	1	0	$\overline{1}$	1
1	1	0	$\overline{1}$	1	1	1	*	1	1	$\overline{1}$	$\overline{1}$
1	$\overline{1}$	0	1	1	$\overline{1}$	1	1	1	$\overline{1}$	$\overline{1}$	0
$\overline{1}$	0	0	$\overline{1}$	$\overline{1}$	0	1	$\overline{1}$	$\overline{1}$	0	$\overline{1}$	$\overline{1}$
$\overline{1}$	1	0	$\overline{1}$	$\overline{1}$	1	1	0	$\overline{1}$	1	$\overline{1}$	*
$\overline{1}$	$\overline{1}$	0	1	$\overline{1}$	$\overline{1}$	1	1	$\overline{1}$	$\overline{1}$	$\overline{1}$	

* = impossible inputs

Table 6c

Figure 37c

n_w				$\widetilde{N}_w$	n_w			$\widetilde{N}_w$
z_i	z_{i-1}	z_{i-2}	z_{i-3}	$\widetilde{Z}_i$	z_i	z_{i-1}	z_{i-2}	$\widetilde{Z}_i$
0	0	0	ϕ	0	0	0	1	0
0	1	0	0	1	0	1	1	1
0	1	0	1	1	0	$\overline{1}$	1	0
0	1	0	$\overline{1}$	0	1	0	1	$\overline{1}$
0	$\overline{1}$	0	0	$\overline{1}$	1	1	1	0
0	$\overline{1}$	0	1	0	1	$\overline{1}$	1	1
0	$\overline{1}$	0	$\overline{1}$	$\overline{1}$	$\overline{1}$	0	1	$\overline{1}$
1	0	0	ϕ	$\overline{1}$	$\overline{1}$	1	1	0
1	1	0	0	0	$\overline{1}$	$\overline{1}$	1	1
1	1	0	1	0	0	0	$\overline{1}$	0
1	1	0	$\overline{1}$	$\overline{1}$	0	1	$\overline{1}$	0
1	$\overline{1}$	0	0	0	0	$\overline{1}$	$\overline{1}$	$\overline{1}$
1	$\overline{1}$	0	1	1	1	0	$\overline{1}$	1
1	$\overline{1}$	0	$\overline{1}$	0	1	1	$\overline{1}$	$\overline{1}$
$\overline{1}$	0	0	ϕ	1	1	$\overline{1}$	$\overline{1}$	0
$\overline{1}$	1	0	0	0	$\overline{1}$	0	$\overline{1}$	1
$\overline{1}$	1	0	1	0	$\overline{1}$	1	$\overline{1}$	$\overline{1}$
$\overline{1}$	1	0	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	0
$\overline{1}$	$\overline{1}$	0	0	0				
$\overline{1}$	$\overline{1}$	0	1	1				
$\overline{1}$	$\overline{1}$	0	$\overline{1}$	0				

Note: ϕ = "don't care" whether 0, 1 or $\overline{1}$

Table 7: a semi-optimization algorithm

Figure 38

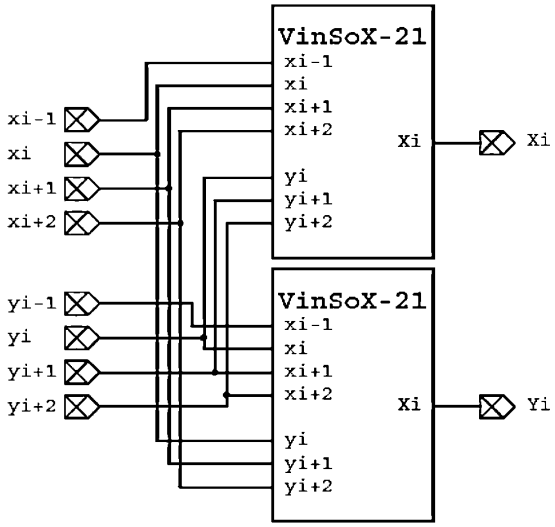


Figure 39

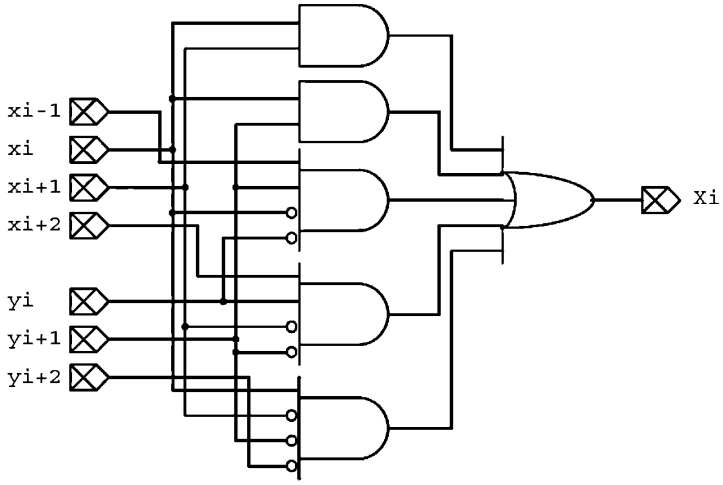


Figure 40

Input n_w				Output n'_w
z_{i+2}	z_{i+1}	z_i	z_{i-1}	z'_i
ϕ	0	0	ϕ	0
0	0	1	ϕ	1
1	0	1	ϕ	1
$\overline{1}$	0	1	ϕ	$\overline{1}$
0	0	$\overline{1}$	ϕ	$\overline{1}$
1	0	$\overline{1}$	ϕ	1
$\overline{1}$	0	$\overline{1}$	ϕ	$\overline{1}$
ϕ	1	0	0	0
ϕ	1	0	1	0
ϕ	1	0	$\overline{1}$	$\overline{1}$
ϕ	1	1	ϕ	1
ϕ	1	$\overline{1}$	ϕ	$\overline{1}$
ϕ	$\overline{1}$	0	0	0
ϕ	$\overline{1}$	0	1	1
ϕ	$\overline{1}$	0	$\overline{1}$	0
ϕ	$\overline{1}$	1	ϕ	1
ϕ	$\overline{1}$	$\overline{1}$	ϕ	$\overline{1}$

Note: ϕ = "don't care" whether 0, 1 or $\overline{1}$

Table 8: Eliminating sub-strings of $10\overline{1}$ and $\overline{1}01$.

Figure 41

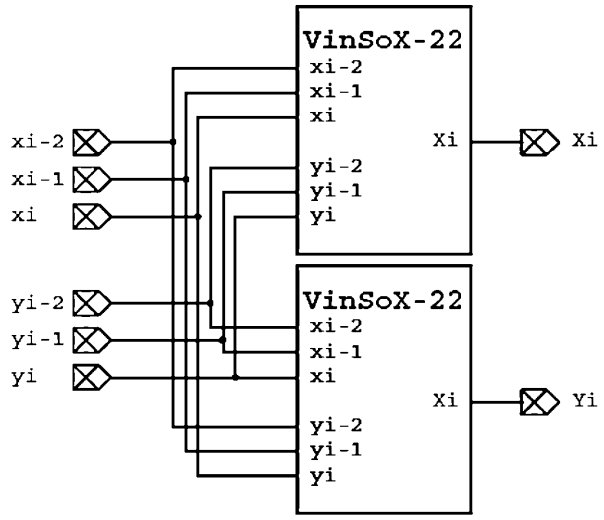


Figure 42

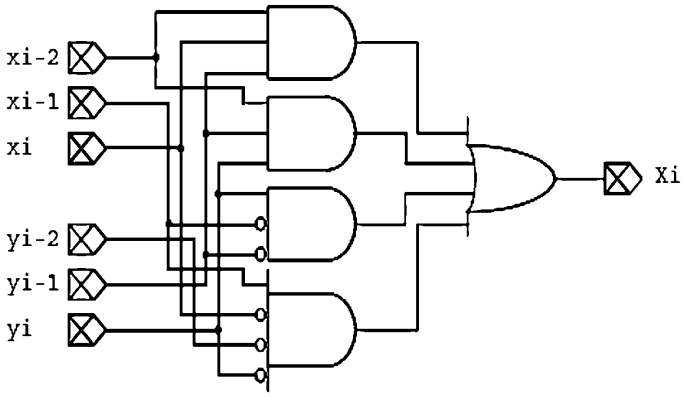


Figure 43

n'_w			$\widetilde{N}_w$	n'_w			$\widetilde{N}_w$	n'_w			$\widetilde{N}_w$
z'_i	z'_{i-1}	z'_{i-2}	$\widetilde{Z}_i$	z'_i	z'_{i-1}	z'_{i-2}	$\widetilde{Z}_i$	z'_i	z'_{i-1}	z'_{i-2}	$\widetilde{Z}_i$
0	0	0	0	1	0	0	$\overline{1}$	$\overline{1}$	0	0	1
0	0	1	0	1	0	1	$\overline{1}$	$\overline{1}$	0	1	*
0	0	$\overline{1}$	0	1	0	$\overline{1}$	*	$\overline{1}$	0	$\overline{1}$	1
0	1	0	1	1	1	0	0	$\overline{1}$	1	0	0
0	1	1	1	1	1	1	0	$\overline{1}$	1	1	0
0	1	$\overline{1}$	0	1	1	$\overline{1}$	$\overline{1}$	$\overline{1}$	1	$\overline{1}$	$\overline{1}$
0	$\overline{1}$	0	$\overline{1}$	1	$\overline{1}$	0	0	$\overline{1}$	$\overline{1}$	0	0
0	$\overline{1}$	1	0	1	$\overline{1}$	1	1	$\overline{1}$	$\overline{1}$	1	1
0	$\overline{1}$	$\overline{1}$	$\overline{1}$	1	$\overline{1}$	$\overline{1}$	0	$\overline{1}$	$\overline{1}$	$\overline{1}$	0

Note: * indicates impossible inputs as $10\overline{1}$ and $\overline{1}01$ have been eliminated.

Table 9: a semi-optimization algorithm.

Figure 44