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FIELD OF THE INVENTION

The present invention relates to methods and apparatus for producing integrated circuit devices and to integrated circuit devices produced thereby.

BACKGROUND OF THE INVENTION

An essential step in the manufacture of all integrated circuit devices is known as "packaging" and involves mechanical and environmental protection of a silicon chip which is at the heart of the integrated circuit as well as electrical interconnection between predetermined locations on the silicon chip and external electrical terminals.

At present three principal technologies are employed for packaging semiconductors: wire bonding, tape automatic bonding (TAB) and flip chip.

Wire bonding employs heat and ultrasonic energy to weld gold bonding wires between bond pads on the chip and contacts on the package.

Tape automatic bonding (TAB) employs a copper foil tape instead of bonding wire. The copper foil tape is configured for each specific die and package combination and includes a pattern of copper traces suited thereto. The individual leads may be connected individually or as a group to the various bond pads on the chip.

Flip chips are integrated circuit dies which have solder bumps formed on top of the bonding pads, thus allowing the die to be "flipped" circuit side down and directly soldered to a substrate. Wire bonds are not required and considerable savings in package spacing may be realized.

The above-described technologies each have certain limitations. Both wire bonding and TAB bonding are prone to bad bond formation and subject the die to

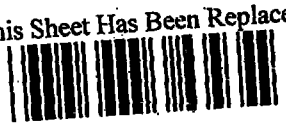
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☐ Claim(s) : paged ..... to paged .....
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relatively high temperatures and mechanical pressures. Both wire bond and TAB technologies are problematic from a package size viewpoint, producing integrated circuit devices having a die-to-package area ratio ranging from about 10% to 60%.

The flip-chip does not provide packaging but rather only interconnection. The interconnection encounters problems of uniformity in the solder bumps as well as in thermal expansion mismatching, which limits the use of available substrates to silicon or materials which have thermal expansion characteristics similar to those of silicon.

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SUMMARY OF THE INVENTION

The present invention seeks to provide apparatus and techniques for production of integrated circuit device overcome many of the above limitations and provide integrated circuits of relatively smaller size and weight and enhanced electrical performance.

There is thus provided in accordance with a preferred embodiment of the present invention a method for producing integrated circuit devices including the steps of:

producing a plurality of integrated circuits on a wafer having first and second planar surfaces, each of the integrated circuits including a multiplicity of pads;

waferwise attaching to both said surfaces of the wafer a layer of protective material;

thereafter partially cutting into the wafer and the protective material attached thereto, thereby to define notches along outlines of a plurality of prepackaged integrated circuit devices;

forming metal contacts onto the plurality of prepackaged integrated circuit devices while they are still joined together on the wafer, at least a portion of said metal contacts extending into the notches; and

thereafter separating the plurality of prepackaged integrated circuit devices into individual devices.

Throughout the specification and claims, the terms "cutting" and "cut" shall have broader than usual meaning and shall refer to removal of material or separating along a line by any suitable technique, such as, for example, etching, sawing, sandblasting and milling.

It is noted that the term "waferwise" does not require that a whole wafer be so processed at a given time. "Waferwise" applies equally to steps

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applied to multiple dies prior to dicing thereof.

In accordance with a preferred embodiment of the present invention the step of partially cutting exposes sectional surfaces of the multiplicity of pads.

Preferably the step of partially cutting cuts pads so as to simultaneously define electrical contact regions for both of a pair of adjacent integrated circuits.

Additionally in accordance with a preferred embodiment of the present invention there is provided a method for producing integrated circuit devices including the steps of:

producing a plurality of integrated circuits on a wafer, each of the integrated circuits including a multiplicity of pads; and

thereafter partially cutting the wafer, thereby to define notches along outlines of a plurality of integrated circuit, and wherein the step of partially cutting exposes sectional surfaces of the multiplicity of pads.

Preferably the step of partially cutting cuts a plurality of pads including some which communicate with a one of a pair of adjacent integrated circuits and others with communication with another of the pair of adjacent integrated circuits, thereby to define electrical contact regions for both of said pair of adjacent integrated circuits.

In accordance with a preferred embodiment of the present invention there are also provided steps of providing a conductive layer over notched edges of the integrated circuits in electrical communication with the exposed edges of the pads and wherein portions of the conductive layer communicating with separate ones of the multiplicity of pads are electrically separated from one another.

In accordance with a preferred embodiment of the present invention, the step of providing a conductive layer comprises forming a conductive coating

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also over non-edge portions of the integrated circuit.

Preferably the partially cutting step is carried out at locations whereby the silicon substrate is not exposed at the notched edges of the resulting integrated circuits.

In accordance with a preferred embodiment of the present invention, prior to the partially cutting step, the integrated circuits are surrounded on their planar surfaces by protective insulation layers and on their edges by epoxy.

Preferably a thermal bonding pad is formed on at least one outer planar surface of said integrated circuit devices.

Additionally in accordance with a preferred embodiment of the present invention there is also provided the step of providing an integrally formed ground plane in said integrated circuit devices.

Preferably, the protective layer is transparent to radiation which is used for erasing EPROM devices.

Additionally in accordance with a preferred embodiment of the present invention there is provided apparatus for producing integrated circuit devices including:

apparatus for producing a plurality of integrated circuits on a wafer having opposite planar surfaces, each of the integrated circuits including a multiplicity of pads;

apparatus for waferwise attaching to both said surfaces of the wafer a layer of protective packaging material; and

partially cutting apparatus for thereafter partially cutting the wafer and the protective material attached thereto, thereby to define notches along outlines of a plurality of prepackaged integrated circuit devices;

metal coating apparatus for forming metal contacts onto the plurality of prepackaged integrated

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circuit devices while they are still joined together on the wafer, at least a portion of the metal contacts extending into the notches; and

separating apparatus for thereafter separating the plurality of prepackaged integrated circuit devices into individual devices.

Preferably the partially cutting apparatus exposes sectional surfaces of the multiplicity of pads and cuts pads which communicate with adjacent integrated circuits, thereby to simultaneously define electrical contact regions for the adjacent integrated circuits.

Further in accordance with a preferred embodiment of the invention there is provided apparatus for producing integrated circuit devices including:

apparatus for producing a plurality of integrated circuits on a wafer, each of the integrated circuits including a multiplicity of pads; and

partially cutting apparatus for thereafter partially cutting the wafer, thereby to define notches along outlines of a plurality of integrated circuit elements which expose sectional surfaces of the multiplicity of pads.

Preferably, the partially cutting apparatus cuts a plurality of pads including some which communicate with a one of a pair of adjacent integrated circuits and others with communication with another of the pair of adjacent integrated circuits, thereby to define electrical contact regions for both of said pair of adjacent integrated circuits.

In accordance with a preferred embodiment of the present invention there is also provided apparatus for providing a conductive layer over notched edges of the integrated circuit in electrical communication with the edges of the pads and for electrically separating portions of the conductive layer communicating with separate ones of the multiplicity of pads.

Preferably, the conductive layer comprises a

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conductive coating over more than the edge of the integrated circuit.

Preferably the partially cutting apparatus is operative at locations whereby the silicon substrate is not exposed at the notched edges of the resulting integrated circuits.

Preferably the apparatus of the present invention is operative to carry out any and all of the above-mentioned method steps.

In accordance with a preferred embodiment of the invention there is provided an integrated circuit device constructed according to a method or using apparatus having any of the foregoing features.

Additionally in accordance with a preferred embodiment of the present invention there is provided an integrated circuit device comprising:

an integrated circuit die having top and bottom surfaces formed of electrically insulative and mechanically protective material and electrically insulative edge surfaces having exposed sections of conductive pads and being inclined with respect to the top and bottom surfaces.

Additionally in accordance with a preferred embodiment of the present invention, the integrated circuit device includes an integrally formed thermal contact to a heat sink on an outer planar surface of the device and an integrally formed ground plane.

Preferably conductive strips are formed on the outside surface of the integrated circuit device for interconnecting the exposed sections of conductive pads at a plurality of edges.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

Fig. 1 is a simplified pictorial illustration of an integrated circuit device constructed and operative in accordance with a preferred embodiment of the present invention;

Fig. 2 is a simplified pictorial illustration of the attachment of a protective packaging layer to a wafer containing a plurality of integrated circuit dies;

Fig. 3 is a simplified pictorial illustration of scribing of the wafer to define individual dies, following the attachment of a protective packaging layer to the wafer;

Figs. 4A, 4B, 4C, 4D and 4E are sectional illustrations of various stages in the manufacture of integrated circuit devices in accordance with a preferred embodiment of the present invention;

Fig. 5 is a partially cut away detailed pictorial illustration of an integrated circuit device produced from the wafer of Fig. 4E;

Figs. 6, 7 and 8 are sectional illustrations of various stages in the manufacture of the integrated circuit device shown in Figs. 1 & 5; and

Figs. 9 and 10 together provide a simplified block diagram illustration of apparatus for carrying out the method of the present invention.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference is now made to Figs. 1 - 10, which illustrate the production of integrated circuit devices in accordance with a preferred embodiment of the present invention.

Fig. 1 illustrates a preferred embodiment of integrated circuit device constructed and operative in accordance with a preferred embodiment of the present invention and includes a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package 10 having a multiplicity of electrical contacts 12 plated along the edge surfaces 14 thereof. In accordance with a preferred embodiment of the invention, contacts 12 extend over edge surfaces onto the planar surfaces 16 of the package. This contact arrangement permits both flat surface mounting and edge mounting of package 10 onto a circuit board. It is noted that the integrated circuit package 10 may include an integrally formed ground plane (not shown) as well as ground plane contacts 18.

In accordance with a preferred embodiment of the present invention, the integrated circuit package 10 may also include one or more thermal bonding pads 19 formed on one or both of the planar surfaces 16 thereof. The provision of such thermal bonding pads 19 is optional.

In accordance with a preferred embodiment of the present invention, and as illustrated in Fig. 2 and Fig. 4A, a complete silicon wafer 20 having a plurality of finished dies 22 formed thereon by conventional techniques, is bonded at its active surface 24 to an insulating cover plate 26 via a layer 28 of epoxy. The insulating cover plate 26 typically comprises glass, alumina, beryllia, sapphire or any other suitable insulative substrate.

Cover plate 26 may be transparent to radiation in a spectral region useful for optical or

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infrared alignment.

It is appreciated that certain steps in the conventional fabrication of silicon wafer 20 may be eliminated when the wafer is used in accordance with the present invention. These steps include the provision of via openings above pads, wafer back grinding and wafer back metal coating.

The complete silicon wafer 20 may be formed with an integral ground plane by conventional lithography techniques at any suitable location therein. Alternatively prior to the bonding step of Fig. 4A, a ground plane may be deposited and configured by conventional techniques over the active surface 24, such that the ground plane lies between active surface 24 and the epoxy layer 28.

Following the bonding step described hereinabove, the silicon wafer is preferably ground down to a decreased thickness, typically 200 microns, as shown in Fig. 4B. This reduction in wafer thickness is enabled by the additional mechanical strength provided by the bonding thereof of the insulating cover plate 26.

Following the reduction in thickness of the wafer, which is optional, the wafer is scribed along its back surface along predetermined dice lines which separate the individual dies. The scribed channels 30 are of sufficient depth to reduce the wafer thickness thereunder to typically 100 microns. The scribed wafer is shown in Fig. 3 and in Fig. 4C.

The scribed wafer is then etched in a conventional silicon etching solution, such as a combination of 2.5% hydrofluoric acid, 50% nitric acid, 10% acetic acid and 37.5% water, so as to etch the silicon down to the field oxide layer, as shown in Fig. 4D.

The result of the silicon etching is a plurality of separated dies 40, each of which includes silicon of thickness about 100 microns.

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As seen in Fig. 4E, following the silicon etching, a second insulating packaging layer 42 is bonded over the dies 40 on the side thereof opposite to insulating packaging layer 26. A layer 44 of epoxy lies between the dies 40 and the layer 42 and epoxy also fills the interstices between dies 40.

The sandwich of the etched wafer 20 and the first and second insulating packaging layers 26 and 42 is then partially cut along lines 50, lying along the interstices between adjacent dies 40 to define notches along the outlines of a plurality of pre-packaged integrated circuits. It is a particular feature of the invention that lines 50 are selected such that the edges of the dies along the notches are distanced from the outer extent of the silicon 40 by at least a distance d, as shown in Figs. 4E and 5, to which reference is now additionally made.

It is a particular feature of the present invention that partial cutting of the sandwich of Fig. 4E along lines 50 exposes edges of a multiplicity of pads 34 on the wafer 20, which pad edges, when so exposed, define contact surfaces 51 on dies 40. Partial cutting of the sandwich of Fig. 4E also exposes edge portions of the ground plane 38 which define ground plane contact surfaces 52.

Referring now particularly to Fig. 5, at least one insulating layer, including the field oxide layer, is shown at reference numeral 32 and metal pads are shown at reference numeral 34. An over-metal insulating layer is shown at reference numeral 36. The ground plane is shown at reference numeral 38.

It is seen that the notch produced by partial cutting as in Fig. 4E typically as inclined sidewalls, as illustrated in Fig. 5. This need not necessarily be the case, however.

Reference is now made to Figs. 6, 7 and 8, which illustrate further steps in the manufacture of integrated circuit devices in accordance with a

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preferred embodiment of the present invention.

Fig. 6 illustrates at reference numeral 54, a preferred cross sectional configuration of a notch produced by partially cutting as described hereinabove in connection with Fig. 4E. Vertical lines 56 indicate the intersection of the notch 54 with the pads 34, defining exposed sectional pad surfaces 51. Vertical lines 58 indicate the location of a subsequent final cut which separates the dies into individual integrated circuits at a later stage.

Fig. 7 illustrates the formation of metal contacts 12 along the inclined edges 14 and part of the top surface 16. These contacts, which may be formed by any suitable metal deposition technique, are seen to extend inside notch 54, thus establishing electrical contact with surfaces 51 of pads 34.

It is a particular feature of the present invention that metal contacts are formed onto the dies in electrical contact with surfaces 51 of pads 34 without first separating the dies into individual chips.

Fig. 8 illustrates subsequent dicing of the individual dies on the wafer, subsequent to metal contact formation thereon, into individual pre-packaged integrated circuit devices.

Reference is now made to Figs. 9 and 10, which together illustrate apparatus for producing integrated circuit devices in accordance with a preferred embodiment of the present invention. A conventional wafer fabrication facility 180 provides complete wafers 20. Individual wafers 20 are bonded on their active surfaces by bonding apparatus 182, preferably having facilities for rotation of the wafer 20, the layer 26 and the epoxy 28 so as to obtain even distribution of the epoxy.

The bonded wafer (Fig. 3) is thinned at its non-active surface as by grinding apparatus 184, such as Model 32BTGW using 12.5A abrasive, which is

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commercially available from Speedfam Machines Co. Ltd. of England.

The wafer is then scribed at its non-active surface by scribing apparatus 186 such as a Kulicke & Soffa 775 dicing saw employing an Ni plated diamond loaded blade, producing a result which is shown in Fig. 4C.

The scribed wafer of Fig. 4C is then etched in a temperature controlled bath 188 containing a silicon etch solution 190. Commercially available equipment for this purpose include a Chemkleen bath and an WHRV circulator both of which are manufactured by Wafab Inc. of the U.S.A.. A suitable conventional silicon etching solution is Isoform Silicon etch, which is commercially available from Micro-Image Technology Ltd. of England. The wafer is conventionally rinsed after etching. The resulting etched wafer is shown in Fig. 4D.

The etched wafer is bonded on the non-active side to another protective layer 42 by bonding apparatus 192, which may be essentially the same as apparatus 182, to produce a doubly bonded wafer sandwich as shown in Fig. 4E.

Notching apparatus 194, which may be identical to apparatus 186, partially cuts the bonded wafer sandwich of Fig. 4E to a configuration shown in Fig. 5.

The notched wafer is then subjected to anti-corrosion treatment in a bath 196, containing a chromating solution 198, such as described in any of the following U.S. Patents: 2,507,956; 2,851,385 and 2,796,370, the disclosure of which is hereby incorporated by reference.

Conductive layer deposition apparatus 200, which operates by vacuum deposition techniques, such as a Model 903M sputtering machine manufactured by Material Research Corporation of the U.S.A., is employed to produce a conductive layer on one or more

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surfaces of each die of the wafer as shown in Fig. 7.

Configuration of contact strips, as shown in Fig. 7, is carried out preferably by using conventional electro-deposited photoresist, which is commercially available from DuPont under the brand name Primecoat or from Shipley, under the brand name Eagle. The photoresist is applied to the wafers in a photoresist bath assembly 202 which is commercially available from DuPont or Shipley.

The photoresist is preferably laser configured by a suitable laser scanner 204 to define suitable etching patterns. The photoresist is then developed in a development bath 206, and then etched in a metal etch solution 208 located in an etching bath 210, thus providing a conductor configuration such as that shown in Fig. 1.

The exposed conductive strips shown in Fig. 7 are then plated, preferably by electroless plating apparatus 212, which is commercially available from Okuno of Japan.

The wafer is then diced into individual prepackaged integrated circuit devices. Preferably the dicing blade 214 should be a diamond resinoid blade of thickness 4 - 12 mils. The resulting dies appear as illustrated generally in Fig. 1.

It will be apparent to persons skilled in the art that the present invention is not limited to what has been particularly shown and described hereinabove. Rather the scope of the present invention is defined only by the claims which follow:

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1. A method for producing integrated circuit devices including the steps of:

producing a plurality of integrated circuits on a wafer having first and second planar surfaces, each of the integrated circuits including a multiplicity of pads;

waferwise attaching to both said surfaces of the wafer a layer of protective material;

thereafter partially cutting into the wafer and the protective material attached thereto, thereby to define notches along outlines of a plurality of prepackaged integrated circuit devices;

forming metal contacts onto the plurality of prepackaged integrated circuit devices while they are still joined together on the wafer, at least a portion of said metal contacts extending into the notches; and

thereafter separating the plurality of prepackaged integrated circuit devices into individual devices.

2. A method according to claim 1 and wherein the step of partially cutting exposes sectional surfaces of the multiplicity of pads.

3. A method according to claim 1 and wherein the step of partially cutting cuts pads so as to simultaneously define electrical contact regions for both of a pair of adjacent integrated circuits.

4. A method for producing integrated circuit devices including the steps of:

producing a plurality of integrated circuits on a wafer, each of the integrated circuits including a multiplicity of pads; and

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thereafter partially cutting the wafer, thereby to define notches along outlines of a plurality of integrated circuits thereby exposing sectional surfaces of the multiplicity of pads.

5. A method according to claim 4 and wherein the step of partially cutting cuts a plurality of pads including some which communicate with a one of a pair of adjacent integrated circuits and others with communication with another of the pair of adjacent integrated circuits, thereby to define electrical contact regions for both of said pair of adjacent integrated circuits.

6. A method according claim 4 and also comprising the steps of providing a conductive layer over notched edges of the integrated circuits in electrical communication with the exposed edges of the pads and wherein portions of the conductive layer communicating with separate ones of the multiplicity of pads are electrically separated from one another.

7. A method according to claim 6 and wherein the step of providing a conductive layer comprises forming a conductive coating also over non-edge portions of the integrated circuit.

8. A method according to claim 4 and wherein the partially cutting step is carried out at locations whereby the silicon substrate is not exposed at the notched edges of the resulting integrated circuits.

9. A method according to claim 4 and wherein prior to the partially cutting step, the integrated circuits are surrounded on their planar surfaces by protective insulation layers and on their edges by epoxy.

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10. A method according to claim 4 and wherein a thermal bonding pad is formed on at least one outer planar surface of said integrated circuit devices.

11. A method according to claim 4 and also comprising the step of providing an integrally formed ground plane in said integrated circuit devices.

12. A method according to claim 10 and wherein said protective insulation layer is transparent to radiation which is used for erasing EPROM devices.

13. Apparatus for producing integrated circuit devices including:

apparatus for producing a plurality of integrated circuits on a wafer having opposite planar surfaces, each of the integrated circuits including a multiplicity of pads;

apparatus for waferwise attaching to both said surfaces of the wafer a layer of protective packaging material; and

partially cutting apparatus for thereafter partially cutting the wafer and the protective material attached thereto, thereby to define notches along outlines of a plurality of prepackaged integrated circuit devices;

metal coating apparatus for forming metal contacts onto the plurality of prepackaged integrated circuit devices while they are still joined together on the wafer, at least a portion of the metal contacts extending into the notches; and

separating apparatus for thereafter separating the plurality of prepackaged integrated circuit devices into individual devices.

14. Apparatus according to claim 13 and wherein the partially cutting apparatus exposes sectional surfaces of the multiplicity of pads and cuts pads

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which communicate with adjacent integrated circuits, thereby to simultaneously define electrical contact regions for the adjacent integrated circuits.

15. Apparatus for producing integrated circuit devices including:

apparatus for producing a plurality of integrated circuits on a wafer, each of the integrated circuits including a multiplicity of pads; and

partially cutting apparatus for thereafter partially cutting the wafer, thereby to define notches along outlines of a plurality of integrated circuit elements which expose sectional surfaces of the multiplicity of pads.

16. Apparatus according to claim 15 and wherein the partially cutting apparatus cuts a plurality of pads including some which communicate with a one of a pair of adjacent integrated circuits and others with communication with another of the pair of adjacent integrated circuits, thereby to define electrical contact regions for both of said pair of adjacent integrated circuits.

17. Apparatus according to claim 15 and also comprising apparatus for providing a conductive layer over notched edges of the integrated circuit in electrical communication with the edges of the pads and for electrically separating portions of the conductive layer communicating with separate ones of the multiplicity of pads.

18. Apparatus according to claim 17 and wherein the conductive layer comprises a conductive coating over more than the edge of the integrated circuit.

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19. Apparatus according to claim 15 and wherein the partially cutting apparatus is operative at locations whereby the silicon substrate is not exposed at the notched edges of the resulting integrated circuits.

20. An integrated circuit device comprising:

an integrated circuit die having top and bottom surfaces formed of electrically insulative and mechanically protective material and electrically insulative edge surfaces having exposed sections of conductive pads and being inclined with respect to the top and bottom surfaces.

21. An integrated circuit device manufactured according to the method of claim 1.

22. An integrated circuit device according to claim 21 and also including at least one of an integrally formed thermal contact to a heat sink on an outer planar surface of the device and an integrally formed ground plane.

23. Apparatus according to any of the preceding claims, substantially as shown and described hereinabove.

24. A method according to any of the preceding claims, substantially as shown and described hereinabove.

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25. Apparatus according to any of the preceding claims, substantially as shown and described in any of the drawings.



26. A method according to any of the preceding claims, substantially as shown and described in any of the drawings.

For the applicant,

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C: 18268 HB-9401

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