CLAIMS

1. A structure comprising:

   - a patterned crystalline semiconductor substrate made from a first crystalline semiconductor material with elevated regions bounded by trenches, the depth (h) of said trenches larger than their width (d); and
   - epitaxial semiconductor material deposited on said elevated substrate regions in the form of isolated, stress-free semiconductor patches; said epitaxial semiconductor material comprising at least one second crystalline semiconductor material having a lattice mismatch or thermal mismatch to said substrate;

   wherein perpendicular sidewalls of adjacent patches are spaced, the spacing of said perpendicular sidewalls being smaller than the width (d) of said trenches, so that most of the epitaxial material is deposited on top of said elevated regions.

2. The structure of claim 1, wherein the height of said adjacent patches is larger than their width.~~:~~

~~— said substrate is made from a first crystalline semiconductor material; and~~

~~— said epitaxial semiconductor material comprises at least one second crystalline semiconductor material having a lattice mismatch or thermal mismatch to said substrate.~~

3. The structure of claim 1, wherein epitaxial regions consisting of merged structures are formed on said elevated regions.

4. The structure of claim 1, wherein said elevated substrate regions are faceted.

5. The structure of claim 1, wherein sidewalls and bottoms of said trenches are covered with a dielectric layer of thickness d_{ox}, said thickness d_{ox} being small with respect to the trench width (d).

6. The structure of claim 1, wherein said elevated regions comprise at least one region, the boundary of which is aligned along a symmetry direction of said substrate.